

AC200 Processor Certification Requirements Document

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CRD Revision History

History of documentation changes that eventually lead to releases.

Date	Revision	Changes
2025-03-07	0.1.0	Created

Typographic Conventions

CSR field colors

- Grey fields are reserved (WPRI)
- Green fields are present
- Red fields are defined by the RISC-V ISA but not present

CSR field types

Abbreviation	Description
RO	Read-Only Field has a hardwired value that does not change. Writes to an RO field are ignored.
RO-H	Read-Only with Hardware update Writes are ignored. Reads reflect a value dynamically generated by hardware.
RW	Read-Write Field is writable by software. Any value that fits in the field is acceptable and shall be retained for subsequent reads.
RW-R	Read-Write Restricted Field is writable by software. Only certain values are legal. Writing an illegal value into the field is ignored, and the field retains its prior state.
RW-H	Read-Write with Hardware update Field is writable by software. Any value that fits in the field is acceptable. Hardware also updates the field without an explicit software write.
RW-RH	Read-Write Restricted with Hardware update Field is writable by software. Only certain values are legal. Writing an illegal value into the field is ignored, such that the field retains its prior state. Hardware also updates the field without an explicit software write.)

Glossary

Table 1. Glossary

Term	Meaning
RISC-V	(Reduced Instruction Set Computer) architecture, version 5
RVI	RISC-V International (organization that oversees RISC-V)
RVCP	RISC-V Certification Program
TSC	Technical Steering Committee (branch of RVI that creates standards)
CSC	Certification Steering Committee (branch of RVI that oversees the RVCP)
CRD	Certification Requirements Document
CTP	Certification Test Plan
CSR	Control & Status Register (located inside processor, not memory-mapped)
TBD	To Be Determined
N/A	“Not Applicable”
AKA	“Also Known As”
Must	Indicates a mandatory requirement
Should	Indicates a recommended requirement
May	Indicates an optional requirement

1. Introduction

The AC200 Processor Certificate targets RISC-V Apps Processors running rich operating systems such as commercial Linux distributions or Android. Software source code compatibility and binary compatibility between implementations are strong requirements.

AC200 is based on the following:

- RVA23 Profile (includes mandatory Hypervisor and Vector support)
- M-mode requirements
- AIA or PLIC interrupt controller
- Debug and trace (TBD)

The AC (Apps processor Class) targets processors that support virtual memory and run rich operating systems such as Linux and Android.

1.1. What’s a CRD?

Certification Requirements Documents (CRDs) list requirements an implementation must meet to obtain an associated RVI (RISC-V International) certificate. CRDs are developed by the RVI CSC (Certification Steering Committee) organization in collaboration with the RVI TSC (Technical Steering Committee) organization who creates RISC-V standards.

The CRDs refer to and augment information provided in existing ratified RVI standards.

There are a variety of certificates offered by RVI to accomodate the various RVI standards. There are certificates for processors, non-processor system IP (e.g., IOMMU), and system platforms (processor + system IP) hardware standards. There are multiple classes of processor certificates available to accomodate the wide range of RISC-V implementations from basic microcontrollers to advanced Applications-class processors.

Each CRD has a list of mandatory behaviors along with a list of optional behaviors. Note that not all behaviors allowed in RISC-V standards are supported by a particular CRD.

1.2. Naming Scheme

1.2.1. CRD Naming

All components of the RVCP share the following naming scheme:

Format: <name>[v<version>]

Where:

- Left & right square braces denote optional.
- Less-than & greater-than signs just separate fields (i.e., they aren’t present in the CRD name).
- <name> identifies the type of RISC-V standard (processor, non-processor system IP, or platform) along with any other information required to

identify the variant of that standard.

- <version> identifies a particular release
 - Format is <major>[.<minor>[.<patch>]]
 - Inspired by semantic versioning scheme (semver.org/) but doesn't follow it exactly

The rules for updating <major>, <minor>, and <patch> are defined by the type of RVCP component. However, the follow these general guidelines:

- A <major> release of 0 is used for pre-release versions and release versions start with 1.
- The <major> release number is updated when mandatory changes are made.
- The <minor> release number is updated when optional changes are made.
- The <patch> release number is updated for documentation fixes/improvements that don't affect certificates already obtained for a particular implementation.

The specific rules for updating the version number of a CRD are as follows:

- The <major> release number is updated for changes that **could** cause a previously certified implementation to no longer meet requirements. An example is requiring a new version of a standard.
- The <minor> release number is updated for increased support of optional behaviors.
- The <patch> release number is updated for documentation fixes/improvements. These changes **cannot** cause a previously certified implementation to no longer meet requirements.

1.2.2. Processor Naming

RVCP components for processors have the following format for their <name>:

```
<class><model>[<-base>]
```

Where:

- <class> is MC for Microcontroller Class and AC for Apps-processor Class
- <model> is 3-digit integer defined as follows:
 - The hundreds's digit indicates the series
 - The ten's digit identifies large differences in mandatory extensions (e.g., V, H) within the series
 - The one's digit indentifies small/medium differences in mandatory extensions (e.g., Zicond, PMP) within the series
- <base> is optional and is 32 for RV32I, 64 for RV64I, and 32E for RV32E
 - If multiple bases are supported and <base> is omitted in a reference, the reference applies to all bases
 - If only one base is supported then <base> is generally omitted

1.3. Requirements Terminology

Table 2. Requirement Types

Term	Meaning
MANDATORY	You have to implement it to get a certificate and the certificate tests will cover it
OPTIONAL	It's up to you if you implement or not. If you claim to implement it, certificate tests will cover it
IN-SCOPE	Either MANDATORY or OPTIONAL
OUT-OF-SCOPE	It's up to you if you implement or not. If you implement it, it won't be certified but make sure you don't mess up anything we are certifying.
INCOMPATIBL E	If you implement it you won't get a certificate

Table 3. Definition of CSR Fields

Field Type	Read Value After Writing Illegal Value	Read Value Function Of	Illegal Instruction Exception	Priv ISA Manual Quote
WLRL	Any deterministic legal or illegal value	Value before write and illegal value written	Optional	Implementations are permitted but not required to raise an illegal-instruction exception if an instruction attempts to write a non-supported value to a WLRL field. Implementations can return arbitrary bit patterns on the read of a WLRL field when the last write was of an illegal value, but the value returned should deterministically depend on the illegal written value and the value of the field prior to the write.

Field Type	Read Value After Writing Illegal Value	Read Value Function Of	Illegal Instruction Exception	Priv ISA Manual Quote
WARL	Any deterministic legal value	Any architectural hart state	Prohibited	Implementations will not raise an exception on writes of unsupported values to a WARL field. Implementations can return any legal value on the read of a WARL field when the last write was of an illegal value, but the legal value returned should deterministically depend on the illegal written value and the architectural state of the hart.
WPRI	0	Nothing	Not specified	Some whole read/write fields are reserved for future use. Implementations that do not furnish these fields must make them read-only zero.

WARL (Write Anything, Read Legal):

The Priv ISA requires reads of WARL fields to return some implementation-dependent deterministic legal value after the field is written with an illegal value. Certifying such behaviors is expensive and provides low value for a certificate since software can’t rely on a particular behavior from one implementation to another.

Processor CRDs define writes to WARL fields of illegal values to be OUT-OF-SCOPE unless otherwise stated (i.e., certification tests will only ever write legal values to WARL fields except for the special cases listed below). When not OUT-OF-SCOPE, the required behavior is defined as this might be more constrained in implementations than in the standard.

The following special cases for WARL are supported when explicitly listed in the corresponding CRD CSR field requirements:

- Probing for Field Width
 - Some WARL fields are variable length such as the ASID field in the virtual memory extension.
 - Here’s the algorithm recommended to discover the ASID width:
 - The number of implemented ASID bits, termed ASIDLEN, may be determined by writing one to every bit position in the ASID field, then reading back the value in the satp CSR to see which bit positions in the ASID field hold a one.
 - The RVCP-provided certification materials (certification tests, certification reference models) can map writes of illegal values to the ASID field to the corresponding read value as long as they are provided the ASIDLEN value for an implementation.
- Probing for Options
 - E.g., Writable misa bits
- Allowed values are a function of extension presence and/or their parameters
 - E.g., satp.mode legal write values

WLRL (Write Legal, Read Legal):

The Priv ISA requires reads of WLRL fields to return some implementation-dependent deterministic arbitrary value after the field is written with an illegal value. Certifying such behaviors is expensive and provides low value for a certificate since software can’t rely on a particular behavior. Processor CRDs define writes to WLRL fields of illegal values to be OUT-OF-SCOPE unless otherwise stated (i.e., certification tests will only ever write legal values to WLRL fields).

WPRI (Write Preserve, Read Ignore):

The Priv ISA requires reads of WPRI fields to return a value of 0. Such WPRI fields are always unimplemented by definition. Certification tests are aware of which fields in the CSRs are WPRI and normally write them with 0 but will also write them with ~0 (all ones) and ensure that reads return 0 in both cases. It is OUT-OF-SCOPE for certification tests to write all possible values of WPRI fields (especially if they are more than just a few bits) and certification tests aren’t intended to be comprehensive verification test suites anyways.

1.4. Related Specifications

Certificate Model	TSC Profile	Unpriv ISA Manual	Priv ISA Manual	Debug Manual
AC200	RVA23	20240411	20240411	1.0.0

1.5. Privileged Modes

M	S	U	HS	VS	VU
IN-SCOPE	IN-SCOPE	IN-SCOPE	IN-SCOPE	IN-SCOPE	IN-SCOPE

2. Extensions

Any RISC-V extensions not listed in this section are OUT-OF-SCOPE. The AC200 certificate doesn't cover their behaviors.

2.1. Mandatory Extensions

The AC200 certificate has 58 mandatory extensions.

Requirement ID	Extension	Version	Long Name	Note
REQ-EXT-A	A	~> 2.1	Atomic instructions	
REQ-EXT-B	B	~> 1.0.0	Bit Manipulation	
REQ-EXT-C	C	~> 2.0	Compressed instructions	
REQ-EXT-D	D	~> 2.2	Double-precision floating-point	NOTE: The rationale to not include Q as a profile option is that quad-precision floating-point is unlikely to be implemented in hardware, and so we do not require or expect software to expend effort optimizing use of Q instructions in case they are present.
REQ-EXT-F	F	~> 2.2	Single-precision floating-point	
REQ-EXT-I	I	~> 2.1	Base integer ISA (RV32I or RV64I)	RVI is the mandatory base ISA for RVA, and is little-endian. As per the unprivileged architecture specification, the ecall instruction causes a requested trap to the execution environment. Misaligned loads and stores might not be supported. The fence.tso instruction is mandatory. NOTE: The fence.tso instruction was incorrectly described as optional in the 2019 ratified specifications. However, fence.tso is encoded within the standard fence encoding such that implementations must treat it as a simple global fence if they do not natively support TSO-ordering optimizations. As software can always assume without any penalty that fence.tso is being exploited by a hardware implementation, there is no advantage to making the instruction a profile option. Later versions of the unprivileged ISA specifications correctly indicate that fence.tso is mandatory.
REQ-EXT-M	M	~> 2.0	Integer multiply and divide	
REQ-EXT-S	S	~> 1.13	Supervisor mode	Supervisor version 1.13
REQ-EXT-Sha	Sha	~> 1.0	Augmented hypervisor	The set of augmented hypervisor extensions: H, Ssstateen, Shcounterenw, Shvstvala, Shtvala, Shvstvcd, Shvsatpa, Shgatpa
REQ-EXT-Sm	Sm	~> 1.13	Machine mode	
REQ-EXT-Smpmp	Smpmp	~> 1.13	Physical Memory Protection	
REQ-EXT-Ssccptr	Ssccptr	~> 1.0	Cacheable and coherent main memory page table reads	Main memory regions with both the cacheability and coherence PMAs must support hardware page-table reads
REQ-EXT-Sscofpmf	Sscofpmf	~> 1.0	Counter Overflow and Privilege Mode Filtering	Count overflow and mode-based filtering. Platforms may choose to mandate the presence of Sscofpmf.
REQ-EXT-Sscounterenw	Sscounterenw	~> 1.0	Support writeable enables for any supported counter	For any hpmcounter that is not read-only zero, the corresponding bit in scounteren must be writable.
REQ-EXT-Ssnpm	Ssnpm	~> 1.0	Pointer masking for next privilege level less than S-mode	Pointer masking, with senvcfg .PME supporting, at minimum, settings PMLen=0 and PMLen=7

Requirement ID	Extension	Version	Long Name	Note
REQ-EXT-Sstc	Sstc	~> 1.0	Supervisor-mode timer interrupts	Supervisor-mode timer interrupts. NOTE: Sstc was not made mandatory in RVB23S64 as it is a more disruptive change affecting system-level architecture, and will take longer for implementations to adopt. It is expected to be made mandatory in the next profile release.
REQ-EXT-Sstvala	Sstvala	~> 1.0	Supervisor Trap Value provides all needed values	stval must be written with the faulting virtual address for load, store, and instruction page-fault, access-fault, and misaligned exceptions, and for breakpoint exceptions other than those caused by execution of the EBREAK or C.EBREAK instructions. For virtual-instruction and illegal instruction exceptions, stval must be written with the faulting instruction .
REQ-EXT-Sstvecd	Sstvecd	~> 1.0	Direct exception vectoring	stvec .MODE must be capable of holding the value 0 (Direct). When stvec .MODE=Direct, stvec .BASE must be capable of holding any valid four-byte-aligned address
REQ-EXT-Ssu64xl	Ssu64xl	~> 1.0	64-bit UXLEN	sstatus .UXL must be capable of holding the value 2 (that is, UXLEN=64 must be supported)
REQ-EXT-Supm	Supm	~> 1.0	Pointer masking available in user mode	Pointer masking, with the execution environment providing a means to select PMLen=0 and PMLen=7 at minimum
REQ-EXT-Sv39	Sv39	~> 1.0	39-bit virtual address translation (3 level)	Page-Based 39-bit Virtual-Memory System
REQ-EXT-Svade	Svade	~> 1.0	Exception on PTE A/D Bits	A page-fault exception is raised when a page is accessed when A bit = 0 , or when a page is written when D bit = 0
REQ-EXT-Svbare	Svbare	~> 1.0	Bare virtual addressing	The satp mode Bare must be supported
REQ-EXT-Svinval	Svinval	~> 1.0	Fine-grained address-translation cache invalidation	Fine-grained address-translation cache invalidation
REQ-EXT-Svnapot	Svnapot	~> 1.0	Naturally Aligned Power-of-Two Translation Contiguity	NAPOT translation contiguity. Svnapot is very low cost to provide, so is made mandatory even in RVB.
REQ-EXT-Svpbmt	Svpbmt	~> 1.0	Page-based memory types	Page-based memory types
REQ-EXT-U	U	~> 2.0	User-mode privilege level	
REQ-EXT-V	V	~> 1.0	Vector Operations	The Vector extension
REQ-EXT-Za128rs	Za128rs	~> 1.0	Reservation set size of at most 128 bytes	Za128rs is a profile-defined extension introduced with RVA20. The minimum reservation set size is effectively determined by the size of atomic accesses in the A extension.
REQ-EXT-Za64rs	Za64rs	~> 1.0	Reservation set size of at most 64 bytes	Reservation sets are contiguous, naturally aligned, and a maximum of 64 bytes
REQ-EXT-Zawrs	Zawrs	~> 1.0	Wait-on-Reservation-Set Instructions	Wait-on-reservation-set (WRS) instructions
REQ-EXT-Zba	Zba	~> 1.0	Address generation	
REQ-EXT-Zbb	Zbb	~> 1.0	Basic bit-manipulation	
REQ-EXT-Zbs	Zbs	~> 1.0	Single-bit instructions	
REQ-EXT-Zcb	Zcb	~> 1.0	Simple code-size saving instructions	Additional compressed (16-bit) instructions
REQ-EXT-Zcmop	Zcmop	~> 1.0	Compressed May-Be-Operations	Compressed (16-bit) may-be operations
REQ-EXT-Zfa	Zfa	~> 1.0	Additional Floating-Point Instructions	Additional floating-point instructions
REQ-EXT-Zfhmin	Zfhmin	~> 1.0	Minimal half-precision floating-point	Zfhmin is a small extension that adds support to load/store and convert IEEE 754 half-precision numbers to and from the IEEE 754 single-precision format. The hardware cost for this extension is low, and mandating the extension avoids adding an option to the profile.

Requirement ID	Extension	Version	Long Name	Note
REQ-EXT-Zic64b	Zic64b	= 1.0	64-byte cache blocks	This is a new extension name for this feature. While the general RISC-V specifications are agnostic to cache block size, selecting a common cache block size simplifies the specification and use of the following cache-block extensions within the application processor profile. Software does not have to query a discovery mechanism and/or provide dynamic dispatch to the appropriate code. We choose 64 bytes at it is effectively an industry standard. Implementations may use longer cache blocks to reduce tag cost provided they use 64-byte sub-blocks to remain compatible. Implementations may use shorter cache blocks provided they sequence cache operations across the multiple cache blocks comprising a 64-byte block to remain compatible.
REQ-EXT-Zicbom	Zicbom	~> 1.0	Cache-block management instructions	
REQ-EXT-Zicbop	Zicbop	~> 1.0	Cache-block prefetch	As with other HINTS, the inclusion of prefetches in the mandatory set of extensions indicates that software should generate these instructions where they are expected to be useful, and hardware is expected to exploit that information.
REQ-EXT-Zicboz	Zicboz	~> 1.0	Cache-block zero instruction	
REQ-EXT-Ziccamao	Ziccama	~> 1.0	Main memory supports all atomics in A extension	Ziccama is a profile-defined extension introduced with RVA20.
REQ-EXT-Ziccif	Ziccif	~> 1.0	Main memory supports instruction fetch with atomicity requirement	Ziccif is a profile-defined extension introduced with RVA20. The fetch atomicity requirement facilitates runtime patching of aligned instructions.
REQ-EXT-Zicclsm	Zicclsm	~> 1.0	Main memory supports misaligned loads/stores	Zicclsm is a profile-defined extension introduced with RVA20. This requires misaligned support for all regular load and store instructions (including scalar and vector) but not AMOs or other specialized forms of memory access. Even though mandated, misaligned loads and stores might execute extremely slowly. Standard software distributions should assume their existence only for correctness, not for performance.
REQ-EXT-Ziccrse	Ziccrse	~> 1.0	Main memory supports forward progress on LR/SC sequences	Ziccrse is a profile-defined extension introduced with RVA20.
REQ-EXT-Zicntr	Zicntr	~> 2.0	Base Counters and Timers	
REQ-EXT-Zicond	Zicond	~> 1.0	Integer Conditional Operations	Integer conditional operations
REQ-EXT-Zicsr	Zicsr	~> 2.0	Control and status register instructions	
REQ-EXT-Zifencei	Zifencei	~> 1.0	Instruction fence	Instruction-Fetch fence instruction. Zifencei is mandated as it is the only standard way to support instruction-cache coherence in RVB23 application processors. A new instruction-cache coherence mechanism is under development (tentatively named Zjid), which might be added as an option in the future.
REQ-EXT-Zihintntl	Zihintntl	~> 1.0	Non-Temporal Locality Hints	Non-temporal memory-access locality hints
REQ-EXT-Zihintpause	Zihintpause	~> 2.0	Pause Hint	While the pause instruction is a HINT can be implemented as a NOP and hence trivially supported by hardware implementers, its inclusion in the mandatory extension list signifies that software should use the instruction whenever it would make sense and that implementers are expected to exploit this information to optimize hardware execution.
REQ-EXT-Zihpm	Zihpm	~> 2.0	Hardware Performance Counters	The number of counters is platform-specific.
REQ-EXT-Zimop	Zimop	~> 1.0	May-Be-Operations	May-be operations
REQ-EXT-Zkt	Zkt	~> 1.0	Data-independent execution latency	Zkt requires a certain subset of integer instructions execute with data-independent latency. Mandating this feature enables portable libraries for safe basic cryptographic operations. It is expected that application processors will naturally have this property and so implementation cost is low, if not zero, in most systems that would support RVA22.
REQ-EXT-Zvbb	Zvbb	~> 1.0	Vector Basic Bit-manipulation	Vector basic bit-manipulation instructions

Requirement ID	Extension	Version	Long Name	Note
REQ-EXT-Zvfhmin	Zvfhmin	~> 1.0	Vector Extension for Minimal Half-Precision Floating-Point	Vector minimal half-precision floating-point
REQ-EXT-Zvkt	Zvkt	~> 1.0	Vector Data-Independent Execution Latency	Vector data-independent execution latency

2.2. Optional Extensions

The AC200 certificate has 14 optional extensions.

Requirement ID	Extension	Version	Long Name	Note
REQ-EXT-Sdtrig	Sdtrig	~> 1.0	Debug triggers	Debug triggers
REQ-EXT-Sspm	Sspm	~> 1.0	Pointer masking available in supervisor mode	Supervisor-mode pointer masking, with the supervisor execution environment providing a means to select PMLen=0 and PMLen=7 (at minimum).
REQ-EXT-Ssstrict	Ssstrict	~> 1.0	Unimplemented reserved encodings trap and no non-conforming extensions	No non-conforming extensions are present. Attempts to execute unimplemented opcodes or access unimplemented CSRs in the standard or reserved encoding spaces raises an illegal instruction exception that results in a contained trap to the supervisor-mode trap handler NOTE: Ssstrict does not prescribe behavior for the custom encoding spaces or CSRs. NOTE: Ssstrict definition applies to the execution environment claiming to be RVB23-compatible, which must have the hypervisor extension. That execution environment will take a contained trap to supervisor-mode (however that trap is implemented, including, but not limited to, emulation/delegation in the outer execution environment). Ssstrict (and all the other RVB23 mandates and options) do not apply to any guest VMs run by a hypervisor. An RVB23 hypervisor can provide guest VMs that are also RVB23-compatible but with an expanded set of emulated standard instructions. An RVB23 hypervisor can also choose to implement guest VMs that are not RVB23 compatible (for example, only RVA20 or only RVA22)
REQ-EXT-Sv48	Sv48	~> 1.13	48-bit virtual address translation (4 level)	Page-based 48-bit virtual-memory system
REQ-EXT-Sv57	Sv57	~> 1.13	57-bit virtual address translation (5 level)	Page-based 57-bit virtual-memory system
REQ-EXT-Svadu	Svadu	~> 1.0	Hardware Updating of PTE A/D Bits	Hardware A/D bit updates
REQ-EXT-Svvptc	Svvptc	~> 1.0	Guarantee visibility of PTE transitions from invalid to valid	Transitions from invalid to valid PTEs will be visible in bounded time without an explicit memory-management fence.
REQ-EXT-Zca	Zca	~> 1.0	C instructions excluding floating-point loads/stores	
REQ-EXT-Zcd	Zcd	~> 1.0	Compressed double-precision floating-point loads/stores	
REQ-EXT-Zcf	Zcf	~> 1.0	Compressed single-precision floating-point loads/stores	
REQ-EXT-Zfh	Zfh	~> 1.0	Half-precision floating point	A future RVB profile might mandate V.
REQ-EXT-Zkn	Zkn	~> 1.0	NIST Algorithm Suite	Scalar crypto NIST algorithms
REQ-EXT-Zkr	Zkr	~> 1.0	Entropy Source	Entropy CSR NOTE: Technically, Zk is also a privileged-mode option, capturing that Zkr, Zkn, and Zkt are all implemented. However, the Zk rollup is less descriptive than specifying the individual extensions explicitly.
REQ-EXT-Zks	Zks	~> 1.0	ShangMi Algorithm Suite	Scalar crypto Shang-Mi algorithms

3. Implementation-dependencies

RISC-V standards support many implementation-defined parameters. In many cases, there are no names associated with these parameters. Names are defined in this section when not provided in the associated standard.

3.1. IN-SCOPE Parameters

These implementation-dependent options defined by MANDATORY or OPTIONAL extensions are IN-SCOPE. An implementation must abide by the "Allowed Value(s)" to obtain a certificate. If the "Allowed Value(s)" is "Any" then any value allowed by the type is acceptable.

The AC200 certificate has 1 IN-SCOPE parameters.

Parameter	Type	Allowed Value(s)	Extension(s)	Note
MXLEN	[32, 64]	64	U , S	

3.2. OUT-OF-SCOPE Parameters

These implementation-dependent options defined by MANDATORY or OPTIONAL extensions are OUT-OF-SCOPE. There are no restrictions on their values for certification purposes because the certificate doesn’t cover the behavior of the associated RISC-V standard as a function of these parameters.

The AC200 certificate has 71 OUT-OF-SCOPE parameters.

Parameters	Type	Extension(s)
ASID_WIDTH	0 to 16	
CACHE_BLOCK_SIZE	1 to 0xfffffffffffffff	
COUNTINHIBIT_EN	32-element array where: [0] is boolean [1] is false [2] is boolean additional items are: boolean	
DBG_HCONTEXT_WIDTH	0 to 14	
DBG_SCONTEXT_WIDTH	0 to 32	
DCSR_MPRVEN_TYPE	[read-only-0, read-only-1, rw]	
DCSR_STEPIE_TYPE	[read-only-0, read-only-1, rw]	
DCSR_STOPCOUNT_TYPE	[read-only-0, read-only-1, rw]	
DCSR_STOPTIME_TYPE	[read-only-0, read-only-1, rw]	
FORCE_UPGRADE_CBO_INVAL_TO_FLUSH	boolean	
HCONTEXT_AVAILABLE	boolean	
MARCHID_IMPLEMENTED	boolean	
MCONTEXT_AVAILABLE	boolean	
MCOUNTENABLE_EN	32-element array of boolean	
MIMPID_IMPLEMENTED	boolean	
MISALIGNED_LDST	boolean	
MISALIGNED_LDST_EXCEPTION_PRIORITY	[low, high]	
MISA_CSR_IMPLEMENTED	boolean	
MSTATUS_TVM_IMPLEMENTED	boolean	
MTVAL_WIDTH	0 to 64	U , S
MTVEC_ACCESS	[ro, rw]	
MTVEC_ILLEGAL_WRITE_BEHAVIOR	[retain, custom]	
MTVEC_MODES	1-element to 2-element array of [0, 1]	
M_MODE_ENDIANNES	[little, big, dynamic]	
NUM_PMP_ENTRIES	0 to 64	
PHYS_ADDR_WIDTH	1 to 64	U , S
PMA_GRANULARITY	2 to 66	
PMLEN	integer	

Parameters	Type	Extension(s)
PMP_GRANULARITY	2 to 66	
PRECISE_SYNCHRONOUS_EXCEPTIONS	boolean	
REPORT_ENCODING_IN_MTVAL_ON_ILLEGAL_INSTRUCTION	boolean	
REPORT_ENCODING_IN_STVAL_ON_ILLEGAL_INSTRUCTION	boolean	
REPORT_VA_IN_MTVAL_ON_BREAKPOINT	boolean	
REPORT_VA_IN_MTVAL_ON_INSTRUCTION_ACCESS_FAULT	boolean	
REPORT_VA_IN_MTVAL_ON_INSTRUCTION_MISALIGNED	boolean	
REPORT_VA_IN_MTVAL_ON_INSTRUCTION_PAGE_FAULT	boolean	
REPORT_VA_IN_MTVAL_ON_LOAD_ACCESS_FAULT	boolean	
REPORT_VA_IN_MTVAL_ON_LOAD_MISALIGNED	boolean	
REPORT_VA_IN_MTVAL_ON_LOAD_PAGE_FAULT	boolean	
REPORT_VA_IN_MTVAL_ON_STORE_AMO_ACCESS_FAULT	boolean	
REPORT_VA_IN_MTVAL_ON_STORE_AMO_MISALIGNED	boolean	
REPORT_VA_IN_MTVAL_ON_STORE_AMO_PAGE_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_BREAKPOINT	boolean	
REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED	boolean	
REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED	boolean	
REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT	boolean	
REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED	boolean	
REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT	boolean	
SATP_MODE_BARE	boolean	
STVAL_WIDTH	≤ 0xfffffffffffffff	
STVEC_MODE_DIRECT	boolean	
STVEC_MODE_VECTORED	boolean	
SXLEN	1-element to 2-element array of [32, 64]	U , S
S_MODE_ENDIANNES	[little, big, dynamic]	
TIME_CSR_IMPLEMENTED	boolean	
TRAP_ON_EBREAK	boolean	
TRAP_ON_ECALL_FROM_M	boolean	
TRAP_ON_ECALL_FROM_S	boolean	
TRAP_ON_ECALL_FROM_U	boolean	
TRAP_ON_ILLEGAL_WLRL	boolean	
TRAP_ON_RESERVED_INSTRUCTION	boolean	
TRAP_ON_UNIMPLEMENTED_CSR	boolean	
TRAP_ON_UNIMPLEMENTED_INSTRUCTION	boolean	
UXLEN	1-element to 2-element array of [32, 64]	U , S
U_MODE_ENDIANNES	[little, big, dynamic]	
VENDOR_ID_BANK	25-bit integer	
VENDOR_ID_OFFSET	7-bit integer	

4. Instruction Summary

The AC200 certificate has up to 255 instructions (exact number depends on an implementation’s options).

Name	Long Name
add	Integer add

Name	Long Name
addi	Add immediate
and	And
andi	And immediate
andn	AND with inverted operand
auipc	Add upper immediate to pc
bclr	Single-Bit clear (Register)
bclri	Single-Bit clear (Immediate)
beq	Branch if equal
bext	Single-Bit extract (Register)
bexti	Single-Bit extract (Immediate)
bge	Branch if greater than or equal
bgeu	Branch if greater than or equal unsigned
binv	Single-Bit invert (Register)
binvi	Single-Bit invert (Immediate)
blt	Branch if less than
bltu	Branch if less than unsigned
bne	Branch if not equal
bset	Single-Bit set (Register)
bseti	Single-Bit set (Immediate)
c.add	Add
c.addi	Add a sign-extended non-zero immediate
c.addi16sp	Add a sign-extended non-zero immediate
c.addi4spn	Add a zero-extended non-zero immediate, scaled by 4, to the stack pointer
c.and	And
c.andi	And immediate
c.beqz	Branch if Equal Zero
c.bnez	Branch if NOT Equal Zero
c.ebreak	Breakpoint exception
c.fld	Load double-precision
c.fldsp	Load doubleword into floating-point register from stack
c.flw	Load single-precision
c.flwsp	Load word into floating-point register from stack
c.fsd	Store double-precision
c.fsdsp	Store double-precision value to stack
c.fsw	Store single-precision
c.fswsp	Store single-precision value to stack
c.j	Jump
c.jalr	Jump and Link Register
c.jr	Jump Register
c.lbu	Load unsigned byte, 16-bit encoding
c.lh	Load signed halfword, 16-bit encoding
c.lhu	Load unsigned halfword, 16-bit encoding
c.li	Load the sign-extended 6-bit immediate
c.lui	Load Upper Immediate
c.lw	Load word
c.lwsp	Load word from stack pointer
c.mop.n	Compressed May-Be-Operation
c.mv	Move Register
c.nop	Non-operation

Name	Long Name
c.not	Bitwise not, 16-bit encoding
c.or	Or
c.sb	Store unsigned byte, 16-bit encoding
c.sh	Store unsigned halfword, 16-bit encoding
c.slli	Shift left logical immediate
c.srai	Shift right arithmetical immediate
c.srli	Shift right logical immediate
c.sub	Subtract
c.sw	Store word
c.swsp	Store word to stack
c.xor	Exclusive Or
cbo.clean	Cache Block Clean
cbo.flush	Cache Block Flush
cbo.inval	Cache Block Invalidate
cbo.zero	Cache Block Zero
clz	Count leading zero bits
cpop	Count set bits
csrrc	Atomic Read and Clear Bits in CSR
csrrci	Atomic Read and Clear Bits in CSR with Immediate
csrrs	Atomic Read and Set Bits in CSR
csrrsi	Atomic Read and Set Bits in CSR with Immediate
csrrw	Atomic Read/Write CSR
csrrwi	Atomic Read/Write CSR Immediate
ctz	Count trailing zero bits
czero.eqz	Conditional zero, if condition is equal to zero
czero.nez	Conditional zero, if condition is nonzero
div	Signed division
divu	Unsigned division
ebreak	Breakpoint exception
ecall	Environment call
fadd.d	Floating-Point Add Double-Precision
fadd.h	No synopsis available
fadd.s	Floating-Point Add Single-Precision
fclass.d	Floating-Point Classify Double-Precision
fclass.h	No synopsis available
fclass.s	Floating-Point Classify Single-Precision
fcvt.d.s	Floating-Point Convert Single-Precision to Double-Precision
fcvt.d.w	Floating-Point Convert Word to Double-Precision
fcvt.d.wu	Floating-Point Convert Unsigned Word to Double-Precision
fcvt.h.s	Convert half-precision float to a single-precision float
fcvt.h.w	Floating-point Convert Word to Half-precision
fcvt.h.wu	Floating-point Convert Unsigned Word to Half-precision
fcvt.s.d	Floating-Point Convert Double-Precision to Single-Precision
fcvt.s.h	Convert single-precision float to a half-precision float
fcvt.s.w	Floating-Point Convert Word to Single-Precision
fcvt.s.wu	Floating-Point Convert Unsigned Word to Single-Precision
fcvt.w.d	Floating-Point Convert Double-Precision to Word
fcvt.w.h	Floating-point Convert Half-precision to Word
fcvt.w.s	Floating-Point Convert Single-Precision to Word

Name	Long Name
fcvt.wu.d	Floating-Point Convert Double-Precision to Unsigned Word
fcvt.wu.h	Floating-point Convert Half-precision to Word
fcvt.wu.s	Floating-Point Convert Single-Precision to Unsigned Word
fdiv.d	Floating-Point Divide Double-Precision
fdiv.h	No synopsis available
fdiv.s	Floating-Point Divide Single-Precision
fence	Memory ordering fence
fence.i	Instruction fence
fence.tso	Memory ordering fence, total store ordering
feq.d	Floating-Point Equal Double-Precision
feq.h	No synopsis available
feq.s	Floating-Point Equal Single-Precision
fld	Floating-Point Load Double-Precision
fle.d	Floating-Point Less Than or Equal Double-Precision
fle.h	No synopsis available
fle.s	Floating-Point Less Than or Equal Single-Precision
fleq.s	Floating-Point Less Than or Equal Quiet Single-Precision
flh	Half-precision floating-point load
fli.s	No synopsis available
flt.d	Floating-Point Less Than Double-Precision
flt.h	No synopsis available
flt.s	Floating-Point Less Than Single-Precision
fltq.s	Floating-Point Less Than Quiet Single-Precision
flw	Floating-Point Load Single-Precision
fmadd.d	Floating-Point Multiply-Add Double-Precision
fmadd.h	No synopsis available
fmadd.s	Floating-Point Multiply-Add Single-Precision
fmax.d	Floating-Point Maximum-Number Double-Precision
fmax.h	No synopsis available
fmax.s	Floating-Point Maximum-Number Single-Precision
fmaxm.s	No synopsis available
fmin.d	Floating-Point Minimum-Number Double-Precision
fmin.h	No synopsis available
fmin.s	Floating-Point Minimum-Number Single-Precision
fminm.s	No synopsis available
fmsub.d	Floating-Point Multiply-Subtract Double-Precision
fmsub.h	No synopsis available
fmsub.s	Floating-Point Multiply-Subtract Single-Precision
fmul.d	Floating-Point Multiply Double-Precision
fmul.h	No synopsis available
fmul.s	Floating-Point Multiply Single-Precision
fmv.h.x	Half-precision floating-point move from integer
fmv.w.x	Floating-Point Move Single-Precision Word from Integer Register
fmv.x.h	Move half-precision value from floating-point to integer register
fmv.x.w	Floating-Point Move Single-Precision Word to Integer Register
fnmadd.d	Floating-Point Negate-Multiply-Add Double-Precision
fnmadd.h	No synopsis available
fnmadd.s	Floating-Point Negate-Multiply-Add Single-Precision
fnmsub.d	Floating-Point Negate-Multiply-Subtract Double-Precision

Name	Long Name
fnmsub.h	No synopsis available
fnmsub.s	Floating-Point Negate-Multiply-Subtract Single-Precision
fround.s	Floating-point round single-precision float to integer
froundnx.s	Floating-point Round Single-precision to Integer with Inexact
fsd	Floating-Point Store Double-Precision
fsgnj.d	Floating-Point Sign-Inject Double-Precision
fsgnj.h	No synopsis available
fsgnj.s	Floating-Point Sign-Inject Single-Precision
fsgnjn.d	Floating-Point Sign-Inject Negate Double-Precision
fsgnjn.h	No synopsis available
fsgnjn.s	Floating-Point Sign-Inject Negate Single-Precision
fsgnjx.d	Floating-Point Sign-Inject XOR Double-Precision
fsgnjx.h	No synopsis available
fsgnjx.s	Floating-Point Sign-Inject XOR Single-Precision
fsh	Half-precision floating-point store
fsqrt.d	Floating-Point Square Root Double-Precision
fsqrt.h	No synopsis available
fsqrt.s	Floating-Point Square Root Single-Precision
fsub.d	Floating-Point Subtract Double-Precision
fsub.h	No synopsis available
fsub.s	Floating-Point Subtract Single-Precision
fsw	Floating-Point Store Single-Precision
jal	Jump and link
jalr	Jump and link register
lb	Load byte
lbu	Load byte unsigned
ld	Load doubleword
lh	Load halfword
lhu	Load halfword unsigned
lui	Load upper immediate
lw	Load word
max	Maximum
maxu	Unsigned maximum
min	Minimum
minu	Unsigned minimum
mop.r.n	May-be-operation (1 source register)
mop.rr.n	May-be-operation (2 source registers)
mret	Machine-mode Return from Trap
mul	Signed multiply
mulh	Signed multiply high
mulhsu	Signed/unsigned multiply high
mulhu	Unsigned multiply high
ntl.all	Non-temporal locality hint, all
ntl.p1	Non-temporal locality hint, innermost private
ntl.pall	Non-temporal locality hint, all private
ntl.s1	Non-temporal locality hint, innermost shared
or	Or
orc.b	Bitware OR-combine, byte granule
ori	Or immediate

Name	Long Name
orn	OR with inverted operand
pause	Pause hint
prefetch.i	Cache block prefetch for instruction fetch
prefetch.r	Cache block prefetch for data read
prefetch.w	Cache block prefetch for data write
rem	Signed remainder
remu	Unsigned remainder
rev8	Byte-reverse register (RV64 encoding)
rol	Rotate left (Register)
ror	Rotate right (Register)
rori	Rotate right (Immediate)
sb	Store byte
sd	Store doubleword
sext.b	Sign-extend byte
sext.h	Sign-extend halfword
sfence.inval.ir	Order implicit page table reads after invalidation
sfence.vma	Supervisor memory-management fence
sfence.w.inval	Order writes before sfence
sh	Store halfword
sh1add	Shift left by 1 and add
sh2add	Shift left by 2 and add
sh3add	Shift left by 3 and add
sinval.vma	Invalidate cached address translations
sll	Shift left logical
slli	Shift left logical immediate
slt	Set on less than
slti	Set on less than immediate
sltiu	Set on less than immediate unsigned
sltu	Set on less than unsigned
sra	Shift right arithmetic
srai	Shift right arithmetic immediate
sret	Supervisor Mode Return from Trap
srl	Shift right logical
srli	Shift right logical immediate
sub	Subtract
sw	Store word
vandn.vv	No synopsis available
vandn.vx	No synopsis available
vbrev.v	No synopsis available
vbrev8.v	No synopsis available
vclz.v	No synopsis available
vcpop.v	No synopsis available
vctz.v	No synopsis available
vrev8.v	No synopsis available
vrol.vv	No synopsis available
vrol.vx	No synopsis available
vror.vi	No synopsis available
vror.vv	No synopsis available
vror.vx	No synopsis available

Name	Long Name
vwsll.vi	No synopsis available
vwsll.vv	No synopsis available
vwsll.vx	No synopsis available
wfi	Wait for interrupt
wrs.nton	Wait-on-Reservation-Set-with-No-Timeout
wrs.sto	Wait-on-Reservation-Set-with-Short-Timeout
xnor	Exclusive NOR
xor	Exclusive Or
xori	Exclusive Or immediate

5. CSR Summary

The AC200 certificate has up to 140 CSRs (exact number depends on an implementation’s options).

5.1. By Name

Name	Long Name	Address	Mode	Defining Extension(s)
cycle	Cycle counter for RDCYCLE Instruction	0xc00	U	Zicntr any
fcsr	Floating-point control and status register (frm + fflags)	0x3	U	F any
fflags	Floating-Point Accrued Exceptions	0x1	U	F any
frm	Floating-Point Dynamic Rounding Mode	0x2	U	F any
hpmcounter10	User-mode Hardware Performance Counter 7	0xc0a	U	Zihpm any
hpmcounter11	User-mode Hardware Performance Counter 8	0xc0b	U	Zihpm any
hpmcounter12	User-mode Hardware Performance Counter 9	0xc0c	U	Zihpm any
hpmcounter13	User-mode Hardware Performance Counter 10	0xc0d	U	Zihpm any
hpmcounter14	User-mode Hardware Performance Counter 11	0xc0e	U	Zihpm any
hpmcounter15	User-mode Hardware Performance Counter 12	0xc0f	U	Zihpm any
hpmcounter16	User-mode Hardware Performance Counter 13	0xc10	U	Zihpm any
hpmcounter17	User-mode Hardware Performance Counter 14	0xc11	U	Zihpm any
hpmcounter18	User-mode Hardware Performance Counter 15	0xc12	U	Zihpm any
hpmcounter19	User-mode Hardware Performance Counter 16	0xc13	U	Zihpm any
hpmcounter20	User-mode Hardware Performance Counter 17	0xc14	U	Zihpm any
hpmcounter21	User-mode Hardware Performance Counter 18	0xc15	U	Zihpm any
hpmcounter22	User-mode Hardware Performance Counter 19	0xc16	U	Zihpm any
hpmcounter23	User-mode Hardware Performance Counter 20	0xc17	U	Zihpm any
hpmcounter24	User-mode Hardware Performance Counter 21	0xc18	U	Zihpm any
hpmcounter25	User-mode Hardware Performance Counter 22	0xc19	U	Zihpm any
hpmcounter26	User-mode Hardware Performance Counter 23	0xc1a	U	Zihpm any
hpmcounter27	User-mode Hardware Performance Counter 24	0xc1b	U	Zihpm any
hpmcounter28	User-mode Hardware Performance Counter 25	0xc1c	U	Zihpm any
hpmcounter29	User-mode Hardware Performance Counter 26	0xc1d	U	Zihpm any
hpmcounter3	User-mode Hardware Performance Counter 0	0xc03	U	Zihpm any
hpmcounter30	User-mode Hardware Performance Counter 27	0xc1e	U	Zihpm any
hpmcounter31	User-mode Hardware Performance Counter 28	0xc1f	U	Zihpm any
hpmcounter4	User-mode Hardware Performance Counter 1	0xc04	U	Zihpm any
hpmcounter5	User-mode Hardware Performance Counter 2	0xc05	U	Zihpm any
hpmcounter6	User-mode Hardware Performance Counter 3	0xc06	U	Zihpm any
hpmcounter7	User-mode Hardware Performance Counter 4	0xc07	U	Zihpm any
hpmcounter8	User-mode Hardware Performance Counter 5	0xc08	U	Zihpm any
hpmcounter9	User-mode Hardware Performance Counter 6	0xc09	U	Zihpm any
instret	Instructions retired counter for RDINSTRET Instruction	0xc02	U	Zicntr any

Name	Long Name	Address	Mode	Defining Extension(s)
marchid	Machine Architecture ID	0xf12	M	Sm any
mcause	Machine Cause	0x342	M	Sm any
mcontext	Machine Context	0x7a8	M	Sdtrig any
mcounteren	Machine Counter Enable	0x306	M	U any
mcountinhibit	Machine Counter Inhibit	0x320	M	Sm any
mcycle	Machine Cycle Counter	0xb00	M	Sm any
medeleg	Machine Exception Delegation	0x302	M	S any
mepc	Machine Exception Program Counter	0x341	M	Sm any
mhartid	Machine Hart ID	0xf14	M	Sm any
mie	Machine Interrupt Enable	0x304	M	Sm any
mimpid	Machine Implementation ID	0xf13	M	Sm any
minstret	Machine Instructions Retired Counter	0xb02	M	Sm any
mip	Machine Interrupt Pending	0x344	M	Sm any
misa	Machine ISA Control	0x301	M	Sm any
mscratch	Machine Scratch Register	0x340	M	Sm any
mstatus	Machine Status	0x300	M	Sm any
mtval	Machine Trap Value	0x343	M	Sm any
mtvec	Machine Trap Vector Control	0x305	M	Sm any
mvendorid	Machine Vendor ID	0xf11	M	Sm any
pmpaddr0	PMP Address 0	0x3b0	M	Smpmp any
pmpaddr1	PMP Address 1	0x3b1	M	Smpmp any
pmpaddr10	PMP Address 10	0x3ba	M	Smpmp any
pmpaddr11	PMP Address 11	0x3bb	M	Smpmp any
pmpaddr12	PMP Address 12	0x3bc	M	Smpmp any
pmpaddr13	PMP Address 13	0x3bd	M	Smpmp any
pmpaddr14	PMP Address 14	0x3be	M	Smpmp any
pmpaddr15	PMP Address 15	0x3bf	M	Smpmp any
pmpaddr16	PMP Address 16	0x3c0	M	Smpmp any
pmpaddr17	PMP Address 17	0x3c1	M	Smpmp any
pmpaddr18	PMP Address 18	0x3c2	M	Smpmp any
pmpaddr19	PMP Address 19	0x3c3	M	Smpmp any
pmpaddr2	PMP Address 2	0x3b2	M	Smpmp any
pmpaddr20	PMP Address 20	0x3c4	M	Smpmp any
pmpaddr21	PMP Address 21	0x3c5	M	Smpmp any
pmpaddr22	PMP Address 22	0x3c6	M	Smpmp any
pmpaddr23	PMP Address 23	0x3c7	M	Smpmp any
pmpaddr24	PMP Address 24	0x3c8	M	Smpmp any
pmpaddr25	PMP Address 25	0x3c9	M	Smpmp any
pmpaddr26	PMP Address 26	0x3ca	M	Smpmp any
pmpaddr27	PMP Address 27	0x3cb	M	Smpmp any
pmpaddr28	PMP Address 28	0x3cc	M	Smpmp any
pmpaddr29	PMP Address 29	0x3cd	M	Smpmp any
pmpaddr3	PMP Address 3	0x3b3	M	Smpmp any
pmpaddr30	PMP Address 30	0x3ce	M	Smpmp any
pmpaddr31	PMP Address 31	0x3cf	M	Smpmp any
pmpaddr32	PMP Address 32	0x3d0	M	Smpmp any
pmpaddr33	PMP Address 33	0x3d1	M	Smpmp any
pmpaddr34	PMP Address 34	0x3d2	M	Smpmp any
pmpaddr35	PMP Address 35	0x3d3	M	Smpmp any

Name	Long Name	Address	Mode	Defining Extension(s)
pmpaddr36	PMP Address 36	0x3d4	M	Smpmp any
pmpaddr37	PMP Address 37	0x3d5	M	Smpmp any
pmpaddr38	PMP Address 38	0x3d6	M	Smpmp any
pmpaddr39	PMP Address 39	0x3d7	M	Smpmp any
pmpaddr4	PMP Address 4	0x3b4	M	Smpmp any
pmpaddr40	PMP Address 40	0x3d8	M	Smpmp any
pmpaddr41	PMP Address 41	0x3d9	M	Smpmp any
pmpaddr42	PMP Address 42	0x3da	M	Smpmp any
pmpaddr43	PMP Address 43	0x3db	M	Smpmp any
pmpaddr44	PMP Address 44	0x3dc	M	Smpmp any
pmpaddr45	PMP Address 45	0x3dd	M	Smpmp any
pmpaddr46	PMP Address 46	0x3de	M	Smpmp any
pmpaddr47	PMP Address 47	0x3df	M	Smpmp any
pmpaddr48	PMP Address 48	0x3e0	M	Smpmp any
pmpaddr49	PMP Address 49	0x3e1	M	Smpmp any
pmpaddr5	PMP Address 5	0x3b5	M	Smpmp any
pmpaddr50	PMP Address 50	0x3e2	M	Smpmp any
pmpaddr51	PMP Address 51	0x3e3	M	Smpmp any
pmpaddr52	PMP Address 52	0x3e4	M	Smpmp any
pmpaddr53	PMP Address 53	0x3e5	M	Smpmp any
pmpaddr54	PMP Address 54	0x3e6	M	Smpmp any
pmpaddr55	PMP Address 55	0x3e7	M	Smpmp any
pmpaddr56	PMP Address 56	0x3e8	M	Smpmp any
pmpaddr57	PMP Address 57	0x3e9	M	Smpmp any
pmpaddr58	PMP Address 58	0x3ea	M	Smpmp any
pmpaddr59	PMP Address 59	0x3eb	M	Smpmp any
pmpaddr6	PMP Address 6	0x3b6	M	Smpmp any
pmpaddr60	PMP Address 60	0x3ec	M	Smpmp any
pmpaddr61	PMP Address 61	0x3ed	M	Smpmp any
pmpaddr62	PMP Address 62	0x3ee	M	Smpmp any
pmpaddr63	PMP Address 63	0x3ef	M	Smpmp any
pmpaddr7	PMP Address 7	0x3b7	M	Smpmp any
pmpaddr8	PMP Address 8	0x3b8	M	Smpmp any
pmpaddr9	PMP Address 9	0x3b9	M	Smpmp any
pmpcfg0	PMP Configuration Register 0	0x3a0	M	Smpmp any
pmpcfg10	PMP Configuration Register 10	0x3aa	M	Smpmp any
pmpcfg12	PMP Configuration Register 12	0x3ac	M	Smpmp any
pmpcfg14	PMP Configuration Register 14	0x3ae	M	Smpmp any
pmpcfg2	PMP Configuration Register 2	0x3a2	M	Smpmp any
pmpcfg4	PMP Configuration Register 4	0x3a4	M	Smpmp any
pmpcfg6	PMP Configuration Register 6	0x3a6	M	Smpmp any
pmpcfg8	PMP Configuration Register 8	0x3a8	M	Smpmp any
satp	Supervisor Address Translation and Protection	0x180	S	S any
scause	Supervisor Cause	0x142	S	S any
scounteren	Supervisor Counter Enable	0x106	S	S any
scountovf	Supervisor Count Overflow	0xda0	S	Sscofpmf any
sepc	Supervisor Exception Program Counter	0x141	S	S any
sip	Supervisor Interrupt Pending	0x144	S	S any
sscratch	Supervisor Scratch Register	0x140	S	S any

Name	Long Name	Address	Mode	Defining Extension(s)
sstatus	Supervisor Status	0x100	S	S any
stval	Supervisor Trap Value	0x143	S	S any
stvec	Supervisor Trap Vector	0x105	S	S any
tdata1	Trigger Data 1	0x7a1	M	Sdtrig any
tdata2	Trigger Data 2	0x7a2	M	Sdtrig any
tdata3	Trigger Data 3	0x7a3	M	Sdtrig any
time	Timer for RDTIME Instruction	0xc01	U	Zicntr any
tselect	Trigger Select	0x7a0	M	Sdtrig any

5.2. By Address

Address	Mode	Name	Long Name	Primary Extension
0x1	U	fflags	Floating-Point Accrued Exceptions	F any
0x2	U	frm	Floating-Point Dynamic Rounding Mode	F any
0x3	U	fcsr	Floating-point control and status register (frm + fflags)	F any
0x100	S	sstatus	Supervisor Status	S any
0x105	S	stvec	Supervisor Trap Vector	S any
0x106	S	scounteren	Supervisor Counter Enable	S any
0x140	S	sscratch	Supervisor Scratch Register	S any
0x141	S	sepc	Supervisor Exception Program Counter	S any
0x142	S	scause	Supervisor Cause	S any
0x143	S	stval	Supervisor Trap Value	S any
0x144	S	sip	Supervisor Interrupt Pending	S any
0x180	S	satp	Supervisor Address Translation and Protection	S any
0x300	M	mstatus	Machine Status	Sm any
0x301	M	misa	Machine ISA Control	Sm any
0x302	M	medeleg	Machine Exception Delegation	S any
0x304	M	mie	Machine Interrupt Enable	Sm any
0x305	M	mtvec	Machine Trap Vector Control	Sm any
0x306	M	mcounteren	Machine Counter Enable	U any
0x320	M	mcountinhibit	Machine Counter Inhibit	Sm any
0x340	M	mscratch	Machine Scratch Register	Sm any
0x341	M	mepc	Machine Exception Program Counter	Sm any
0x342	M	mcause	Machine Cause	Sm any
0x343	M	mtval	Machine Trap Value	Sm any
0x344	M	mip	Machine Interrupt Pending	Sm any
0x3a0	M	pmpcfg0	PMP Configuration Register 0	Smpmp any
0x3a2	M	pmpcfg2	PMP Configuration Register 2	Smpmp any
0x3a4	M	pmpcfg4	PMP Configuration Register 4	Smpmp any
0x3a6	M	pmpcfg6	PMP Configuration Register 6	Smpmp any
0x3a8	M	pmpcfg8	PMP Configuration Register 8	Smpmp any
0x3aa	M	pmpcfg10	PMP Configuration Register 10	Smpmp any
0x3ac	M	pmpcfg12	PMP Configuration Register 12	Smpmp any
0x3ae	M	pmpcfg14	PMP Configuration Register 14	Smpmp any
0x3b0	M	pmpaddr0	PMP Address 0	Smpmp any
0x3b1	M	pmpaddr1	PMP Address 1	Smpmp any
0x3b2	M	pmpaddr2	PMP Address 2	Smpmp any
0x3b3	M	pmpaddr3	PMP Address 3	Smpmp any
0x3b4	M	pmpaddr4	PMP Address 4	Smpmp any
0x3b5	M	pmpaddr5	PMP Address 5	Smpmp any

Address	Mode	Name	Long Name	Primary Extension
0x3b6	M	pmpaddr6	PMP Address 6	Smpmp any
0x3b7	M	pmpaddr7	PMP Address 7	Smpmp any
0x3b8	M	pmpaddr8	PMP Address 8	Smpmp any
0x3b9	M	pmpaddr9	PMP Address 9	Smpmp any
0x3ba	M	pmpaddr10	PMP Address 10	Smpmp any
0x3bb	M	pmpaddr11	PMP Address 11	Smpmp any
0x3bc	M	pmpaddr12	PMP Address 12	Smpmp any
0x3bd	M	pmpaddr13	PMP Address 13	Smpmp any
0x3be	M	pmpaddr14	PMP Address 14	Smpmp any
0x3bf	M	pmpaddr15	PMP Address 15	Smpmp any
0x3c0	M	pmpaddr16	PMP Address 16	Smpmp any
0x3c1	M	pmpaddr17	PMP Address 17	Smpmp any
0x3c2	M	pmpaddr18	PMP Address 18	Smpmp any
0x3c3	M	pmpaddr19	PMP Address 19	Smpmp any
0x3c4	M	pmpaddr20	PMP Address 20	Smpmp any
0x3c5	M	pmpaddr21	PMP Address 21	Smpmp any
0x3c6	M	pmpaddr22	PMP Address 22	Smpmp any
0x3c7	M	pmpaddr23	PMP Address 23	Smpmp any
0x3c8	M	pmpaddr24	PMP Address 24	Smpmp any
0x3c9	M	pmpaddr25	PMP Address 25	Smpmp any
0x3ca	M	pmpaddr26	PMP Address 26	Smpmp any
0x3cb	M	pmpaddr27	PMP Address 27	Smpmp any
0x3cc	M	pmpaddr28	PMP Address 28	Smpmp any
0x3cd	M	pmpaddr29	PMP Address 29	Smpmp any
0x3ce	M	pmpaddr30	PMP Address 30	Smpmp any
0x3cf	M	pmpaddr31	PMP Address 31	Smpmp any
0x3d0	M	pmpaddr32	PMP Address 32	Smpmp any
0x3d1	M	pmpaddr33	PMP Address 33	Smpmp any
0x3d2	M	pmpaddr34	PMP Address 34	Smpmp any
0x3d3	M	pmpaddr35	PMP Address 35	Smpmp any
0x3d4	M	pmpaddr36	PMP Address 36	Smpmp any
0x3d5	M	pmpaddr37	PMP Address 37	Smpmp any
0x3d6	M	pmpaddr38	PMP Address 38	Smpmp any
0x3d7	M	pmpaddr39	PMP Address 39	Smpmp any
0x3d8	M	pmpaddr40	PMP Address 40	Smpmp any
0x3d9	M	pmpaddr41	PMP Address 41	Smpmp any
0x3da	M	pmpaddr42	PMP Address 42	Smpmp any
0x3db	M	pmpaddr43	PMP Address 43	Smpmp any
0x3dc	M	pmpaddr44	PMP Address 44	Smpmp any
0x3dd	M	pmpaddr45	PMP Address 45	Smpmp any
0x3de	M	pmpaddr46	PMP Address 46	Smpmp any
0x3df	M	pmpaddr47	PMP Address 47	Smpmp any
0x3e0	M	pmpaddr48	PMP Address 48	Smpmp any
0x3e1	M	pmpaddr49	PMP Address 49	Smpmp any
0x3e2	M	pmpaddr50	PMP Address 50	Smpmp any
0x3e3	M	pmpaddr51	PMP Address 51	Smpmp any
0x3e4	M	pmpaddr52	PMP Address 52	Smpmp any
0x3e5	M	pmpaddr53	PMP Address 53	Smpmp any
0x3e6	M	pmpaddr54	PMP Address 54	Smpmp any

Address	Mode	Name	Long Name	Primary Extension
0x3e7	M	pmpaddr55	PMP Address 55	Smpmp any
0x3e8	M	pmpaddr56	PMP Address 56	Smpmp any
0x3e9	M	pmpaddr57	PMP Address 57	Smpmp any
0x3ea	M	pmpaddr58	PMP Address 58	Smpmp any
0x3eb	M	pmpaddr59	PMP Address 59	Smpmp any
0x3ec	M	pmpaddr60	PMP Address 60	Smpmp any
0x3ed	M	pmpaddr61	PMP Address 61	Smpmp any
0x3ee	M	pmpaddr62	PMP Address 62	Smpmp any
0x3ef	M	pmpaddr63	PMP Address 63	Smpmp any
0x7a0	M	tselect	Trigger Select	Sdtrig any
0x7a1	M	tdata1	Trigger Data 1	Sdtrig any
0x7a2	M	tdata2	Trigger Data 2	Sdtrig any
0x7a3	M	tdata3	Trigger Data 3	Sdtrig any
0x7a8	M	mcontext	Machine Context	Sdtrig any
0xb00	M	mcycle	Machine Cycle Counter	Sm any
0xb02	M	minstret	Machine Instructions Retired Counter	Sm any
0xc00	U	cycle	Cycle counter for RDCYCLE Instruction	Zicntr any
0xc01	U	time	Timer for RDTIME Instruction	Zicntr any
0xc02	U	instret	Instructions retired counter for RDINSTRET Instruction	Zicntr any
0xc03	U	hpmcounter3	User-mode Hardware Performance Counter 0	Zihpm any
0xc04	U	hpmcounter4	User-mode Hardware Performance Counter 1	Zihpm any
0xc05	U	hpmcounter5	User-mode Hardware Performance Counter 2	Zihpm any
0xc06	U	hpmcounter6	User-mode Hardware Performance Counter 3	Zihpm any
0xc07	U	hpmcounter7	User-mode Hardware Performance Counter 4	Zihpm any
0xc08	U	hpmcounter8	User-mode Hardware Performance Counter 5	Zihpm any
0xc09	U	hpmcounter9	User-mode Hardware Performance Counter 6	Zihpm any
0xc0a	U	hpmcounter10	User-mode Hardware Performance Counter 7	Zihpm any
0xc0b	U	hpmcounter11	User-mode Hardware Performance Counter 8	Zihpm any
0xc0c	U	hpmcounter12	User-mode Hardware Performance Counter 9	Zihpm any
0xc0d	U	hpmcounter13	User-mode Hardware Performance Counter 10	Zihpm any
0xc0e	U	hpmcounter14	User-mode Hardware Performance Counter 11	Zihpm any
0xc0f	U	hpmcounter15	User-mode Hardware Performance Counter 12	Zihpm any
0xc10	U	hpmcounter16	User-mode Hardware Performance Counter 13	Zihpm any
0xc11	U	hpmcounter17	User-mode Hardware Performance Counter 14	Zihpm any
0xc12	U	hpmcounter18	User-mode Hardware Performance Counter 15	Zihpm any
0xc13	U	hpmcounter19	User-mode Hardware Performance Counter 16	Zihpm any
0xc14	U	hpmcounter20	User-mode Hardware Performance Counter 17	Zihpm any
0xc15	U	hpmcounter21	User-mode Hardware Performance Counter 18	Zihpm any
0xc16	U	hpmcounter22	User-mode Hardware Performance Counter 19	Zihpm any
0xc17	U	hpmcounter23	User-mode Hardware Performance Counter 20	Zihpm any
0xc18	U	hpmcounter24	User-mode Hardware Performance Counter 21	Zihpm any
0xc19	U	hpmcounter25	User-mode Hardware Performance Counter 22	Zihpm any
0xc1a	U	hpmcounter26	User-mode Hardware Performance Counter 23	Zihpm any
0xc1b	U	hpmcounter27	User-mode Hardware Performance Counter 24	Zihpm any
0xc1c	U	hpmcounter28	User-mode Hardware Performance Counter 25	Zihpm any
0xc1d	U	hpmcounter29	User-mode Hardware Performance Counter 26	Zihpm any
0xc1e	U	hpmcounter30	User-mode Hardware Performance Counter 27	Zihpm any
0xc1f	U	hpmcounter31	User-mode Hardware Performance Counter 28	Zihpm any
0xda0	S	scountovf	Supervisor Count Overflow	Sscofpmf any

Address	Mode	Name	Long Name	Primary Extension
0xf11	M	mvendorid	Machine Vendor ID	Sm any
0xf12	M	marchid	Machine Architecture ID	Sm any
0xf13	M	mimpid	Machine Implementation ID	Sm any
0xf14	M	mhartid	Machine Hart ID	Sm any

6. Additional Requirements

This section contains requirements in addition to those already specified related to extensions and parameters. These additional requirements are organized as groups of related requirements.

6.1. M-mode Requirements

Extra requirements for M-mode beyond the minimum M-mode defined by the Sm extension. These extra requirements come from github.com/riscv/riscv-profiles/blob/main/src/old-m-profiles.adoc.

Req Number	Description
REQ-M_Mode-Non_Zero_CSRs	The mvendorid , marchid , and mimpid CSRs must be nonzero.
REQ-M_Mode-mstatus_writable_fields	The mstatus.TVM , mstatus.TW , and mstatus.TSR CSR fields must be writable.
REQ-M_Mode-medeleg_writable_bits	The medeleg CSR bits 3, 8, 12, 13, and 15 must be writable.
REQ-M_Mode-mideleg_writable_bits	The mideleg CSR bits 1, 5, and 9 must be writable.
REQ-M_Mode-mideleg_readonlyzero_bits	The mideleg CSR bits 3, 7, and 11 must be read-only zero.
REQ-M_Mode-mcounteren_writable_bits	For any mhpmcounter that is writable, the corresponding bit in mcounteren must be writable.

Appendix A: Extension Details

A.1. Extension A

Long Name: Atomic instructions
Version Requirement: ~> 2.1

A.1.1. Available Versions

Version 2.1.0	
State	ratified
Ratification date	2019-12

A.1.2. Synopsis

The atomic-instruction extension, named [A](#), contains instructions that atomically read-modify-write memory to support synchronization between multiple RISC-V harts running in the same memory space. The two forms of atomic instruction provided are load-reserved/store-conditional instructions and atomic fetch-and-op memory instructions. Both types of atomic instruction support various memory consistency orderings including unordered, acquire, release, and sequentially consistent semantics. These instructions allow RISC-V to support the RCsc memory consistency model. cite:[Gharachorloo90memoryconsistency]



After much debate, the language community and architecture community appear to have finally settled on release consistency as the standard memory consistency model and so the RISC-V atomic support is built around this model.

The [A](#) extension comprises instructions provided by the [Zaamo](#) and [Zalrsc](#) extensions.

A.1.3. Specifying Ordering of Atomic Instructions

The base RISC-V ISA has a relaxed memory model, with the [FENCE](#) instruction used to impose additional ordering constraints. The address space is divided by the execution environment into memory and I/O domains, and the [FENCE](#) instruction provides options to order accesses to one or both of these two address domains.

To provide more efficient support for release consistency cite:[Gharachorloo90memoryconsistency], each atomic instruction has two bits, *aq* and *rl*, used to specify additional memory ordering constraints as viewed by other RISC-V harts. The bits order accesses to one of the two address domains, memory or I/O, depending on which address domain the atomic instruction is accessing. No ordering constraint is implied to accesses to the other domain, and a FENCE instruction should be used to order across both domains.

If both bits are clear, no additional ordering constraints are imposed on the atomic memory operation. If only the *aq* bit is set, the atomic memory operation is treated as an *acquire* access, i.e., no following memory operations on this RISC-V hart can be observed to take place before the acquire memory operation. If only the *rl* bit is set, the atomic memory operation is treated as a *release* access, i.e., the release memory operation cannot be observed to take place before any earlier memory operations on this RISC-V hart. If both the *aq* and *rl* bits are set, the atomic memory operation is *sequentially consistent* and cannot be observed to happen before any earlier memory operations or after any later memory operations in the same RISC-V hart and to the same address domain.

A.2. Extension B

Long Name: Bit Manipulation
Version Requirement: ~> 1.0.0

A.2.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-04
Ratification document	drive.google.com/file/d/1SgLoasaBjs5WboQMaU3wpHkjUwV71UZn/view

A.2.2. Synopsis

The B standard extension comprises instructions provided by the [Zba](#), [Zbb](#), and [Zbs](#) extensions.

Bit 1 of the [misa](#) register encodes the presence of the B standard extension. When [misa.B](#) is 1, the implementation supports the instructions provided by the [Zba](#), [Zbb](#), and [Zbs](#) extensions. When [misa.B](#) is 0, it indicates that the implementation may not support one or more of the [Zba](#), [Zbb](#), or [Zbs](#) extensions.

A.3. Extension C

Long Name: Compressed instructions
Version Requirement: ~> 2.0

A.3.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2019-12

A.3.2. Synopsis

The **C** extension reduces static and dynamic code size by adding short 16-bit instruction encodings for common operations. The C extension can be added to any of the base ISAs (RV32, RV64, RV128), and we use the generic term "RVC" to cover any of these. Typically, 50%-60% of the RISC-V instructions in a program can be replaced with RVC instructions, resulting in a 25%-30% code-size reduction.

A.3.3. Overview

RVC uses a simple compression scheme that offers shorter 16-bit versions of common 32-bit RISC-V instructions when:

- the immediate or address offset is small, or
- one of the registers is the zero register (**x0**), the ABI link register (**x1**), or the ABI stack pointer (**x2**), or
- the destination register and the first source register are identical, or
- the registers used are the 8 most popular ones.

The C extension is compatible with all other standard instruction extensions. The C extension allows 16-bit instructions to be freely intermixed with 32-bit instructions, with the latter now able to start on any 16-bit boundary, i.e., IALIGN=16. With the addition of the C extension, no instructions can raise instruction-address-misaligned exceptions.



Removing the 32-bit alignment constraint on the original 32-bit instructions allows significantly greater code density.

The compressed instruction encodings are mostly common across RV32C, RV64C, and RV128C, but as shown in [Table 34](#), a few opcodes are used for different purposes depending on base ISA. For example, the wider address-space RV64C and RV128C variants require additional opcodes to compress loads and stores of 64-bit integer values, while RV32C uses the same opcodes to compress loads and stores of single-precision floating-point values. Similarly, RV128C requires additional opcodes to capture loads and stores of 128-bit integer values, while these same opcodes are used for loads and stores of double-precision floating-point values in RV32C and RV64C. If the C extension is implemented, the appropriate compressed floating-point load and store instructions must be provided whenever the relevant standard floating-point extension (F and/or D) is also implemented. In addition, RV32C includes a compressed jump and link instruction to compress short-range subroutine calls, where the same opcode is used to compress ADDIW for RV64C and RV128C.



- Double-precision loads and stores are a significant fraction of static and dynamic instructions, hence the motivation to include them in the RV32C and RV64C encoding.
- Although single-precision loads and stores are not a significant source of static or dynamic compression for benchmarks compiled for the currently supported ABIs, for microcontrollers that only provide hardware single-precision floating-point units and have an ABI that only supports single-precision floating-point numbers, the single-precision loads and stores will be used at least as frequently as double-precision loads and stores in the measured benchmarks. Hence, the motivation to provide compressed support for these in RV32C.
- Short-range subroutine calls are more likely in small binaries for microcontrollers, hence the motivation to include these in RV32C.
- Although reusing opcodes for different purposes for different base ISAs adds some complexity to documentation, the impact on implementation complexity is small even for designs that support multiple base ISAs. The compressed floating-point load and store variants use the same instruction format with the same register specifiers as the wider integer loads and stores.

RVC was designed under the constraint that each RVC instruction expands into a single 32-bit instruction in either the base ISA (RV32I/E, RV64I/E, or RV128I) or the F and D standard extensions where present. Adopting this constraint has two main benefits:

- Hardware designs can simply expand RVC instructions during decode, simplifying verification and minimizing modifications to existing microarchitectures.
- Compilers can be unaware of the RVC extension and leave code compression to the assembler and linker, although a compression-aware compiler will generally be able to produce better results.



We felt the multiple complexity reductions of a simple one-one mapping between C and base IFD instructions far outweighed the potential gains of a slightly denser encoding that added additional instructions only supported in the C extension, or that allowed encoding of multiple IFD instructions in one C instruction.

It is important to note that the C extension is not designed to be a stand-alone ISA, and is meant to be used alongside a base ISA.

Variable-length instruction sets have long been used to improve code density. For example, the IBM Stretch [cite:\[stretch\]](#), developed in the late 1950s, had an ISA with 32-bit and 64-bit instructions, where some of the 32-bit instructions were compressed versions of the full 64-bit instructions. Stretch also employed the concept of limiting the set of registers that were addressable in some of the shorter instruction formats, with short branch instructions that could only refer to one of the index registers. The later IBM 360 architecture [cite:\[ibm360\]](#) supported a simple variable-length instruction encoding with 16-bit, 32-bit, or 48-bit instruction formats.

In 1963, CDC introduced the Cray-designed CDC 6600 [cite:\[cdc6600\]](#), a precursor to RISC architectures, that introduced a register-rich load-store architecture with instructions of two lengths, 15-bits and 30-bits. The later Cray-1 design used a very similar instruction format, with 16-bit and 32-bit instruction lengths.

The initial RISC ISAs from the 1980s all picked performance over code size, which was reasonable for a workstation environment, but not for embedded systems. Hence, both ARM and MIPS subsequently made versions of the ISAs that offered smaller code size by offering an alternative 16-bit wide instruction set instead of the standard 32-bit wide instructions. The compressed RISC ISAs reduced code size relative to their starting points by about 25-30%, yielding code that was significantly smaller than 80x86. This result surprised some, as their intuition was that the variable-length CISC ISA should be smaller than RISC ISAs that offered only 16-bit and 32-bit formats.

Since the original RISC ISAs did not leave sufficient opcode space free to include these unplanned compressed instructions, they were instead developed as complete new ISAs. This meant compilers needed different code generators for the separate compressed ISAs. The first compressed RISC ISA extensions (e.g., ARM Thumb and MIPS16) used only a fixed 16-bit instruction size, which gave good reductions in static code size but caused an increase in dynamic instruction count, which led to lower performance compared to the original fixed-width 32-bit instruction size. This led to the development of a second generation of compressed RISC ISA designs with mixed 16-bit and 32-bit instruction lengths (e.g., ARM Thumb2, microMIPS, PowerPC VLE), so that performance was similar to pure 32-bit instructions but with significant code size savings. Unfortunately, these different generations of compressed ISAs are incompatible with each other and with the original uncompressed ISA, leading to significant complexity in documentation, implementations, and software tools support.

Of the commonly used 64-bit ISAs, only PowerPC and microMIPS currently supports a compressed instruction format. It is surprising that the most popular 64-bit ISA for mobile platforms (ARM v8) does not include a compressed instruction format given that static code size and dynamic instruction fetch bandwidth are important metrics. Although static code size is not a major concern in larger systems, instruction fetch bandwidth can be a major bottleneck in servers running commercial workloads, which often have a large instruction working set.

Benefiting from 25 years of hindsight, RISC-V was designed to support compressed instructions from the outset, leaving enough opcode space for RVC to be added as a simple extension on top of the base ISA (along with many other extensions). The philosophy of RVC is to reduce code size for embedded applications *and* to improve performance and energy-efficiency for all applications due to fewer misses in the instruction cache. Waterman shows that RVC fetches 25%-30% fewer instruction bits, which reduces instruction cache misses by 20%-25%, or roughly the same performance impact as doubling the instruction cache size. [cite:\[waterman-ms\]](#)



A.3.4. Compressed Instruction Formats

[Table 4](#) shows the nine compressed instruction formats. CR, CI, and CSS can use any of the 32 RVI registers, but CIW, CL, CS, CA, and CB are limited to just 8 of them. [Table 5](#) lists these popular registers, which correspond to registers **x8** to **x15**. Note that there is a separate version of load and store instructions that use the stack pointer as the base address register, since saving to and restoring from the stack are so prevalent, and that they use the CI and CSS formats to allow access to all 32 data registers. CIW supplies an 8-bit immediate for the ADDI4SPN instruction.



The RISC-V ABI was changed to make the frequently used registers map to registers 'x8-x15'. This simplifies the decompression decoder by having a contiguous naturally aligned set of register numbers, and is also compatible with the RV32E and RV64E base ISAs, which only have 16 integer registers.

Compressed register-based floating-point loads and stores also use the CL and CS formats respectively, with the eight registers mapping to **f8** to **f15**.



*The standard RISC-V calling convention maps the most frequently used floating-point registers to registers **f8** to **f15**, which allows the same register decompression decoding as for integer register numbers.*

The formats were designed to keep bits for the two register source specifiers in the same place in all instructions, while the destination register field can move. When the full 5-bit destination register specifier is present, it is in the same place as in the 32-bit RISC-V encoding. Where immediates are sign-extended, the sign extension is always from bit 12. Immediate fields have been scrambled, as in the base specification, to reduce the number of immediate muxes required.



The immediate fields are scrambled in the instruction formats instead of in sequential order so that as many bits as possible are in the same position in every instruction, thereby simplifying implementations.

For many RVC instructions, zero-valued immediates are disallowed and **x0** is not a valid 5-bit register specifier. These restrictions free up encoding space for other instructions requiring fewer operand bits.

Table 4. Compressed 16-bit RVC instruction formats

Format	Meaning	15 14 13 12		11 10 9 8 7			6 5 4 3 2			1 0
CR	Register	funct4		rd/rs1			rs2			op
CI	Immediate	funct3	imm	rd/rs1			imm			op
CSS	Stack-relative Store	funct3	imm			rs2			op	
CIW	Wide Immediate	funct3	imm					rd'	op	
CL	Load	funct3	imm		rs1'	imm	rd'	op		
CS	Store	funct3	imm		rs1'	imm	rs2'	op		
CA	Arithmetic	funct6			rd'/rs1'	funct2	rs2'	op		
CB	Branch/Arithmetic	funct3	offset		rd'/rs1'	offset			op	
CJ	Jump	funct3	jump target						op	

Table 5. Registers specified by the three-bit *rs1'*, *rs2'*, and *rd'* fields of the *CIW*, *CL*, *CS*, *CA*, and *CB* formats.

RVC Register Number	000	001	010	011	100	101	110	111
Integer Register Number	x8	x9	x10	x11	x12	x13	x14	x15
Integer Register ABI Name	s0	s1	a0	a1	a2	a3	a4	a5
Floating-Point Register Number	f8	f9	f10	f11	f12	f13	f14	f15
Floating-Point Register ABI Name	fs0	fs1	fa0	fa1	fa2	fa3	fa4	fa5

A.4. Extension D

Long Name: Double-precision floating-point

Version Requirement: ~> 2.2

A.4.1. Available Versions

Version 2.2.0	
State	ratified
Ratification date	2019-12
Changes	Define NaN-boxing scheme, changed definition of FMAX and FMIN

A.4.2. Synopsis

The [D](#) extension adds double-precision floating-point computational instructions compliant with the [IEEE 754-2008](#) arithmetic standard. The [D](#) extension depends on the base single-precision instruction subset [F](#).

A.4.3. D Register State

The [D](#) extension widens the 32 floating-point registers, [f0-f31](#), to 64 bits (FLEN=64 in [Table 6](#). The [f](#) registers can now hold either 32-bit or 64-bit floating-point values as described below in [Section A.4.4](#).

	FLEN can be 32, 64, or 128 depending on which of the F, D, and Q extensions are supported. There can be up to four different floating-point precisions supported, including H, F, D, and Q.

A.4.4. NaN Boxing of Narrower Values

When multiple floating-point precisions are supported, then valid values of narrower *n*-bit types, *n*<FLEN, are represented in the lower *n* bits of an FLEN-bit NaN value, in a process termed NaN-boxing. The upper bits of a valid NaN-boxed value must be all 1s. Valid NaN-boxed *n*-bit values therefore appear as negative quiet NaNs (qNaNs) when viewed as any wider *m*-bit value, *n* < *m* ≤ FLEN. Any operation that writes a narrower result to an 'f' register must write all 1s to the uppermost FLEN-*n* bits to yield a legal NaN-boxedvalue.

	Software might not know the current type of data stored in a floating-point register but has to be able to save and restore the register values, hence the result of using wider operations to transfer narrower values has to be defined. A common case is for callee-saved registers, but a standard convention is also desirable for features including varargs, user-level threading libraries, virtual machine migration, and debugging.

Floating-point *n*-bit transfer operations move external values held in IEEE standard formats into and out of the [f](#) registers, and comprise floating-point loads and stores (FL*n*/FS*n*) and floating-point move instructions (FMV*n*.X/FMV.X.*n*). A narrower *n*-bit transfer, *n*<FLEN, into the [f](#) registers will create a valid NaN-boxed value. A narrower *n*-bit transfer out of the floating-point registers will transfer the lower *n* bits of the register ignoring the upper FLEN-*n* bits.

Apart from transfer operations described in the previous paragraph, all other floating-point operations on narrower n -bit operations, $n < \text{FLEN}$, check if the input operands are correctly NaN-boxed, i.e., all upper $\text{FLEN} - n$ bits are 1. If so, the n least-significant bits of the input are used as the input value, otherwise the input value is treated as an n -bit canonical NaN.



Earlier versions of this document did not define the behavior of feeding the results of narrower or wider operands into an operation, except to require that wider saves and restores would preserve the value of a narrower operand. The new definition removes this implementation-specific behavior, while still accommodating both non-recoded and recoded implementations of the floating-point unit. The new definition also helps catch software errors by propagating NaNs if values are used incorrectly.

Non-recoded implementations unpack and pack the operands to IEEE standard format on the input and output of every floating-point operation. The NaN-boxing cost to a non-recoded implementation is primarily in checking if the upper bits of a narrower operation represent a legal NaN-boxed value, and in writing all 1s to the upper bits of a result.

Recoded implementations use a more convenient internal format to represent floating-point values, with an added exponent bit to allow all values to be held normalized. The cost to the recoded implementation is primarily the extra tagging needed to track the internal types and sign bits, but this can be done without adding new state bits by recoding NaNs internally in the exponent field. Small modifications are needed to the pipelines used to transfer values in and out of the recoded format, but the datapath and latency costs are minimal. The recoding process has to handle shifting of input subnormal values for wide operands in any case, and extracting the NaN-boxed value is a similar process to normalization except for skipping over leading-1 bits instead of skipping over leading-0 bits, allowing the datapath muxing to be shared.





The rationale to not include Q as a profile option is that quad-precision floating-point is unlikely to be implemented in hardware, and so we do not require or expect software to expend effort optimizing use of Q instructions in case they are present.

A.4.5. Instructions

The following 26 instructions are added by extension version 2.2.0 (the minimum version of this extension that satisfies the extension requirement).

fadd.d	Floating-Point Add Double-Precision
fclass.d	Floating-Point Classify Double-Precision
fcvt.d.s	Floating-Point Convert Single-Precision to Double-Precision
fcvt.d.w	Floating-Point Convert Word to Double-Precision
fcvt.d.wu	Floating-Point Convert Unsigned Word to Double-Precision
fcvt.s.d	Floating-Point Convert Double-Precision to Single-Precision
fcvt.w.d	Floating-Point Convert Double-Precision to Word
fcvt.wu.d	Floating-Point Convert Double-Precision to Unsigned Word
fdiv.d	Floating-Point Divide Double-Precision
feq.d	Floating-Point Equal Double-Precision
fld	Floating-Point Load Double-Precision
fle.d	Floating-Point Less Than or Equal Double-Precision
flt.d	Floating-Point Less Than Double-Precision
fmadd.d	Floating-Point Multiply-Add Double-Precision
fmax.d	Floating-Point Maximum-Number Double-Precision
fmin.d	Floating-Point Minimum-Number Double-Precision
fmsub.d	Floating-Point Multiply-Subtract Double-Precision
fmul.d	Floating-Point Multiply Double-Precision
fnmadd.d	Floating-Point Negate-Multiply-Add Double-Precision
fnmsub.d	Floating-Point Negate-Multiply-Subtract Double-Precision
fsd	Floating-Point Store Double-Precision
fsgnj.d	Floating-Point Sign-Inject Double-Precision
fsgnjn.d	Floating-Point Sign-Inject Negate Double-Precision
fsgnjx.d	Floating-Point Sign-Inject XOR Double-Precision
fsqrt.d	Floating-Point Square Root Double-Precision
fsub.d	Floating-Point Subtract Double-Precision

A.5. Extension F

Long Name: Single-precision floating-point

A.5.1. Available Versions

Version 2.2.0	
State	ratified
Ratification date	2019-12
Changes	Define NaN-boxing scheme, changed definition of FMAX and FMIN

A.5.2. Synopsis

This chapter describes the standard instruction-set extension for single-precision floating-point, which is named "F" and adds single-precision floating-point computational instructions compliant with the IEEE 754-2008 arithmetic standard cite:[ieee754-2008]. The F extension depends on the "Zicsr" extension for control and status register access.

A.5.3. F Register State

The F extension adds 32 floating-point registers, **f0-f31**, each 32 bits wide, and a floating-point control and status register **fcsr**, which contains the operating mode and exception status of the floating-point unit. This additional state is shown in [Table 6](#). We use the term FLEN to describe the width of the floating-point registers in the RISC-V ISA, and FLEN=32 for the F single-precision floating-point extension. Most floating-point instructions operate on values in the floating-point register file. Floating-point load and store instructions transfer floating-point values between registers and memory. Instructions to transfer values to and from the integer register file are also provided.



We considered a unified register file for both integer and floating-point values as this simplifies software register allocation and calling conventions, and reduces total user state. However, a split organization increases the total number of registers accessible with a given instruction width, simplifies provision of enough regfile ports for wide superscalar issue, supports decoupled floating-point-unit architectures, and simplifies use of internal floating-point encoding techniques. Compiler support and calling conventions for split register file architectures are well understood, and using dirty bits on floating-point register file state can reduce context-switch overhead.

Table 6. RISC-V standard F extension single-precision floating-point state

FLEN-1	0
	f0
	f1
	f2
	f3
	f4
	f5
	f6
	f7
	f8
	f9
	f10
	f11
	f12
	f13
	f14
	f15
	f16
	f17
	f18
	f19
	f20
	f21
	f22
	f23
	f24
	f25
	f26
	f27
	f28
	f29

FLEN-1	0
f30	
f31	
FLEN	
31	0
fcsr	
32	

Floating-Point Control and Status Register

The floating-point control and status register, [fcsr](#), is a RISC-V control and status register (CSR). It is a 32-bit read/write register that selects the dynamic rounding mode for floating-point arithmetic operations and holds the accrued exception flags, as shown in [Floating-Point Control and Status Register](#).

Floating-point control and status register

Unresolved directive in AC200-CRD.adoc - include::images/wavedrom/float-csr.adoc[]

The [fcsr](#) register can be read and written with the FRCSR and FSCSR instructions, which are assembler pseudoinstructions built on the underlying CSR access instructions. FRCSR reads [fcsr](#) by copying it into integer register *rd*. FSCSR swaps the value in [fcsr](#) by copying the original value into integer register *rd*, and then writing a new value obtained from integer register *rs1* into [fcsr](#).

The fields within the [fcsr](#) can also be accessed individually through different CSR addresses, and separate assembler pseudoinstructions are defined for these accesses. The FRRM instruction reads the Rounding Mode field [frm](#) ([fcsr](#) bits 7—5) and copies it into the least-significant three bits of integer register *rd*, with zero in all other bits. FSRM swaps the value in [frm](#) by copying the original value into integer register *rd*, and then writing a new value obtained from the three least-significant bits of integer register *rs1* into [frm](#). FRFLAGS and FSFLAGS are defined analogously for the Accrued Exception Flags field [fflags](#) ([fcsr](#) bits 4—0).

Bits 31—8 of the [fcsr](#) are reserved for other standard extensions. If these extensions are not present, implementations shall ignore writes to these bits and supply a zero value when read. Standard software should preserve the contents of these bits.

Floating-point operations use either a static rounding mode encoded in the instruction, or a dynamic rounding mode held in [frm](#). Rounding modes are encoded as shown in [Table 7](#). A value of 111 in the instruction’s *rm* field selects the dynamic rounding mode held in [frm](#). The behavior of floating-point instructions that depend on rounding mode when executed with a reserved rounding mode is *reserved*, including both static reserved rounding modes (101-110) and dynamic reserved rounding modes (101-111). Some instructions, including widening conversions, have the *rm* field but are nevertheless mathematically unaffected by the rounding mode; software should set their *rm* field to RNE (000) but implementations must treat the *rm* field as usual (in particular, with regard to decoding legal vs. reserved encodings).

Table 7. Rounding mode encoding.

Rounding Mode	Mnemonic	Meaning
000	RNE	Round to Nearest, ties to Even
001	RTZ	Round towards Zero
010	RDN	Round Down (towards $-\infty$)
011	RUP	Round Up (towards $+\infty$)
100	RMM	Round to Nearest, ties to Max Magnitude
101		<i>Reserved for future use.</i>
110		<i>Reserved for future use.</i>
111	DYN	In instruction’s <i>rm</i> field, selects dynamic rounding mode; In Rounding Mode register, <i>reserved</i> .



The C99 language standard effectively mandates the provision of a dynamic rounding mode register. In typical implementations, writes to the dynamic rounding mode CSR state will serialize the pipeline. Static rounding modes are used to implement specialized arithmetic operations that often have to switch frequently between different rounding modes.

The ratified version of the F spec mandated that an illegal-instruction exception was raised when an instruction was executed with a reserved dynamic rounding mode. This has been weakened to reserved, which matches the behavior of static rounding-mode instructions. Raising an illegal-instruction exception is still valid behavior when encountering a reserved encoding, so implementations compatible with the ratified spec are compatible with the weakened spec.

The accrued exception flags indicate the exception conditions that have arisen on any floating-point arithmetic instruction since the field was last reset by software, as shown in [Table 8](#). The base RISC-V ISA does not support generating a trap on the setting of a floating-point exception flag.

Table 8. Accrued exception flag encoding.

Flag Mnemonic	Flag Meaning
NV	Invalid Operation
DZ	Divide by Zero

Flag Mnemonic	Flag Meaning
OF	Overflow
UF	Underflow
NX	Inexact



As allowed by the standard, we do not support traps on floating-point exceptions in the F extension, but instead require explicit checks of the flags in software. We considered adding branches controlled directly by the contents of the floating-point accrued exception flags, but ultimately chose to omit these instructions to keep the ISA simple.

A.5.4. NaN Generation and Propagation

Except when otherwise stated, if the result of a floating-point operation is NaN, it is the canonical NaN. The canonical NaN has a positive sign and all significand bits clear except the MSB, a.k.a. the quiet bit. For single-precision floating-point, this corresponds to the pattern `0x7fc00000`.



We considered propagating NaN payloads, as is recommended by the standard, but this decision would have increased hardware cost. Moreover, since this feature is optional in the standard, it cannot be used in portable code.

Implementers are free to provide a NaN payload propagation scheme as a nonstandard extension enabled by a nonstandard operating mode. However, the canonical NaN scheme described above must always be supported and should be the default mode.



We require implementations to return the standard-mandated default values in the case of exceptional conditions, without any further intervention on the part of user-level software (unlike the Alpha ISA floating-point trap barriers). We believe full hardware handling of exceptional cases will become more common, and so wish to avoid complicating the user-level ISA to optimize other approaches. Implementations can always trap to machine-mode software handlers to provide exceptional default values.

A.5.5. Subnormal Arithmetic

Operations on subnormal numbers are handled in accordance with the IEEE 754-2008 standard.

In the parlance of the IEEE standard, tininess is detected after rounding.



Detecting tininess after rounding results in fewer spurious underflow signals.

A.5.6. Instructions

The following 26 instructions are added by extension version 2.2.0 (the minimum version of this extension that satisfies the extension requirement).

fadd.s	Floating-Point Add Single-Precision
fclass.s	Floating-Point Classify Single-Precision
fcvt.s.w	Floating-Point Convert Word to Single-Precision
fcvt.s.wu	Floating-Point Convert Unsigned Word to Single-Precision
fcvt.w.s	Floating-Point Convert Single-Precision to Word
fcvt.wu.s	Floating-Point Convert Single-Precision to Unsigned Word
fdiv.s	Floating-Point Divide Single-Precision
feq.s	Floating-Point Equal Single-Precision
fle.s	Floating-Point Less Than or Equal Single-Precision
flt.s	Floating-Point Less Than Single-Precision
flw	Floating-Point Load Single-Precision
fmadd.s	Floating-Point Multiply-Add Single-Precision
fmax.s	Floating-Point Maximum-Number Single-Precision
fmin.s	Floating-Point Minimum-Number Single-Precision
fmsub.s	Floating-Point Multiply-Subtract Single-Precision
fmul.s	Floating-Point Multiply Single-Precision
fmv.w.x	Floating-Point Move Single-Precision Word from Integer Register
fmv.x.w	Floating-Point Move Single-Precision Word to Integer Register
fnmadd.s	Floating-Point Negate-Multiply-Add Single-Precision
fnmsub.s	Floating-Point Negate-Multiply-Subtract Single-Precision
fsgnj.s	Floating-Point Sign-Inject Single-Precision

fsgnjn.s	Floating-Point Sign-Inject Negate Single-Precision
fsgnjx.s	Floating-Point Sign-Inject XOR Single-Precision
fsqrt.s	Floating-Point Square Root Single-Precision
fsub.s	Floating-Point Subtract Single-Precision
fsw	Floating-Point Store Single-Precision

A.5.7. CSRs

The following 3 CSRs are added by extension version 2.2.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
fcsr	Floating-point control and status register (frm + fflags)	0x3	U
fflags	Floating-Point Accrued Exceptions	0x1	U
frm	Floating-Point Dynamic Rounding Mode	0x2	U

A.6. Extension I

Long Name: Base integer ISA (RV32I or RV64I)

Version Requirement: ~> 2.1

A.6.1. Available Versions

Version 2.1.0	
State	ratified
Ratification date	2019-06
Changes	ratified RVWMO memory model and exclusion of FENCE.I, counters, and CSR instructions that were in previous base ISA

A.6.2. Synopsis

Base integer instructions — TODO

	RVI is the mandatory base ISA for RVA, and is little-endian.
	As per the unprivileged architecture specification, the ecall instruction causes a requested trap to the execution environment.
	Misaligned loads and stores might not be supported.
	The fence.tso instruction is mandatory.
	 The fence.tso instruction was incorrectly described as optional in the 2019 ratified specifications. However, fence.tso is encoded within the standard fence encoding such that implementations must treat it as a simple global fence if they do not natively support TSO-ordering optimizations. As software can always assume without any penalty that fence.tso is being exploited by a hardware implementation, there is no advantage to making the instruction a profile option. Later versions of the unprivileged ISA specifications correctly indicate that fence.tso is mandatory.

A.6.3. Instructions

The following 43 instructions are added by extension version 2.1.0 (the minimum version of this extension that satisfies the extension requirement).

add	Integer add
addi	Add immediate
and	And
andi	And immediate
auipc	Add upper immediate to pc
beq	Branch if equal
bge	Branch if greater than or equal
bgeu	Branch if greater than or equal unsigned
blt	Branch if less than
bltu	Branch if less than unsigned

bne	Branch if not equal
ebreak	Breakpoint exception
ecall	Environment call
fence.tso	Memory ordering fence, total store ordering
fence	Memory ordering fence
jal	Jump and link
jalr	Jump and link register
lb	Load byte
lbu	Load byte unsigned
ld	Load doubleword
lh	Load halfword
lhu	Load halfword unsigned
lui	Load upper immediate
lw	Load word
or	Or
ori	Or immediate
sb	Store byte
sd	Store doubleword
sh	Store halfword
sll	Shift left logical
slli	Shift left logical immediate
slt	Set on less than
slti	Set on less than immediate
sltiu	Set on less than immediate unsigned
sltu	Set on less than unsigned
sra	Shift right arithmetic
srai	Shift right arithmetic immediate
srl	Shift right logical
srli	Shift right logical immediate
sub	Subtract
sw	Store word
xor	Exclusive Or
xori	Exclusive Or immediate

A.7. Extension M

Long Name: Integer multiply and divide
Version Requirement: ~> 2.0

A.7.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2019-12

A.7.2. Synopsis

This chapter describes the standard integer multiplication and division instruction extension, which is named [M](#) and contains instructions that multiply or divide values held in two integer registers.



We separate integer multiply and divide out from the base to simplify low-end implementations, or for applications where integer multiply and divide operations are either infrequent or better handled in attached accelerators.

A.7.3. Instructions

The following 8 instructions are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

div	Signed division
divu	Unsigned division
mul	Signed multiply
mulh	Signed multiply high
mulhsu	Signed/unsigned multiply high
mulhu	Unsigned multiply high
rem	Signed remainder
remu	Unsigned remainder

A.8. Extension S

Long Name: Supervisor mode
Version Requirement: ~> 1.13

A.8.1. Available Versions

Version 1.11.0	
State	ratified
Ratification date	2019-06
Version 1.12.0	
State	ratified
Ratification date	2021-12
Version 1.13.0	
State	ratified
Ratification date	2024-10

A.8.2. Synopsis

This chapter describes the RISC-V supervisor-level architecture, which contains a common core that is used with various supervisor-level address translation and protection schemes.



Supervisor mode is deliberately restricted in terms of interactions with underlying physical hardware, such as physical memory and device interrupts, to support clean virtualization. In this spirit, certain supervisor-level facilities, including requests for timer and interprocessor interrupts, are provided by implementation-specific mechanisms. In some systems, a supervisor execution environment (SEE) provides these facilities in a manner specified by a supervisor binary interface (SBI). Other systems supply these facilities directly, through some other implementation-defined mechanism.



Supervisor version 1.13

A.8.3. Instructions

The following 2 instructions are added by extension version 1.11.0 (the minimum version of this extension that satisfies the extension requirement).

sfence.vma	Supervisor memory-management fence
sret	Supervisor Mode Return from Trap

A.8.4. CSRs

The following 10 CSRs are added by extension version 1.11.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
medeleg	Machine Exception Delegation	0x302	M
satp	Supervisor Address Translation and Protection	0x180	S
scause	Supervisor Cause	0x142	S
scounteren	Supervisor Counter Enable	0x106	S
sepc	Supervisor Exception Program Counter	0x141	S
sip	Supervisor Interrupt Pending	0x144	S
sscratch	Supervisor Scratch Register	0x140	S

Name	Long Name	Address	Mode
sstatus	Supervisor Status	0x100	S
stval	Supervisor Trap Value	0x143	S
stvec	Supervisor Trap Vector	0x105	S

A.8.5. OUT-OF-SCOPE Parameters

ASID_WIDTH ⇒ 0 to 16

Number of implemented ASID bits. Maximum is 16 for XLEN==64, and 9 for XLEN==32

MSTATUS_TVM_IMPLEMENTED ⇒ boolean

Whether or not mstatus.TVM is implemented.

When not implemented mstatus.TVM will be read-only-zero.

REPORT_ENCODING_IN_STVAL_ON_ILLEGAL_INSTRUCTION ⇒ boolean

When true, [stval](#) is written with the encoding of an instruction that causes an [IllegalInstruction](#) exception.

When false [stval](#) is written with 0 when an [IllegalInstruction](#) exception occurs.

REPORT_VA_IN_MTVAL_ON_INSTRUCTION_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionPageFault](#).

When false, [mtval](#) is written with 0 when an instruction fetch causes an [InstructionPageFault](#).

REPORT_VA_IN_MTVAL_ON_LOAD_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual address of a load when it causes a [LoadPageFault](#).

When false, [mtval](#) is written with 0 when a load causes a [LoadPageFault](#).

REPORT_VA_IN_MTVAL_ON_STORE_AMO_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual address of a store when it causes a [StoreAmoPageFault](#).

When false, [mtval](#) is written with 0 when a store causes a [StoreAmoPageFault](#).

REPORT_VA_IN_STVAL_ON_BREAKPOINT ⇒ boolean

When true, [stval](#) is written with the virtual PC of the EBREAK instruction (same information as [mepc](#)).

When false, [stval](#) is written with 0 on an EBREAK instruction.

Regardless, [stval](#) is always written with a virtual PC when an external breakpoint is generated

REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionAccessFault](#).

When false, [stval](#) is written with 0 when an instruction fetch causes an [InstructionAccessFault](#).

REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED ⇒ boolean

When true, [stval](#) is written with the virtual PC when an instruction fetch is misaligned.

When false, [stval](#) is written with 0 when an instruction fetch is misaligned.

Note that when IALIGN=16 (i.e., when the [C](#) or one of the [Zc*](#) extensions are implemented), it is impossible to generate a misaligned fetch, and so this parameter has no effect.

REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionPageFault](#).

When false, [stval](#) is written with 0 when an instruction fetch causes an [InstructionPageFault](#).

REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a load when it causes a [LoadAccessFault](#).

When false, [stval](#) is written with 0 when a load causes a [LoadAccessFault](#).

REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED ⇒ boolean

When true, [stval](#) is written with the virtual address of a load instruction when the address is misaligned and MISALIGNED_LDST is false.

When false, [stval](#) is written with 0 when a load address is misaligned and MISALIGNED_LDST is false.

REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a load when it causes a [LoadPageFault](#).

When false, `stval` is written with 0 when a load causes a `LoadPageFault`.

`REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT` ⇒ **boolean**

When true, `stval` is written with the virtual address of a store when it causes a `StoreAmoAccessFault`.

When false, `stval` is written with 0 when a store causes a `StoreAmoAccessFault`.

`REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED` ⇒ **boolean**

When true, `stval` is written with the virtual address of a store instruction when the address is misaligned and `MISALIGNED_LDST` is false.

When false, `stval` is written with 0 when a store address is misaligned and `MISALIGNED_LDST` is false.

`REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT` ⇒ **boolean**

When true, `stval` is written with the virtual address of a store when it causes a `StoreAmoPageFault`.

When false, `stval` is written with 0 when a store causes a `StoreAmoPageFault`.

`SATP_MODE_BARE` ⇒ **boolean**

Whether or not `satp.MODE == Bare` is supported.

`STVAL_WIDTH` ⇒ **≤ 0xffffffffffffff**

The number of implemented bits in `stval`.

Must be greater than or equal to $\max(\text{PHYS\_ADDR\_WIDTH}, \text{VA\_SIZE})$

`STVEC_MODE_DIRECT` ⇒ **boolean**

Whether or not `stvec.MODE` supports Direct (0).

`STVEC_MODE_VECTORED` ⇒ **boolean**

Whether or not `stvec.MODE` supports Vectored (1).

`SXLEN` ⇒ **1-element to 2-element array of [32, 64]**

Set of XLENs supported in S-mode. Can be one of:

- 32: `SXLEN` is always 32
- 64: `SXLEN` is always 64
- [32, 64]: `SXLEN` can be changed (via `mstatus.SXL`) between 32 and 64

`S_MODE_ENDIANNES` ⇒ **[little, big, dynamic]**

Endianness of data in S-mode. Can be one of:

- little: S-mode data is always little endian
- big: S-mode data is always big endian
- dynamic: S-mode data can be either little or big endian, depending on the CSR field `mstatus.SBE`

`TRAP_ON_ECALL_FROM_S` ⇒ **boolean**

Whether or not an ECALL-from-S-mode causes a synchronous exception.

The spec states that implementations may handle ECALLs transparently without raising a trap, in which case the EEI must provide a builtin.

A.9. Extension Sdtrig

Long Name: Debug triggers

Version Requirement: ~> 1.0

A.9.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2025-02

A.9.2. Synopsis

Triggers can cause a breakpoint exception, entry into Debug Mode, or a trace action without having to execute a special instruction. This makes them invaluable when debugging code from ROM. They can trigger on execution of instructions at a given memory address, or on the address/data in loads/stores.

If Sdtrig is implemented, the Trigger Module must support at least one trigger. Accessing trigger CSRs that are not used by any of the implemented triggers must result in an illegal instruction exception. M-Mode and Debug Mode accesses to trigger CSRs that are used by any of the implemented

triggers must succeed, regardless of the current type of the currently selected trigger.

A trigger matches when the conditions that it specifies (e.g. a load from a specific address) are met. A trigger fires when a trigger that matches performs the action configured for that trigger.

Triggers do not fire while in Debug Mode.



Debug triggers

A.9.3. CSRs

The following 5 CSRs are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
mcontext	Machine Context	0x7a8	M
tdata1	Trigger Data 1	0x7a1	M
tdata2	Trigger Data 2	0x7a2	M
tdata3	Trigger Data 3	0x7a3	M
tselect	Trigger Select	0x7a0	M

A.9.4. Parameters

The following parameters (implementation options) may affect the operation of this extension:

DBG_HCONTEXT_WIDTH

Specifies the size of HCONTEXT

DBG_SCONTEXT_WIDTH

Specifies the size of SCONTEXT

DCSR_MPRVEN_TYPE

Implementation of dcsr.MPRVEN is optional. It may be tied to either 0 or 1.

Behavior of the dcsr.MPRVEN bit: * 'read-only-0': tied to 0 * 'read-only-1': tied to 1 * 'rw': read-write

DCSR_STEPIE_TYPE

Implementation of dcsr.STEPIE is optional. It may be tied to either 0 or 1.

Behavior of the dcsr.STEPIE bit: * 'read-only-0': tied to 0 * 'read-only-1': tied to 1 * 'rw': read-write

DCSR_STOPCOUNT_TYPE

Implementation of dcsr.STOPCOUNT is optional. It may be tied to either 0 or 1.

Behavior of the dcsr.STOPCOUNT bit: * 'read-only-0': tied to 0 * 'read-only-1': tied to 1 * 'rw': read-write

DCSR_STOPTIME_TYPE

Implementation of dcsr.STOPTIME is optional. It may be tied to either 0 or 1.

Behavior of the dcsr.STOPTIME bit: * 'read-only-0': tied to 0 * 'read-only-1': tied to 1 * 'rw': read-write

HCONTEXT_AVAILABLE

Specifies if HCONTEXT is available

MCONTEXT_AVAILABLE

Specifies if MCONTEXT is available

A.10. Extension Sha

Long Name: Augmented hypervisor

Version Requirement: ~> 1.0

A.10.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-10

A.10.2. Synopsis

Sha comprises the following extensions:

- **H** The hypervisor extension.
- **Ssstateen** Supervisor-mode view of the state-enable extension. The supervisor-mode (**ssstateen0-3**) and hypervisor-mode (**hstateen0-3**) state-enable registers must be provided.
- **Shcounterenw** For any **hpmcounter** that is not read-only zero, the corresponding bit in **hcounteren** must be writable.
- **Shvstvala** **vstval** must be written in all cases described above for **stval**.
- **Shtvala** **htval** must be written with the faulting guest physical address in all circumstances permitted by the ISA.
- **Shvstvecd** **vstvec.MODE** must be capable of holding the value 0 (Direct). When **vstvec.MODE**=Direct, **vstvec.BASE** must be capable of holding any valid four-byte-aligned address.
- **Shvsatpa** All translation modes supported in **satp** must be supported in **vsatp**.
- **Shgatpa** For each supported virtual memory scheme SvNN supported in **satp**, the corresponding hgatp SvNNx4 mode must be supported. The **hgatp** mode Bare must also be supported.



Sha is a new profile-defined extension that captures the full set of features that are mandated to be supported along with the H extension. There is no change to the features added by including the hypervisor extension in a profile—the new name is solely to simplify the text of the profiles. The definition has been added to the RVA22 profile text, where the hypervisor extension was first added, and will be added to the hypervisor section of the combined ISA manual.



The set of augmented hypervisor extensions: H, Ssstateen, Shcounterenw, Shvstvala, Shtvala, Shvstvecd, Shvsatpa, Shgatpa

A.11. Extension Sm

Long Name: Machine mode
Version Requirement: ~> 1.13

A.11.1. Available Versions

Version 1.11.0	
State	ratified
Ratification date	2019-12
Changes	• Moved Machine spec to Ratified status. • Improvements to the description and commentary. • Specified which interrupt sources are reserved for standard use. • Allocated some synchronous exception causes for custom use. • Specified the priority ordering of synchronous exceptions. • Added specification that xRET instructions may, but are not required to, clear LR reservations if A extension present. • Made the mstatus.MPP field WARL, rather than WLRL. • Made the unused xip fields WPRI, rather than WIRI. • Made the unused misa fields WARL, rather than WIRI. • Rectified an editing error that misdescribed the mechanism by which mstatus is written upon an exception. • Described scheme for emulating misaligned AMOs. • Specified the behavior of the misa and xepc registers in systems with variable IALIGN. • Specified the behavior of writing self-contradictory values to the misa register. • Specified contents of CSRs across XLEN modification. • Moved PLIC chapter into its own document.
Version 1.12.0	
State	ratified
Ratification date	2021-12

Version 1.12.0	
Changes	• Changed MRET to clear mstatus.MPRV when leaving M-mode. • Relaxed I/O regions have been specified to follow RVWMO. The previous specification implied that PPO rules other than fences and acquire/release annotations did not apply. • Constrained the LR/SC reservation set size and shape when using page-based virtual memory. • PMP changes require an SFENCE.VMA on any hart that implements page-based virtual memory, even if VM is not currently enabled. • Removed the N extension. • Defined the mandatory RV32-only CSR mstatush, which contains most of the same fields as the upper 32 bits of RV64's mstatus. • Defined the mandatory CSR mconfigptr, which if nonzero contains the address of a configuration data structure. • Defined mseccfg and msecfgh CSRs, which control the machine's security configuration. • Defined menvcfg CSR (and RV32-only menvcfgh), which control various characteristics of the execution environment. • Designated part of SYSTEM major opcode for custom use. • Permitted the unconditional delegation of less-privileged interrupts. • Added optional big-endian and bi-endian support. • Made priority of load/store/AMO address-misaligned exceptions implementation-defined relative to load/store/AMO page-fault and access-fault exceptions. • Software breakpoint exceptions are permitted to write either 0 or the pc to xtval. • Specified relaxed constraints for implicit reads of non-idempotent regions.

Version 1.13.0	
State	frozen
Changes	• Redefined misa.MXL to be read-only, making MXLEN a constant. • Defined the misa.B field to reflect that the B extension has been implemented. • Defined the misa.V field to reflect that the V extension has been implemented. • Defined the RV32-only medeleg CSR. • Defined the misaligned atomicity granule PMA, superseding the proposed Zam extension. • Defined hardware error and software check exception codes. • Specified synchronization requirements when changing the PBMTE fields in menvcfg and henvcfg. • Exposed count-overflow interrupts to VS-mode via the Shlcofideleg extension. • Relaxed behavior of some HINTs when MXLEN > XLEN. • Transliterated the document from LaTeX into AsciiDoc. • Included all ratified extensions through March 2024. • Clarified that "platform- or custom-use" interrupts are actually "platform-use interrupts", where the platform can choose to make some custom. • Clarified semantics of explicit accesses to CSRs wider than XLEN bits. • Clarified that MXLEN≥SXLEN. • Clarified that WFI is not a HINT instruction. • Clarified that, for a given exception cause, xtval might sometimes be set to a nonzero value but sometimes not. • Clarified exception behavior of unimplemented or inaccessible CSRs. • Replaced the concept of vacant memory regions with inaccessible memory or I/O regions. • Clarified that timer and count-overflow interrupts' arrival in interrupt-pending registers is not immediate. • Clarified that MXR affects only explicit memory accesses.

A.11.2. Synopsis

This chapter describes the machine-level operations available in machine-mode (M-mode), which is the highest privilege mode in a RISC-V hart. M-mode is used for low-level access to a hardware platform and is the first mode entered at reset. M-mode can also be used to implement features that are too difficult or expensive to implement in hardware directly. The RISC-V machine-level ISA contains a common core that is extended depending on which other privilege levels are supported and other details of the hardware implementation. This chapter describes the RISC-V machine-level architecture, which contains a common core that is used with various supervisor-level address translation and protection schemes.

A.11.3. Instructions

The following 2 instructions are added by extension version 1.11.0 (the minimum version of this extension that satisfies the extension requirement).

mret	Machine-mode Return from Trap
wfi	Wait for interrupt

A.11.4. CSRs

The following 16 CSRs are added by extension version 1.11.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
marchid	Machine Architecture ID	0xf12	M
mcause	Machine Cause	0x342	M
mcountinhibit	Machine Counter Inhibit	0x320	M
mcycle	Machine Cycle Counter	0xb00	M
mepc	Machine Exception Program Counter	0x341	M
mhartid	Machine Hart ID	0xf14	M
mie	Machine Interrupt Enable	0x304	M
mimpid	Machine Implementation ID	0xf13	M
minstret	Machine Instructions Retired Counter	0xb02	M
mip	Machine Interrupt Pending	0x344	M
misa	Machine ISA Control	0x301	M
mscratch	Machine Scratch Register	0x340	M
mstatus	Machine Status	0x300	M
mtval	Machine Trap Value	0x343	M
mtvec	Machine Trap Vector Control	0x305	M
mvendorid	Machine Vendor ID	0xf11	M

A.11.5. OUT-OF-SCOPE Parameters

COUNTINHIBIT_EN ⇒ 32-element array where:

- [0] is boolean
- [1] is false
- [2] is boolean

additional items are:

boolean::

+

Indicates which hardware performance monitor counters can be disabled from [mcountinhibit](#).

An unimplemented counter cannot be specified, i.e., if HPM_COUNTER_EN[3] is false, it would be illegal to set COUNTINHIBIT_EN[3] to true.

COUNTINHIBIT_EN[1] can never be true, since it corresponds to [mcountinhibit](#), which is always read-only-0.

MARCHID_IMPLEMENTED ⇒ boolean

- false: [marchid](#) is not implemented, and must be read-only-0
- true: [marchid](#) is implemented, and the value is determined by [ARCH_ID_VALUE](#)

MIMPID_IMPLEMENTED ⇒ boolean

- false: [mimpid](#) is not implemented, and must be read-only-0
- true: [mimpid](#) is implemented, and the value is determined by [IMP_ID_VALUE](#)

MISALIGNED_LDST ⇒ boolean

Does the implementation perform non-atomic misaligned loads and stores to main memory (does **not** affect misaligned support to device memory)? If not, the implementation always throws a misaligned exception.

MISALIGNED_LDST_EXCEPTION_PRIORITY ⇒ [low, high]

The relative priority of a load/store/AMO exception vs. load/store/AMO page-fault or access-fault exceptions.

May be one of:

low	Misaligned load/store/AMO exceptions are always lower priority than load/store/AMO page-fault and access-fault exceptions.
high	Misaligned load/store/AMO exceptions are always higher priority than load/store/AMO page-fault and access-fault exceptions.

MISALIGNED_LDST_EXCEPTION_PRIORITY cannot be "high" when MISALIGNED_MAX_ATOMICITY_GRANULE_SIZE is non-zero, since the atomicity of an access cannot be determined in that case until after address translation.

MISA_CSR_IMPLEMENTED ⇒ boolean

Options:

true

The [misa](#) CSR returns a non-zero value.

false

The [misa](#) CSR is read-only-0.

MTVAL_WIDTH ⇒ 0 to 64

The number of implemented bits in the [mtval](#) CSR. This is the CSR that may be written when a trap is taken into M-mode with exception-specific information to assist software in handling the trap (e.g., address associated with exception).

Must be greater than or equal to $max(\textcolor{red}{PHYS\_ADDR\_WIDTH}, \textcolor{red}{VA\_SIZE})$

MTVEC_ACCESS ⇒ [ro, rw]

Options:

ro

[mtvec](#) is read-only.

rw

[mtvec](#) is read-write, but may not accept all values.

MTVEC_ILLEGAL_WRITE_BEHAVIOR ⇒ [retain, custom]

Options:

retain

When either [mtvec.MODE](#) or [mtvec.BASE](#) is illegal, [mtvec](#) will retain its current value

custom

When either [mtvec.MODE](#) or [mtvec.BASE](#) is illegal, [mtvec](#) will obtain an unpredictable value

Other values may be added over time once other common behaviors are identified.

MTVEC_MODES ⇒ 1-element to 2-element array of [0, 1]

Options:

0

Direct; All traps set [pc](#) to [mtvec.BASE](#)

1

Vectored; Asynchronous interrupts set [pc](#) to [mtvec.BASE](#) + 4 x cause.

If only one mode is given, [mtvec.MODE](#) is assumed to be read-only with that value. Otherwise, [mtvec.MODE](#) is read-write.

M_MODE_ENDIANNESSE ⇒ [little, big, dynamic]

Options:

little	M-mode data is always little endian
big	M-mode data is always big endian
dynamic	M-mode data can be either little or big endian, depending on the CSR field mstatus.MBE

PHYS_ADDR_WIDTH ⇒ 1 to 64

Implementation-defined size of the physical address space.

PMA_GRANULARITY ⇒ 2 to 66

Generally, for systems with an MMU, should not be smaller than 12, as that would preclude caching PMA results in the TLB along with virtual memory translations

PRECISE_SYNCHRONOUS_EXCEPTIONS ⇒ boolean

If false, any exception not otherwise mandated to precise (e.g., PMP violation) will cause execution to enter an unpredictable state.

REPORT_ENCODING_IN_MTVAL_ON_ILLEGAL_INSTRUCTION ⇒ boolean

Options:

- true: [mtval](#) is written with the encoding of an instruction causing an `IllegalInstruction` exception
- false: [mtval](#) is written with 0 when an instruction causes an `IllegalInstruction` exception.

REPORT_VA_IN_MTVAL_ON_BREAKPOINT ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual PC of an `EBREAK` instruction (same information as [mepc](#)).
- false: [mtval](#) is written with 0 on an `EBREAK` instruction.

Regardless, [mtval](#) is always written with a virtual PC when an external breakpoint is generated

REPORT_VA_IN_MTVAL_ON_INSTRUCTION_ACCESS_FAULT ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a fetch causing the access fault
- false: [mtval](#) is written with 0 when a fetch causes an access fault

REPORT_VA_IN_MTVAL_ON_INSTRUCTION_MISALIGNED ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a trapping misaligned fetch
- false: [mtval](#) is written with 0 when a misaligned fetch traps

REPORT_VA_IN_MTVAL_ON_LOAD_ACCESS_FAULT ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a load causing the access fault
- false: [mtval](#) is written with 0 when a load causes an access fault

REPORT_VA_IN_MTVAL_ON_LOAD_MISALIGNED ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a trapping misaligned load.
- false: [mtval](#) is written with 0 when a misaligned load traps.

REPORT_VA_IN_MTVAL_ON_STORE_AMO_ACCESS_FAULT ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a store or AMO causing the access fault
- false: [mtval](#) is written with 0 when a store or AMO causes an access fault

REPORT_VA_IN_MTVAL_ON_STORE_AMO_MISALIGNED ⇒ boolean

Options:

- true: [mtval](#) is written with the virtual address of a trapping misaligned store or AMO.
- false: [mtval](#) is written with 0 when a misaligned store or AMO traps.

TRAP_ON_EBREAK ⇒ boolean

The spec states that implementations may handle `EBREAK`s transparently without raising a trap, in which case the EEI must provide a builtin.

TRAP_ON_ECALL_FROM_M ⇒ boolean

The spec states that implementations may handle `ECALL`s transparently without raising a trap, in which case the EEI must provide a builtin.

TRAP_ON_ILLEGAL_WLRL ⇒ boolean

Options:

- true: Writing an illegal value to a `WLRL` CSR field will cause an `IllegalInstruction` exception.
- false: Writing an illegal value to a `WLRL` CSR field causes unpredictable behavior.

TRAP_ON_RESERVED_INSTRUCTION ⇒ boolean

Options:

- true: Fetching an unimplemented and/or undefined instruction from the standard/reserved opcode space will cause an `IllegalInstruction`

exception.

- false: Fetching an unimplemented and/or undefined instruction from the standard/reserved opcode space causes unpredictable behavior.

TRAP_ON_RESERVED_INSTRUCTION may be false while TRAP_ON_UNIMPLEMENTED_INSTRUCTION is true when a custom instruction is implemented in the standard/reserved opcode space.

TRAP_ON_UNIMPLEMENTED_CSR ⇒ **boolean**

- Options:
- true: Accessing an unimplemented CSR (via a [Zicsr](#) instruction) will cause an IllegalInstruction exception.
 - false: Accessing an unimplemented CSR (via a [Zicsr](#) instruction) will cause unpredictable behavior.

TRAP_ON_UNIMPLEMENTED_INSTRUCTION ⇒ **boolean**

- Options:
- true: Fetching an unimplemented instruction will cause an IllegalInstruction exception.
 - false: Fetching an unimplemented instruction causes unpredictable behavior.

An unimplemented instruction is any instruction encoding that is not defined by the implementation. Custom instructions are considered implemented.

VENDOR_ID_BANK ⇒ **25-bit integer**

Encodes the number of one-byte continuation codes in the Bank field of [mvendorid](#).

in JEDEC’s parlance, the bank number is one greater than the number of continuation codes; hence, the mvendorid Bank field encodes a value that is one less than the JEDEC bank number.

VENDOR_ID_OFFSET ⇒ **7-bit integer**

Encodes the final byte of a JEDEC manufactor ID, discarding the parity bit.

A.12. Extension Smpmp

Long Name: Physical Memory Protection
Version Requirement: ~> 1.13

A.12.1. Available Versions

Version 1.11.0	
State	ratified
Ratification date	2019-12
Changes	• Made the unused pmpaddr and pmpcfg fields WARL, rather than WIRI. • Specified semantics for PMP regions coarser than four bytes.
Version 1.12.0	
State	ratified
Ratification date	2021-12
Changes	• PMP changes require an SFENCE.VMA on any hart that implements page-based virtual memory, even if VM is not currently enabled. • PMP reset values are now platform-defined. • An additional 48 optional PMP registers have been defined.
Version 1.13.0	
State	frozen

A.12.2. Synopsis

To support secure processing and contain faults, it is desirable to limit the physical addresses accessible by software running on a hart. The optional PMP (Physical Memory Protection) unit provides per-hart machine-mode control registers to allow physical memory access privileges (read, write, execute) to be specified for each physical memory region. The PMP values are checked in parallel with the PMA checks.



This is a placeholder extension name defined by the [riscv-unified-db](#) and isn’t considered an extension in the Privileged ISA manual. This was chosen as an extension rather than a M-mode parameter since the PMP has no visible ISA features (such as read-only-0 CSRs) if not present in an implementation. Making it an extension in the database prevents having the PMP CSRs show up in implementations that don’t have a PMP.

A.12.3. CSRs

The following 72 CSRs are added by extension version 1.11.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
pmpaddr0	PMP Address 0	0x3b0	M
pmpaddr1	PMP Address 1	0x3b1	M
pmpaddr10	PMP Address 10	0x3ba	M
pmpaddr11	PMP Address 11	0x3bb	M
pmpaddr12	PMP Address 12	0x3bc	M
pmpaddr13	PMP Address 13	0x3bd	M
pmpaddr14	PMP Address 14	0x3be	M
pmpaddr15	PMP Address 15	0x3bf	M
pmpaddr16	PMP Address 16	0x3c0	M
pmpaddr17	PMP Address 17	0x3c1	M
pmpaddr18	PMP Address 18	0x3c2	M
pmpaddr19	PMP Address 19	0x3c3	M
pmpaddr2	PMP Address 2	0x3b2	M
pmpaddr20	PMP Address 20	0x3c4	M
pmpaddr21	PMP Address 21	0x3c5	M
pmpaddr22	PMP Address 22	0x3c6	M
pmpaddr23	PMP Address 23	0x3c7	M
pmpaddr24	PMP Address 24	0x3c8	M
pmpaddr25	PMP Address 25	0x3c9	M
pmpaddr26	PMP Address 26	0x3ca	M
pmpaddr27	PMP Address 27	0x3cb	M
pmpaddr28	PMP Address 28	0x3cc	M
pmpaddr29	PMP Address 29	0x3cd	M
pmpaddr3	PMP Address 3	0x3b3	M
pmpaddr30	PMP Address 30	0x3ce	M
pmpaddr31	PMP Address 31	0x3cf	M
pmpaddr32	PMP Address 32	0x3d0	M
pmpaddr33	PMP Address 33	0x3d1	M
pmpaddr34	PMP Address 34	0x3d2	M
pmpaddr35	PMP Address 35	0x3d3	M
pmpaddr36	PMP Address 36	0x3d4	M
pmpaddr37	PMP Address 37	0x3d5	M
pmpaddr38	PMP Address 38	0x3d6	M
pmpaddr39	PMP Address 39	0x3d7	M
pmpaddr4	PMP Address 4	0x3b4	M
pmpaddr40	PMP Address 40	0x3d8	M
pmpaddr41	PMP Address 41	0x3d9	M
pmpaddr42	PMP Address 42	0x3da	M
pmpaddr43	PMP Address 43	0x3db	M
pmpaddr44	PMP Address 44	0x3dc	M
pmpaddr45	PMP Address 45	0x3dd	M
pmpaddr46	PMP Address 46	0x3de	M
pmpaddr47	PMP Address 47	0x3df	M
pmpaddr48	PMP Address 48	0x3e0	M
pmpaddr49	PMP Address 49	0x3e1	M
pmpaddr5	PMP Address 5	0x3b5	M
pmpaddr50	PMP Address 50	0x3e2	M

Name	Long Name	Address	Mode
pmpaddr51	PMP Address 51	0x3e3	M
pmpaddr52	PMP Address 52	0x3e4	M
pmpaddr53	PMP Address 53	0x3e5	M
pmpaddr54	PMP Address 54	0x3e6	M
pmpaddr55	PMP Address 55	0x3e7	M
pmpaddr56	PMP Address 56	0x3e8	M
pmpaddr57	PMP Address 57	0x3e9	M
pmpaddr58	PMP Address 58	0x3ea	M
pmpaddr59	PMP Address 59	0x3eb	M
pmpaddr6	PMP Address 6	0x3b6	M
pmpaddr60	PMP Address 60	0x3ec	M
pmpaddr61	PMP Address 61	0x3ed	M
pmpaddr62	PMP Address 62	0x3ee	M
pmpaddr63	PMP Address 63	0x3ef	M
pmpaddr7	PMP Address 7	0x3b7	M
pmpaddr8	PMP Address 8	0x3b8	M
pmpaddr9	PMP Address 9	0x3b9	M
pmpcfg0	PMP Configuration Register 0	0x3a0	M
pmpcfg10	PMP Configuration Register 10	0x3aa	M
pmpcfg12	PMP Configuration Register 12	0x3ac	M
pmpcfg14	PMP Configuration Register 14	0x3ae	M
pmpcfg2	PMP Configuration Register 2	0x3a2	M
pmpcfg4	PMP Configuration Register 4	0x3a4	M
pmpcfg6	PMP Configuration Register 6	0x3a6	M
pmpcfg8	PMP Configuration Register 8	0x3a8	M

A.12.4. OUT-OF-SCOPE Parameters

NUM_PMP_ENTRIES ⇒ 0 to 64

Number of implemented PMP entries. Can be any value between 0-64, inclusive.

The architecture mandates that the number of implemented PMP registers must appear to be 0, 16, or 64.

Therefore, pmp registers will behave as follows according to NUN_PMP_ENTRIES:

NUM_PMP_ENTRIES	pmpaddr<0-15> / pmpcfg<0-3>	pmpaddr<16-63> / pmpcfg<4-15>
0	N	N
1-16	Y	N
17-64	Y	Y

- N = Not implemented; access will cause *IllegalInstruction* if TRAP_ON_UNIMPLEMENTED_CSR is true
- Y = Implemented; access will not cause an exception (from M-mode), but register may be read-only-zero if NUM_PMP_ENTRIES is less than the corresponding register



pmpcfgN for an odd N never exists when XLEN == 64

When NUM_PMP_ENTRIES is not exactly 0, 16, or 64, some extant pmp registers, and associated pmpNcfg, will be read-only zero (but will never cause an exception).

PMP_GRANULARITY ⇒ 2 to 66

log2 of the smallest supported PMP region.

Generally, for systems with an MMU, should not be smaller than 12, as that would preclude caching PMP results in the TLB along with virtual memory translations

Note that PMP_GRANULARITY is equal to G+2 (not G) as described in the privileged architecture.

A.13. Extension Ssccptr

Long Name: Cacheable and coherent main memory page table reads
Version Requirement: ~> 1.0

A.13.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03
Ratification document	github.com/riscv/riscv-profiles/releases/tag/v1.0

A.13.2. Synopsis

Main memory regions with both the cacheability and coherence PMAs must support hardware page-table reads.

-  This extension was ratified with the RVA20 profiles.
-  Main memory regions with both the cacheability and coherence PMAs must support hardware page-table reads

A.14. Extension Sscofpmf

Long Name: Counter Overflow and Privilege Mode Filtering
Version Requirement: ~> 1.0

A.14.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-08
Ratification document	drive.google.com/file/d/1KcjgbLM5L1ZKY8934aJl8aQwGIMz6Cbo/view?usp=drive_link

A.14.2. Synopsis

Counter Overflow and Privilege Mode Filtering

-  Count overflow and mode-based filtering. Platforms may choose to mandate the presence of Sscofpmf.

A.14.3. CSRs

The following 1 CSRs are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
scountovf	Supervisor Count Overflow	0xda0	S

A.15. Extension Sscounterenw

Long Name: Support writeable enables for any supported counter
Version Requirement: ~> 1.0

A.15.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-08
Ratification document	drive.google.com/file/d/1KcjgbLM5L1ZKY8934aJl8aQwGIMz6Cbo/view?usp=drive_link

A.15.2. Synopsis

For any hpmcounter that is not read-only zero, the corresponding bit in [scounteren](#) must be writable.

-  This extension was ratified with the RVA22 profiles.



For any **hpmcounter** that is not read-only zero, the corresponding bit in **scounteren** must be writable.

A.16. Extension Ssnpm

Long Name: Pointer masking for next privilege level less than S-mode

Version Requirement: ~> 1.0

A.16.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-10

A.16.2. Synopsis

A supervisor-level extension that provides pointer masking for the next lower privilege mode (U-mode), and for VS-modes and VU-modes if the H extension is present.



Pointer masking, with **senvcfg**.PME supporting, at minimum, settings PMLEN=0 and PMLEN=7

A.16.3. OUT-OF-SCOPE Parameters

PMLen ⇒ **integer**

The number of high-order bits of an address that are masked by the pointer masking facility.

A.17. Extension Sspm

Long Name: Pointer masking available in supervisor mode

Version Requirement: ~> 1.0

A.17.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-10

A.17.2. Synopsis

Indicates that there is pointer-masking support available in supervisor mode, with some facility provided in the application execution environment to control pointer masking.

This extension describes an execution environment but has no bearing on hardware implementations. It is intended to be used in profile specifications where a Supervisor profile can only reference Supervisor level pointer masking functionality, and not the associated CSR controls that exist at a higher privilege level (i.e., in the execution environment).



Supervisor-mode pointer masking, with the supervisor execution environment providing a means to select PMLEN=0 and PMLEN=7 (at minimum).

A.18. Extension Ssstrict

Long Name: Unimplemented reserved encodings trap and no non-conforming extensions

Version Requirement: ~> 1.0

A.18.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-10

A.18.2. Synopsis

No non-conforming extensions are present. Attempts to execute unimplemented opcodes or access unimplemented CSRs in the standard or reserved encoding spaces raises an illegal instruction exception that results in a contained trap to the supervisor-mode trap handler.



Ssstrict does not prescribe behavior for the custom encoding spaces or CSRs.

	Ssstrict definition applies to the execution environment claiming to be RVA23/RVB23-compatible. If the hypervisor extension is present, that execution environment will take a contained trap to supervisor-mode (however that trap is implemented, including, but not limited to, emulation/delegation in the outer execution environment). Ssstrict (and all the other RVA23/RVB23 mandates and options) do not apply to any guest VMs run by a hypervisor. An RVA23/RVB23 hypervisor can provide guest VMs that are also RVA23/RVB23-compatible but with an expanded set of emulated standard instructions. An RVA23/RVB23 hypervisor can also choose to implement guest VMs that are not RVA23/RVB23 compatible (e.g., lacking H, or only RVA20).
	Ssstrict is a new RVA23/RVB23 profile-defined extension that restricts the behavior of reserved encoding spaces. The extension will be added to the supervisor chapter of the privileged architecture.
	No non-conforming extensions are present. Attempts to execute unimplemented opcodes or access unimplemented CSRs in the standard or reserved encoding spaces raises an illegal instruction exception that results in a contained trap to the supervisor-mode trap handler
	 Ssstrict does not prescribe behavior for the custom encoding spaces or CSRs.
	 Ssstrict definition applies to the execution environment claiming to be RVB23-compatible, which must have the hypervisor extension. That execution environment will take a contained trap to supervisor-mode (however that trap is implemented, including, but not limited to, emulation/delegation in the outer execution environment). Ssstrict (and all the other RVB23 mandates and options) do not apply to any guest VMs run by a hypervisor. An RVB23 hypervisor can provide guest VMs that are also RVB23-compatible but with an expanded set of emulated standard instructions. An RVB23 hypervisor can also choose to implement guest VMs that are not RVB23 compatible (for example, only RVA20 or only RVA22)

A.19. Extension Sstc

Long Name: Supervisor-mode timer interrupts
Version Requirement: ~> 1.0

A.19.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-03
Ratification document	drive.google.com/file/d/1m84Re2yK8m_vbW7TspvevCDR82MOBaSX/view?usp=drive_link

A.19.2. Synopsis

Supervisor-mode timer interrupts

	Supervisor-mode timer interrupts.
	Sstc was not made mandatory in RVB23S64 as it is a more disruptive change affecting system-level architecture, and will take longer for implementations to adopt. It is expected to be made mandatory in the next profile release.

A.20. Extension Sstvala

Long Name: Supervisor Trap Value provides all needed values
Version Requirement: ~> 1.0

A.20.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03
Ratification document	github.com/riscv/riscv-profiles/releases/tag/v1.0

A.20.2. Synopsis

[stval](#) must be written with the faulting virtual address for load, store, and instruction page-fault, access-fault, and misaligned exceptions, and for breakpoint exceptions other than those caused by execution of the [ebreak](#) or ``c.ebreak` instructions.

For virtual-instruction and illegal-instruction exceptions, [stval](#) must be written with the faulting instruction.



This extension was ratified with the RVA20 profiles.



stval must be written with the faulting virtual address for load, store, and instruction page-fault, access-fault, and misaligned exceptions, and for breakpoint exceptions other than those caused by execution of the EBREAK or C.EBREAK instructions. For virtual-instruction and illegal instruction exceptions, **stval** must be written with the faulting instruction .

A.21. Extension Sstvecd

Long Name: Direct exception vectoring

Version Requirement: ~> 1.0

A.21.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03
Ratification document	github.com/riscv/riscv-profiles/releases/tag/v1.0

A.21.2. Synopsis

stvec.MODE must be capable of holding the value 0 (Direct). When **stvec.MODE**=Direct, **stvec.BASE** must be capable of holding any valid four-byte-aligned address.



stvec.MODE must be capable of holding the value 0 (Direct). When **stvec.MODE**=Direct, **stvec.BASE** must be capable of holding any valid four-byte-aligned address

A.22. Extension Ssu64xl

Long Name: 64-bit UXLEN

Version Requirement: ~> 1.0

A.22.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.22.2. Synopsis

sstatus.UXL must be capable of holding the value 2 (i.e., UXLEN=64 must be supported).



This extension is defined by RVA22.



sstatus.UXL must be capable of holding the value 2 (that is, UXLEN=64 must be supported)

A.23. Extension Supm

Long Name: Pointer masking available in user mode

Version Requirement: ~> 1.0

A.23.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-10

A.23.2. Synopsis

Indicates that there is pointer-masking support available in user mode, with some facility provided in the application execution environment to control pointer masking.

This extension describes an execution environment but has no bearing on hardware implementations. It is intended to be used in profile specifications where a User profile can only reference User level pointer masking functionality, and not the associated CSR controls that exist at a higher privilege level (i.e., in the execution environment).



Pointer masking, with the execution environment providing a means to select PMLen=0 and PMLen=7 at minimum

A.24. Extension Sv39

Long Name: 39-bit virtual address translation (3 level)

Version Requirement: ~> 1.0

A.24.1. Available Versions

Version 1.11.0	
State	ratified
Ratification date	2019-05
Version 1.12.0	
State	ratified
Ratification date	2021-12
Ratification document	github.com/riscv/riscv-isa-manual/releases/download/Priv-v1.12/riscv-privileged-20211203.pdf
Version 1.13.0	
State	ratified
Ratification date	2024-10

A.24.2. Synopsis

39-bit virtual address translation (3 level)



Page-Based 39-bit Virtual-Memory System

A.25. Extension Sv48

Long Name: 48-bit virtual address translation (4 level)

Version Requirement: ~> 1.13

A.25.1. Available Versions

Version 1.11.0	
State	ratified
Ratification date	2019-05
Version 1.12.0	
State	ratified
Ratification date	2021-12
Ratification document	github.com/riscv/riscv-isa-manual/releases/download/Priv-v1.12/riscv-privileged-20211203.pdf
Version 1.13.0	
State	ratified
Ratification date	2024-10

A.25.2. Synopsis

48-bit virtual address translation (4 level)



Page-based 48-bit virtual-memory system

A.26. Extension Sv57

Long Name: 57-bit virtual address translation (5 level)

Version Requirement: ~> 1.13

A.26.1. Available Versions

Version 1.11.0	
State	ratified
Version 1.12.0	
State	ratified
Ratification date	2021-12
Ratification document	github.com/riscv/riscv-isa-manual/releases/download/Priv-v1.12/riscv-privileged-20211203.pdf
Version 1.13.0	
State	ratified
Ratification date	2024-10

A.26.2. Synopsis

57-bit virtual address translation (5 level)



Page-based 57-bit virtual-memory system

A.27. Extension Svade

Long Name: Exception on PTE A/D Bits
Version Requirement: ~> 1.0

A.27.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-11
Ratification document	github.com/riscvarchive/riscv-svadu/releases/download/v1.0/riscv-svadu.pdf

A.27.2. Synopsis

The Svade extension indicates that hardware does **not** update the A/D bits of a page table during a page walk. Rather, encountering a PTE with the A bit clear or the D bit clear when an operation is a write will cause a Page Fault.



A page-fault exception is raised when a page is accessed when A bit = 0 , or when a page is written when D bit = 0

A.28. Extension Svadu

Long Name: Hardware Updating of PTE A/D Bits
Version Requirement: ~> 1.0

A.28.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-11
Ratification document	github.com/riscvarchive/riscv-svadu/releases/download/v1.0/riscv-svadu.pdf

A.28.2. Synopsis

The Svadu extension adds support and CSR controls for hardware updating of PTE A/D bits. The A and D bits are managed by these extensions as follows:

- When a virtual page is accessed and the A bit is clear, the PTE is updated to set the A bit. When the virtual page is written and the D bit is clear, the PTE is updated to set the D bit. When G-stage address translation is in use and is not Bare, the G-stage virtual pages may be accessed or written by implicit accesses to VS-level memory management data structures, such as page tables.
- When two-stage address translation is in use, an explicit access may cause both VS-stage and G-stage PTEs to be updated. The following rules apply to all PTE updates caused by an explicit or an implicit memory accesses.

The PTE update must be atomic with respect to other accesses to the PTE, and must atomically perform all tablewalk checks for that leaf PTE as part of, and before, conditionally updating the PTE value. Updates of the A bit may be performed as a result of speculation, even if the associated memory access ultimately is not performed architecturally. However, updates to the D bit, resulting from an explicit store, must be exact (i.e.,

non-speculative), and observed in program order by the local hart. When two-stage address translation is active, updates of the D bit in G-stage PTEs may be performed as a result of speculative updates of the A bit in VS-stage PTEs.

The PTE update must appear in the global memory order before the memory access that caused the PTE update and before any subsequent explicit memory access to that virtual page by the local hart. The ordering on loads and stores provided by FENCE instructions and the acquire/release bits on atomic instructions also orders the PTE updates associated with those loads and stores as observed by remote harts.

The PTE update is not required to be atomic with respect to the memory access that caused the update and a trap may occur between the PTE update and the memory access that caused the PTE update. If a trap occurs then the A and/or D bit may be updated but the memory access that caused the PTE update might not occur. The hart must not perform the memory access that caused the PTE update before the PTE update is globally visible.



The PTE updates due to memory accesses ordered-after a FENCE are not themselves ordered by the FENCE.

Simpler implementations that cannot precisely order the PTE update before subsequent explicit memory accesses to the associated virtual page by the local hart may simply order the PTE update before all subsequent explicit memory accesses to any virtual page by the local hart.

Svadu extension requires the page tables to be located in memory with hardware page-table write access and *RsrvEventual* PMA.

The translation of virtual addresses (or guest physical addresses) to physical (or guest physical) addresses is accomplished with the same algorithm as specified in the Supervisor-Level ISA extension (section "Virtual Address Translation Process") and as modified by the hypervisor extension (section "Two-stage Address Translation"), except that step 7 of the translation process, instead of causing a page-fault exception due to A and/or D bits being 0 when required to be 1, continues as follows:

7. If `pte.a = 0`, or if the original memory access is a store and `pte.d = 0`:
- a. If a store to `pte` would violate a PMA or PMP check, raise an access-fault exception corresponding to the original access type.

b. Perform the following steps atomically:

i. Compare `pte` to the value of the PTE at address `a + va.vpn[i] * PTESIZE`.

ii. If the values match, set `pte.a` to 1 and, if the original memory access is a store, also set `pte.d` to 1.

iii. If the comparison fails, return to step 2
- The Svadu extension adds the `ADUE` bit (bit 61) to `menvcfg`. When `menvcfg.ADUE` is 1, hardware updating of PTE A/D bits is enabled during single-stage address translation. When the hypervisor extension is implemented, if `menvcfg.ADUE` is 1, hardware updating of PTE A/D bits is enabled during G-stage address translation. When `menvcfg.ADUE` is zero, the implementation behaves as though Svadu were not implemented. If Svadu is not implemented, `menvcfg.ADUE` is read-only zero. Furthermore, for implementations with the hypervisor extension, `henvcfg.ADUE` is read-only zero if `menvcfg.ADUE` is zero.
- When the hypervisor extension is implemented, the Svadu extension adds the `ADUE` bit (bit 61) to `henvcfg`. When `henvcfg.ADUE` is 1, hardware updating of PTE A/D bits is enabled during VS-stage address translation. When `henvcfg.ADUE` is zero, the implementation behaves as though Svadu were not implemented for VS-stage address translation.
- 

Hardware A/D bit updates
- ## A.29. Extension Svbare
- Long Name:** Bare virtual addressing
Version Requirement: ~> 1.0
- ### A.29.1. Available Versions
Version 1.0.0	
State	ratified
Ratification date	2023-03
- ### A.29.2. Synopsis
- This extension mandates that the `satp` mode Bare must be supported.
- 

This extension was ratified as part of the RVA22 profile.



The `satp` mode Bare must be supported
- ## A.30. Extension Svinval
- Long Name:** Fine-grained address-translation cache invalidation
Version Requirement: ~> 1.0
- ### A.30.1. Available Versions
Version 1.0.0	
State	ratified
Ratification date	2021-11
- ### A.30.2. Synopsis
- The `Svinval` extension splits `sfence.vma`, `hfence.vma`, and `hfence.gvma` instructions into finer-grained invalidation and ordering operations that can be more efficiently batched or pipelined on certain classes of high-performance implementation.
- The `sinval.vma` instruction invalidates any address-translation cache entries that an `sfence.vma` instruction with the same values of rs1 and rs2 would invalidate. However, unlike `sfence.vma`, `sinval.vma` instructions are only ordered with respect to `sfence.vma`, `sfence.w.inval`, and `sfence.inval.ir` instructions as defined below.
- The `sfence.w.inval` instruction guarantees that any previous stores already visible to the current RISC-V hart are ordered before subsequent `sinval.vma` instructions executed by the same hart. The `sfence.inval.ir` instruction guarantees that any previous `sinval.vma` instructions executed by the current hart are ordered before subsequent implicit references by that hart to the memory-management data structures.
- 52

When executed in order (but not necessarily consecutively) by a single hart, the sequence `sfence.w.inval`, `sinval.vma`, and `sfence.inval.ir` has the same effect as a hypothetical `sfence.vma` instruction in which:

- the values of `rs1` and `rs2` for the `sfence.vma` are the same as those used in the `sinval.vma`,
- reads and writes prior to the `sfence.w.inval` are considered to be those prior to the `sfence.vma`, and
- reads and writes following the `sfence.inval.ir` are considered to be those subsequent to the `sfence.vma`.

If the hypervisor extension is implemented, the `Svinval` extension also provides two additional instructions: `hinval.vvma` and `hinval.gvma`. These have the same semantics as `sinval.vma`, except that they combine with `sfence.w.inval` and `sfence.inval.ir` to replace `hfence.vvma` and `hfence.gvma`, respectively, instead of `sfence.vma`. In addition, `hinval.gvma` uses VMIDs instead of ASIDs.

`sinval.vma`, `hinval.vvma`, and `hinval.gvma` require the same permissions and raise the same exceptions as `sfence.vma`, `hfence.vvma`, and `hfence.gvma`, respectively. In particular, an attempt to execute any of these instructions in U-mode always raises an `IllegalInstruction` exception, and an attempt to execute `sinval.vma` or `hinval.gvma` in S-mode or HS-mode when `mstatus.TVM`=1 also raises an `IllegalInstruction` exception. An attempt to execute `hinval.vvma` or `hinval.gvma` in VS-mode or VU-mode, or to execute `sinval.vma` in VU-mode, raises a `VirtualInstruction` exception. When `hstatus.VTVM`=1, an attempt to execute `sinval.vma` in VS-mode also raises a `VirtualInstruction` exception.

Attempting to execute `sfence.w.inval` or `sfence.inval.ir` in U-mode raises an `IllegalInstruction` exception. Doing so in VU-mode raises a `VirtualInstruction` exception. `sfence.w.inval` and `sfence.inval.ir` are unaffected by the `mstatus.TVM` and `hstatus.VTVM` fields and hence are always permitted in S-mode and VS-mode.

i

`sfence.w.inval` and `sfence.inval.ir` instructions do not need to be trapped when `mstatus.TVM`=1 or when `hstatus.VTVM`=1, as they only have ordering effects but no visible side effects. Trapping of the `sinval.vma` instruction is sufficient to enable emulation of the intended overall TLB maintenance functionality.

In typical usage, software will invalidate a range of virtual addresses in the address-translation caches by executing an `sfence.w.inval` instruction, executing a series of `sinval.vma`, `hinval.vvma`, or `hinval.gvma` instructions to the addresses (and optionally ASIDs or VMIDs) in question, and then executing an `sfence.inval.ir` instruction.

High-performance implementations will be able to pipeline the address-translation cache invalidation operations, and will defer any pipeline stalls or other memory ordering enforcement until an `sfence.w.inval`, `sfence.inval.ir`, `sfence.vma`, `hfence.gvma`, or `hfence.vvma` instruction is executed.

Simpler implementations may implement `sinval.vma`, `hinval.vvma`, and `hinval.gvma` identically to `sfence.vma`, `hfence.vvma`, and `hfence.gvma`, respectively, while implementing `sfence.w.inval` and `sfence.inval.ir` instructions as no-ops.

i

Fine-grained address-translation cache invalidation

A.30.3. Instructions

The following 3 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

<code>sfence.inval.ir</code>	Order implicit page table reads after invalidation
<code>sfence.w.inval</code>	Order writes before sfence
<code>sinval.vma</code>	Invalidate cached address translations

A.31. Extension Svnapot

Long Name: Naturally Aligned Power-of-Two Translation Contiguity
Version Requirement: ~> 1.0

A.31.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-11

A.31.2. Synopsis

In Sv39, Sv48, and Sv57, when a PTE has N=1, the PTE represents a translation that is part of a range of contiguous virtual-to-physical translations with the same values for PTE bits 5-0. Such ranges must be of a naturally aligned power-of-2 (NAPOT) granularity larger than the base page size.

The Svnapot extension depends on Sv39.

Table 9. Page table entry encodings when pte.N=1

i	<i>pte.ppn[i]</i>	Description	<i>pte.napot_bits</i>
0	x xxxx xxx1	Reserved	-
0	x xxxx xx1x	Reserved	-
0	x xxxx x1xx	Reserved	-
0	x xxxx 1000	64 KiB contiguous region	4
0	x xxxx 0xxx	Reserved	-
≥1	x xxxx xxxx	Reserved	-

NAPOT PTEs behave identically to non-NAPOT PTEs within the address-translation algorithm in [\[sv32algorithm\]](#), except that:

- If the encoding in *pte* is valid according to [Table 9](#), then instead of returning the original value of *pte*, implicit reads of a NAPOT PTE return a copy of *pte* in which *pte.ppn[i][pte.napot_bits-1:0]* is replaced by *vpn[i][pte.napot_bits-1:0]*. If the encoding in *pte* is reserved according to [Table 9](#), then a page-fault exception must be raised.
- Implicit reads of NAPOT page table entries may create address-translation cache entries mapping $a + j \cdot \text{PTESIZE}$ to a copy of *pte* in which *pte.ppn[i][pte.napot_bits-1:0]* is replaced by *vpn[i][pte.napot_bits-1:0]*, for any or all j such that $j \gg \text{napot\_bits} = \text{vpn}[i] \gg \text{napot\_bits}$, all for the address space identified in *satp* as loaded by step 1.

The motivation for a NAPOT PTE is that it can be cached in a TLB as one or more entries representing the contiguous region as if it were a single (large) page covered by a single translation. This compaction can help relieve TLB pressure in some scenarios. The encoding is designed to fit within the pre-existing Sv39, Sv48, and Sv57 PTE formats so as not to disrupt existing implementations or designs that choose not to implement the scheme. It is also designed so as not to complicate the definition of the address-translation algorithm.

The address translation cache abstraction captures the behavior that would result from the creation of a single TLB entry covering the entire NAPOT region. It is also designed to be consistent with implementations that support NAPOT PTEs by splitting the NAPOT region into TLB entries covering any smaller power-of-two region sizes. For example, a 64 KiB NAPOT PTE might trigger the creation of 16 standard 4 KiB TLB entries, all with contents generated from the NAPOT PTE (even if the PTEs for the other 4 KiB regions have different contents).

In typical usage scenarios, NAPOT PTEs in the same region will have the same attributes, same PPNs, and same values for bits 5-0. RSW remains reserved for supervisor software control. It is the responsibility of the OS and/or hypervisor to configure the page tables in such a way that there are no inconsistencies between NAPOT PTEs and other NAPOT or non-NAPOT PTEs that overlap the same address range. If an update needs to be made, the OS generally should first mark all of the PTEs invalid, then issue SFENCE.VMA instruction(s) covering all 4 KiB regions within the range (either via a single SFENCE.VMA with `rs1<em>rs1</em>=<code>x0</code>`, or with multiple SFENCE.VMA instructions with `rs1<em>rs1</em>=<code>x0</code>`), then update the PTE(s), as described in [\[sfence.vma\]](#), unless any inconsistencies are known to be benign. If any inconsistencies do exist, then the effect is the same as when SFENCE.VMA is used incorrectly: one of the translations will be chosen, but the choice is unpredictable.

If an implementation chooses to use a NAPOT PTE (or cached version thereof), it might not consult the PTE directly specified by the algorithm in [\[sv32algorithm\]](#) at all. Therefore, the D and A bits may not be identical across all mappings of the same address range even in typical use cases. The operating system must query all NAPOT aliases of a page to determine whether that page has been accessed and/or is dirty. If the OS manually sets the A and/or D bits for a page, it is recommended that the OS also set the A and/or D bits for other NAPOT aliases as appropriate in order to avoid unnecessary traps.

Just as with normal PTEs, TLBs are permitted to cache NAPOT PTEs whose V (Valid) bit is clear.

Depending on need, the NAPOT scheme may be extended to other intermediate page sizes and/or to other levels of the page table in the future. The encoding is designed to accommodate other NAPOT sizes should that need arise. For example:

i	<i>pte.ppn[i]</i>	Description	<i>pte.napot_bits</i>
0	x xxxx xxx1	8 KiB contiguous region	1
0	x xxxx xx10	16 KiB contiguous region	2
0	x xxxx x100	32 KiB contiguous region	3
0	x xxxx 1000	64 KiB contiguous region	4
0	x xxx1 0000	128 KiB contiguous region	5
...	...	...	...
1	x xxxx xxx1	4 MiB contiguous region	1
1	x xxxx xx10	8 MiB contiguous region	2
...	...	...	...

In such a case, an implementation may or may not support all options. The discoverability mechanism for this extension would be extended to allow system software to determine which sizes are supported.

Other sizes may remain deliberately excluded, so that PPN bits not being used to indicate a valid NAPOT region size (e.g., the least-significant bit of *pte.ppn[i]*) may be repurposed for other uses in the future.

However, in case finer-grained intermediate page size support proves not to be useful, we have chosen to standardize only 64 KiB

	support as a first step.
	NAPOT translation contiguity. Svnapot is very low cost to provide, so is made mandatory even in RVB.

A.32. Extension Svpbmt

Long Name: Page-based memory types
Version Requirement: ~> 1.0

A.32.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-12

A.32.2. Synopsis

This extension mandates that the [satp](#) mode Bare must be supported.

	Page-based memory types

A.33. Extension Svptc

Long Name: Guarantee visibility of PTE transitions from invalid to valid
Version Requirement: ~> 1.0

A.33.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-06

A.33.2. Synopsis

When the Svptc extension is implemented, explicit stores by a hart that update the Valid bit of leaf and/or non-leaf PTEs from 0 to 1 and are visible to a hart will eventually become visible within a bounded timeframe to subsequent implicit accesses by that hart to such PTEs.

	Svptc relieves an operating system from executing certain memory-management instructions, such as SFENCE.VMA or SINVAL.VMA, which would normally be used to synchronize the hart’s address-translation caches when a memory-resident PTE is changed from Invalid to Valid. Synchronizing the hart’s address-translation caches with other forms of updates to a memory-resident PTE, including when a PTE is changed from Valid to Invalid, requires the use of suitable memory-management instructions. Svptc guarantees that a change to a PTE from Invalid to Valid is made visible within a bounded time, thereby making the execution of these memory-management instructions redundant. The performance benefit of eliding these instructions outweighs the cost of an occasional gratuitous additional page fault that may occur.+ Depending on the microarchitecture, some possible ways to facilitate implementation of Svptc include: not having any address-translation caches, not storing Invalid PTEs in the address-translation caches, automatically evicting Invalid PTEs using a bounded timer, or making address-translation caches coherent with store instructions that modify PTEs.
	Transitions from invalid to valid PTEs will be visible in bounded time without an explicit memory-management fence.

A.34. Extension U

Long Name: User-mode privilege level
Version Requirement: ~> 2.0

A.34.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2019-12

A.34.2. Synopsis

User-mode privilege level is supported by an implementation if the U extension is present. Note that the RISC-V ISA doesn’t formally define a U extension and it is only discussed in the Privileged ISA manual.

A.34.3. CSRs

The following 1 CSRs are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
mcounteren	Machine Counter Enable	0x306	M

A.34.4. OUT-OF-SCOPE Parameters

ASID_WIDTH ⇒ 0 to 16

Number of implemented ASID bits. Maximum is 16 for XLEN==64, and 9 for XLEN==32

MCOUNTENABLE_EN ⇒ 32-element array of boolean

Indicates which counters can be delegated via [mcounteren](#).

An unimplemented counter cannot be specified, i.e., if HPM_COUNTER_EN[3] is false, it would be illegal to set MCOUNTENABLE_EN[3] to true.

MCOUNTENABLE_EN[0:2] must all be false if [Zicntr](#) is not implemented. MCOUNTENABLE_EN[3:31] must all be false if [Zihpm](#) is not implemented.

MSTATUS_TVM_IMPLEMENTED ⇒ boolean

Whether or not mstatus.TVM is implemented.

When not implemented mstatus.TVM will be read-only-zero.

REPORT_ENCODING_IN_STVAL_ON_ILLEGAL_INSTRUCTION ⇒ boolean

When true, [stval](#) is written with the encoding of an instruction that causes an [IllegalInstruction](#) exception.

When false [stval](#) is written with 0 when an [IllegalInstruction](#) exception occurs.

REPORT_VA_IN_MTVAL_ON_INSTRUCTION_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionPageFault](#).

When false, [mtval](#) is written with 0 when an instruction fetch causes an [InstructionPageFault](#).

REPORT_VA_IN_MTVAL_ON_LOAD_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual address of a load when it causes a [LoadPageFault](#).

When false, [mtval](#) is written with 0 when a load causes a [LoadPageFault](#).

REPORT_VA_IN_MTVAL_ON_STORE_AMO_PAGE_FAULT ⇒ boolean

When true, [mtval](#) is written with the virtual address of a store when it causes a [StoreAmoPageFault](#).

When false, [mtval](#) is written with 0 when a store causes a [StoreAmoPageFault](#).

REPORT_VA_IN_STVAL_ON_BREAKPOINT ⇒ boolean

When true, [stval](#) is written with the virtual PC of the EBREAK instruction (same information as [mepc](#)).

When false, [stval](#) is written with 0 on an EBREAK instruction.

Regardless, [stval](#) is always written with a virtual PC when an external breakpoint is generated

REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionAccessFault](#).

When false, [stval](#) is written with 0 when an instruction fetch causes an [InstructionAccessFault](#).

REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED ⇒ boolean

When true, [stval](#) is written with the virtual PC when an instruction fetch is misaligned.

When false, [stval](#) is written with 0 when an instruction fetch is misaligned.

Note that when IALIGN=16 (i.e., when the [C](#) or one of the [Zc*](#) extensions are implemented), it is impossible to generate a misaligned fetch, and so this parameter has no effect.

REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual PC of an instructino when fetch causes an [InstructionPageFault](#).

When false, [stval](#) is written with 0 when an instruction fetch causes an [InstructionPageFault](#).

REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a load when it causes a [LoadAccessFault](#).

When false, [stval](#) is written with 0 when a load causes a [LoadAccessFault](#).

REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED ⇒ boolean

When true, [stval](#) is written with the virtual address of a load instruction when the address is misaligned and MISALIGNED_LDST is false.

When false, [stval](#) is written with 0 when a load address is misaligned and MISALIGNED_LDST is false.

REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a load when it causes a [LoadPageFault](#).

When false, [stval](#) is written with 0 when a load causes a [LoadPageFault](#).

REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a store when it causes a [StoreAmoAccessFault](#).

When false, [stval](#) is written with 0 when a store causes a [StoreAmoAccessFault](#).

REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED ⇒ boolean

When true, [stval](#) is written with the virtual address of a store instruction when the address is misaligned and MISALIGNED_LDST is false.

When false, [stval](#) is written with 0 when a store address is misaligned and MISALIGNED_LDST is false.

REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT ⇒ boolean

When true, [stval](#) is written with the virtual address of a store when it causes a [StoreAmoPageFault](#).

When false, [stval](#) is written with 0 when a store causes a [StoreAmoPageFault](#).

SATP_MODE_BARE ⇒ boolean

Whether or not satp.MODE == Bare is supported.

STVAL_WIDTH ⇒ ≤ 0xffffffffffffff

The number of implemented bits in [stval](#).

Must be greater than or equal to $\max(\text{PHYS\_ADDR\_WIDTH}, \text{VA\_SIZE})$

STVEC_MODE_DIRECT ⇒ boolean

Whether or not [stvec.MODE](#) supports Direct (0).

STVEC_MODE_VECTORED ⇒ boolean

Whether or not [stvec.MODE](#) supports Vectored (1).

SXLEN ⇒ 1-element to 2-element array of [32, 64]

Set of XLENs supported in S-mode. Can be one of:

- 32: SXLEN is always 32
- 64: SXLEN is always 64
- [32, 64]: SXLEN can be changed (via mstatus.SXL) between 32 and 64

S_MODE_ENDIANNESSE ⇒ [little, big, dynamic]

Endianness of data in S-mode. Can be one of:

- little: S-mode data is always little endian
- big: S-mode data is always big endian
- dynamic: S-mode data can be either little or big endian, depending on the CSR field [mstatus.SBE](#)

TRAP_ON_ECALL_FROM_S ⇒ boolean

Whether or not an ECALL-from-S-mode causes a synchronous exception.

The spec states that implementations may handle ECALLs transparently without raising a trap, in which case the EEI must provide a builtin.

TRAP_ON_ECALL_FROM_U ⇒ boolean

Whether or not an ECALL-from-U-mode causes a synchronous exception.

The spec states that implementations may handle ECALLs transparently without raising a trap, in which case the EEI must provide a builtin.

UXLEN ⇒ 1-element to 2-element array of [32, 64]

Set of XLENs supported in U-mode. When both 32 and 64 are supported, SXLEN can be changed, via mstatus.UXL, between 32 and 64.

U_MODE_ENDIANNESSE ⇒ [little, big, dynamic]

Endianness of data in U-mode. Can be one of:

- little: U-mode data is always little endian
- big: U-mode data is always big endian

- dynamic: U-mode data can be either little or big endian, depending on the CSR field [mstatus.UBE](#)

A.35. Extension V

Long Name: Vector Operations
Version Requirement: ~> 1.0

A.35.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-11

A.35.2. Synopsis

General support for data-parallel execution.



The Vector extension

A.36. Extension Za128rs

Long Name: Reservation set size of at most 128 bytes
Version Requirement: ~> 1.0

A.36.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.36.2. Synopsis

Reservation sets must be contiguous, naturally aligned, and at most 128 bytes in size.



This extension was ratified as part of the RVA20 profile.



The minimum reservation set size is effectively determined by the size of atomic accesses in the A extension.



Za128rs is a profile-defined extension introduced with RVA20. The minimum reservation set size is effectively determined by the size of atomic accesses in the [A](#) extension.

A.37. Extension Za64rs

Long Name: Reservation set size of at most 64 bytes
Version Requirement: ~> 1.0

A.37.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.37.2. Synopsis

Reservation sets must be contiguous, naturally aligned, and at most 64 bytes in size.



This extension was ratified as part of the RVA22 profile.



The minimum reservation set size is effectively determined by the size of atomic accesses in the A extension.



Reservation sets are contiguous, naturally aligned, and a maximum of 64 bytes

A.38. Extension Zawrs

Long Name: Wait-on-Reservation-Set Instructions
Version Requirement: ~> 1.0

A.38.1. Available Versions

Version 1.0.1	
State	ratified
Ratification date	2022-11

A.38.2. Synopsis

The [Zawrs](#) extension defines a pair of instructions to be used in polling loops that allows a core to enter a low-power state and wait on a store to a memory location. Waiting for a memory location to be updated is a common pattern in many use cases such as:

- Contenders for a lock waiting for the lock variable to be updated.
- Consumers waiting on the tail of an empty queue for the producer to queue work/data. The producer may be code executing on a RISC-V hart, an accelerator device, an external I/O agent.
- Code waiting on a flag to be set in memory indicative of an event occurring. For example, software on a RISC-V hart may wait on a "done" flag to be set in memory by an accelerator device indicating completion of a job previously submitted to the device.



Wait-on-reservation-set (WRS) instructions

A.38.3. Instructions

The following 2 instructions are added by extension version 1.0.1 (the minimum version of this extension that satisfies the extension requirement).

wrs.nto	Wait-on-Reservation-Set-with-No-Timeout
wrs.sto	Wait-on-Reservation-Set-with-Short-Timeout

A.39. Extension Zba

Long Name: Address generation
Version Requirement: ~> 1.0

A.39.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-06

A.39.2. Synopsis

The Zba instructions can be used to accelerate the generation of addresses that index into arrays of basic types (halfword, word, doubleword) using both unsigned word-sized and XLEN-sized indices: a shifted index is added to a base address.

The shift and add instructions do a left shift of 1, 2, or 3 because these are commonly found in real-world code and because they can be implemented with a minimal amount of additional hardware beyond that of the simple adder. This avoids lengthening the critical path in implementations.

While the shift and add instructions are limited to a maximum left shift of 3, the [slli](#) instruction (from the base ISA) can be used to perform similar shifts for indexing into arrays of wider elements. The [slli.uw](#) — added in this extension — can be used when the index is to be interpreted as an unsigned word.

A.39.3. Instructions

The following 3 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

sh1add	Shift left by 1 and add
sh2add	Shift left by 2 and add
sh3add	Shift left by 3 and add

A.40. Extension Zbb

Long Name: Basic bit-manipulation
Version Requirement: ~> 1.0

A.40.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-06

A.40.2. Synopsis

Basic bit-manipulation

A.40.3. Instructions

The following 17 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

andn	AND with inverted operand
orn	OR with inverted operand
rev8	Byte-reverse register (RV64 encoding)
rol	Rotate left (Register)
ror	Rotate right (Register)
rori	Rotate right (Immediate)
xnor	Exclusive NOR
clz	Count leading zero bits
cpop	Count set bits
ctz	Count trailing zero bits
max	Maximum
maxu	Unsigned maximum
min	Minimum
minu	Unsigned minimum
orc.b	Bitware OR-combine, byte granule
sext.b	Sign-extend byte
sext.h	Sign-extend halfword

A.41. Extension Zbs

Long Name: Single-bit instructions

Version Requirement: ~> 1.0

A.41.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-06
Ratification document	drive.google.com/drive/u/0/folders/1_wqb-rXOVkGa6rqmugN3kwCftWDf1daU

A.41.2. Synopsis

The single-bit instructions provide a mechanism to set, clear, invert, or extract a single bit in a register. The bit is specified by its index

A.41.3. Instructions

The following 8 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

bclr	Single-Bit clear (Register)
bclri	Single-Bit clear (Immediate)
bext	Single-Bit extract (Register)
bexti	Single-Bit extract (Immediate)
binv	Single-Bit invert (Register)
binvi	Single-Bit invert (Immediate)
bset	Single-Bit set (Register)

bseti	Single-Bit set (Immediate)

A.42. Extension Zca

Long Name: C instructions excluding floating-point loads/stores
Version Requirement: ~> 1.0

A.42.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-04

A.42.2. Synopsis

The Zca extension is added as way to refer to instructions in the C extension that do not include the floating-point loads and stores.

Therefore it excludes all 16-bit floating point loads and stores: c.flw, c.flwsp, c.fsw, c.fswsp, c.fld, c.fldsp, c.fsd, c.fsdsp.



The 'C' extension only includes F/D instructions when D and F are also specified.

A.42.3. Instructions

The following 26 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

c.add	Add
c.addi	Add a sign-extended non-zero immediate
c.addi16sp	Add a sign-extended non-zero immediate
c.addi4spn	Add a zero-extended non-zero immediate, scaled by 4, to the stack pointer
c.and	And
c.andi	And immediate
c.beqz	Branch if Equal Zero
c.bnez	Branch if NOT Equal Zero
c.ebreak	Breakpoint exception
c.j	Jump
c.jalr	Jump and Link Register
c.jr	Jump Register
c.li	Load the sign-extended 6-bit immediate
c.lui	Load Upper Immediate
c.lw	Load word
c.lwsp	Load word from stack pointer
c.mv	Move Register
c.nop	Non-operation
c.or	Or
c.slli	Shift left logical immediate
c.srai	Shift right arithmetical immediate
c.srli	Shift right logical immediate
c.sub	Subtract
c.sw	Store word
c.swsp	Store word to stack
c.xor	Exclusive Or

A.43. Extension Zcb

Long Name: Simple code-size saving instructions
Version Requirement: ~> 1.0

A.43.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-04

A.43.2. Synopsis

Zcb has simple code-size saving instructions which are easy to implement on all CPUs. All proposed encodings are currently reserved for all architectures, and have no conflicts with any existing extensions.

The Zcb extension depends on the Zca extension.

As shown on the individual instruction pages, many of the instructions in Zcb depend upon another extension being implemented. For example, c.mul is only implemented if M or Zmmul is implemented, and c.sext.b is only implemented if Zbb is implemented.



Additional compressed (16-bit) instructions

A.43.3. Instructions

The following 6 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

c.lbu	Load unsigned byte, 16-bit encoding
c.lh	Load signed halfword, 16-bit encoding
c.lhu	Load unsigned halfword, 16-bit encoding
c.not	Bitwise not, 16-bit encoding
c.sb	Store unsigned byte, 16-bit encoding
c.sh	Store unsigned halfword, 16-bit encoding

A.44. Extension Zcd

Long Name: Compressed double-precision floating-point loads/stores

Version Requirement: ~> 1.0

A.44.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-04

A.44.2. Synopsis

Zcd is the existing set of compressed double precision floating point loads and stores: [c.fld](#), [c.fldsp](#), [c.fsd](#), [c.fsdsp](#).

A.44.3. Instructions

The following 4 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

c.fld	Load double-precision
c.fldsp	Load doubleword into floating-point register from stack
c.fsd	Store double-precision
c.fsdsp	Store double-precision value to stack

A.45. Extension Zcf

Long Name: Compressed single-precision floating-point loads/stores

Version Requirement: ~> 1.0

A.45.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-04

A.45.2. Synopsis

Zcf is the existing set of compressed single precision floating point loads and stores (RV32 only): [c.flw](#), [c.flwsp](#), [c.fsw](#), [c.fswsp](#).

A.45.3. Instructions

The following 4 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

c.flw	Load single-precision
c.flwsp	Load word into floating-point register from stack
c.fsw	Store single-precision
c.fswsp	Store single-precision value to stack

A.46. Extension Zcmop

Long Name: Compressed May-Be-Operations
Version Requirement: ~> 1.0

A.46.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-03

A.46.2. Synopsis

The "Zcmop" extension, which defines eight 16-bit MOP instructions named C.MOP.*n*, where *n* is an odd integer between 1 and 15, inclusive. C.MOP.*n* is encoded in the reserved encoding space corresponding to C.LUI *xn*, 0, as shown in [Table 10](#). Unlike the MOPs defined in the Zimop extension, the C.MOP.*n* instructions are defined to *not* write any register. Their encoding allows future extensions to define them to read register **x[n]**.

The Zcmop extension depends upon the Zca extension.



Very few suitable 16-bit encoding spaces exist. This space was chosen because it already has unusual behavior with respect to the **rd/rs1** field—it encodes [c.addi16sp](#) when the field contains **x2**--and is therefore of lower value for most purposes.

Table 10. C.MOP.*n* instruction encoding.

Mnemonic	Encoding	Redefinable to read register
C.MOP.1	0110000010000001	x1
C.MOP.3	0110000110000001	x3
C.MOP.5	0110001010000001	x5
C.MOP.7	0110001110000001	x7
C.MOP.9	0110010010000001	x9
C.MOP.11	0110010110000001	x11
C.MOP.13	0110011010000001	x13
C.MOP.15	0110011110000001	x15



The recommended assembly syntax for C.MOP.*n* is simply the nullary C.MOP.*n*. The possibly accessed register is implicitly **xn**.



The expectation is that each Zcmop instruction is equivalent to some Zimop instruction, but the choice of expansion (if any) is left to the extension that redefines the MOP. Note, a Zcmop instruction that does not write a value can expand into a write to **x0**.



Compressed (16-bit) may-be operations

A.46.3. Instructions

The following 1 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

c.mop.n	Compressed May-Be-Operation

A.47. Extension Zfa

Long Name: Additional Floating-Point Instructions
Version Requirement: ~> 1.0

A.47.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-09

A.47.2. Synopsis

[Zfa](#) adds instructions for immediate loads, IEEE 754-2019 minimum and maximum operations, round-to-integer operations, and quiet floating-point comparisons. For RV32D, the [Zfa](#) extension also adds instructions to transfer double-precision floating-point values to and from integer registers, and for RV64Q, it adds analogous instructions for quad-precision floating-point values. The [Zfa](#) extension depends on the [F](#) extension.



Additional floating-point instructions

A.47.3. Instructions

The following 7 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

fleq.s	Floating-Point Less Than or Equal Quiet Single-Precision
fltq.s	Floating-Point Less Than Quiet Single-Precision
fli.s	No synopsis available
fmaxm.s	No synopsis available
fminm.s	No synopsis available
fround.s	Floating-point round single-precision float to integer
froundnx.s	Floating-point Round Single-precision to Integer with Inexact

A.48. Extension Zfh

Long Name: Half-precision floating point
Version Requirement: ~> 1.0

A.48.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-11

A.48.2. Synopsis

16-bit half-precision binary floating-point instructions compliant with the IEEE 754-2008 arithmetic standard. The [Zfh](#) extension depends on the single-precision floating-point extension, [F](#). The NaN-boxing scheme is extended to allow a half-precision value to be NaN-boxed inside a single-precision value (which may be recursively NaN-boxed inside a double- or quad-precision value when the D or Q extension is present).



A future RVB profile might mandate V.

A.48.3. Instructions

The following 22 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

fadd.h	No synopsis available
fclass.h	No synopsis available
fcvt.h.w	Floating-point Convert Word to Half-precision
fcvt.h.wu	Floating-point Convert Unsigned Word to Half-precision
fcvt.w.h	Floating-point Convert Half-precision to Word
fcvt.wu.h	Floating-point Convert Half-precision to Word
fdiv.h	No synopsis available
feq.h	No synopsis available
fle.h	No synopsis available
flt.h	No synopsis available
fmadd.h	No synopsis available
fmax.h	No synopsis available

fmin.h	No synopsis available
fmsub.h	No synopsis available
fmul.h	No synopsis available
fnmadd.h	No synopsis available
fnmsub.h	No synopsis available
fsgnj.h	No synopsis available
fsgnjn.h	No synopsis available
fsgnjx.h	No synopsis available
fsqrt.h	No synopsis available
fsub.h	No synopsis available

A.49. Extension Zfhmin

Long Name: Minimal half-precision floating-point
Version Requirement: ~> 1.0

A.49.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-11

A.49.2. Synopsis

[Zfhmin](#) provides minimal support for 16-bit half-precision binary floating-point instructions. The Zfhmin extension is a subset of the [Zfh](#) extension, consisting only of data transfer and conversion instructions. Like [Zfh](#), the [Zfhmin](#) extension depends on the single-precision floating-point extension, [F](#). The expectation is that [Zfhmin](#) software primarily uses the half-precision format for storage, performing most computation in higher precision.

The [Zfhmin](#) extension includes the following instructions from the [Zfh](#) extension: [flh](#), [fsh](#), [fmv.x.h](#), [fmv.h.x](#), [fcvt.s.h](#), and [fcvt.h.s](#). If the [D](#) extension is present, the [fcvt.d.h](#) and [fcvt.h.d](#) instructions are also included. If the [Q](#) extension is present, the [fcvt.q.h](#) and [fcvt.h.q](#) instructions are additionally included.



[Zfhmin](#) does not include the [fsgnj.h](#) instruction, because it suffices to instead use the [fsgnj.s](#) instruction to move half-precision values between floating-point registers.

Half-precision addition, subtraction, multiplication, division, and square-root operations can be faithfully emulated by converting the half-precision operands to single-precision, performing the operation using single-precision arithmetic, then converting back to half-precision. cite:[roux:hal-01091186] Performing half-precision fused multiply-addition using this method incurs a 1-ulp error on some inputs for the RNE and RMM rounding modes.

Conversion from 8- or 16-bit integers to half-precision can be emulated by first converting to single-precision, then converting to half-precision. Conversion from 32-bit integer can be emulated by first converting to double-precision. If the [D](#) extension is not present and a 1-ulp error under RNE or RMM is tolerable, 32-bit integers can be first converted to single-precision instead. The same remark applies to conversions from 64-bit integers without the [Q](#) extension.



Zfhmin is a small extension that adds support to load/store and convert IEEE 754 half-precision numbers to and from the IEEE 754 single-precision format. The hardware cost for this extension is low, and mandating the extension avoids adding an option to the profile.

A.49.3. Instructions

The following 6 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

fcvt.h.s	Convert half-precision float to a single-precision float
fcvt.s.h	Convert single-precision float to a half-precision float
flh	Half-precision floating-point load
fmv.h.x	Half-precision floating-point move from integer
fmv.x.h	Move half-precision value from floating-point to integer register
fsh	Half-precision floating-point store

A.50. Extension Zic64b

Long Name: 64-byte cache blocks
Version Requirement: = 1.0

A.50.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03
Ratification document	github.com/riscv/riscv-profiles/releases/tag/v1.0

A.50.2. Synopsis

Cache blocks must be 64 bytes in size, naturally aligned in the address space.



This extension was ratified with the RVA20 profiles.



This is a new extension name for this feature. While the general RISC-V specifications are agnostic to cache block size, selecting a common cache block size simplifies the specification and use of the following cache-block extensions within the application processor profile. Software does not have to query a discovery mechanism and/or provide dynamic dispatch to the appropriate code. We choose 64 bytes at it is effectively an industry standard. Implementations may use longer cache blocks to reduce tag cost provided they use 64-byte sub-blocks to remain compatible. Implementations may use shorter cache blocks provided they sequence cache operations across the multiple cache blocks comprising a 64-byte block to remain compatible.

A.51. Extension Zicbom

Long Name: Cache-block management instructions
Version Requirement: ~> 1.0

A.51.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2022-05

A.51.2. Synopsis

Cache-block management instructions

A.51.3. Instructions

The following 3 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

cbo.clean	Cache Block Clean
cbo.flush	Cache Block Flush
cbo.inval	Cache Block Invalidate

A.51.4. OUT-OF-SCOPE Parameters

CACHE_BLOCK_SIZE ⇒ 1 to 0xffffffffffffff

The observable size of a cache block, in bytes

FORCE_UPGRADE_CBO_INVAL_TO_FLUSH ⇒ boolean

When true, an implementation prohibits setting `menvcfg.CBIE == 11` such that all `cbo.inval` instructions either trap (when `menvcfg.CBIE == '00'`) or flush (when `menvcfg.CBIE == '01'`).

When false, an implementation allows a true INVAL operation for `cbo.inval`, and thus supports the setting `menvcfg.CBIE == 11`.

A.52. Extension Zicbop

Long Name: Cache-block prefetch
Version Requirement: ~> 1.0

A.52.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2022-05

A.52.2. Synopsis

Cache-block prefetch instructions



As with other HINTS, the inclusion of prefetches in the mandatory set of extensions indicates that software should generate these instructions where they are expected to be useful, and hardware is expected to exploit that information.

A.52.3. Instructions

The following 3 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

prefetch.i	Cache block prefetch for instruction fetch
prefetch.r	Cache block prefetch for data read
prefetch.w	Cache block prefetch for data write

A.52.4. OUT-OF-SCOPE Parameters

CACHE_BLOCK_SIZE ⇒ 1 to 0xffffffff
The observable size of a cache block, in bytes

A.53. Extension Zicboz

Long Name: Cache-block zero instruction
Version Requirement: ~> 1.0

A.53.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2022-05

A.53.2. Synopsis

Cache-block zero instruction

A.53.3. Instructions

The following 1 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

cbo.zero	Cache Block Zero

A.53.4. OUT-OF-SCOPE Parameters

CACHE_BLOCK_SIZE ⇒ 1 to 0xffffffff
The observable size of a cache block, in bytes

A.54. Extension Ziccamo

Long Name: Main memory supports all atomics in A extension
Version Requirement: ~> 1.0

A.54.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.54.2. Synopsis

Main memory regions with both the cacheability and coherence PMAs must support AMOArithmetic.

-  This extension was ratified as part of the RVA20 profile.
-  Ziccamo is a profile-defined extension introduced with RVA20.

A.55. Extension Ziccif

Long Name: Main memory supports instruction fetch with atomicity requirement

Version Requirement: ~> 1.0

A.55.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.55.2. Synopsis

Main memory regions with both the cacheability and coherence PMAs must support instruction fetch, and any instruction fetches of naturally aligned power-of-2 sizes up to min(ILEN,XLEN) (i.e., 32 bits for RVA22) are atomic.

-  This extension was ratified as part of the RVA20 profile.
-  Ziccif is a profile-defined extension introduced with RVA20. The fetch atomicity requirement facilitates runtime patching of aligned instructions.

A.56. Extension Zicclsm

Long Name: Main memory supports misaligned loads/stores

Version Requirement: ~> 1.0

A.56.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-03

A.56.2. Synopsis

Misaligned loads and stores to main memory regions with both the cacheability and coherence PMAs must be supported.

-  This extension was ratified as part of the RVA20 profile.
-  This requires misaligned support for all regular load and store instructions (including scalar and vector) but not AMOs or other specialized forms of memory access. Even though mandated, misaligned loads and stores might execute extremely slowly. Standard software distributions should assume their existence only for correctness, not for performance.
-  Zicclsm is a profile-defined extension introduced with RVA20. This requires misaligned support for all regular load and store instructions (including scalar and vector) but not AMOs or other specialized forms of memory access. Even though mandated, misaligned loads and stores might execute extremely slowly. Standard software distributions should assume their existence only for correctness, not for performance.

A.57. Extension Ziccrse

Long Name: Main memory supports forward progress on LR/SC sequences

Version Requirement: ~> 1.0

A.57.1. Available Versions

Version 1.0.0	
State	ratified

Version 1.0.0	
Ratification date	2023-03

A.57.2. Synopsis

Main memory regions with both the cacheability and coherence PMAs must support RsrvEventual.

-  This extension was ratified as part of the RVA20 profile.
-  Ziccrse is a profile-defined extension introduced with RVA20.

A.58. Extension Zicntr

Long Name: Base Counters and Timers
Version Requirement: ~> 2.0

A.58.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2019-12

A.58.2. Synopsis

The CYCLE, TIME, and INSTRET counters, which have dedicated functions (cycle count, real-time clock, and instructions retired, respectively).

A.58.3. CSRs

The following 3 CSRs are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
cycle	Cycle counter for RDCYCLE Instruction	0xc00	U
instret	Instructions retired counter for RDINSTRET Instruction	0xc02	U
time	Timer for RDTIME Instruction	0xc01	U

A.58.4. OUT-OF-SCOPE Parameters

TIME_CSR_IMPLEMENTED ⇒ boolean

Whether or not a real hardware [time](#) CSR exists. Implementations can either provide a real CSR or emulate access at M-mode.

Possible values:

- true**
[time/timeh](#) exists, and accessing it will not cause an IllegalInstruction trap
- false**
[time/timeh](#) does not exist. Accessing the CSR will cause an IllegalInstruction trap or enter an unpredictable state, depending on TRAP_ON_UNIMPLEMENTED_CSR. Privileged software may emulate the [time](#) CSR, or may pass the exception to a lower level.

A.59. Extension Zicond

Long Name: Integer Conditional Operations
Version Requirement: ~> 1.0

A.59.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-11

A.59.2. Synopsis

The "Conditional" operations extension provides a simple solution that provides most of the benefit and all of the flexibility one would desire to support conditional arithmetic and conditional-select/move operations, while remaining true to the RISC-V design philosophy. The instructions follow the format for R-type instructions with 3 operands (*i.e.*, 2 source operands and 1 destination operand).

Using these instructions, branchless sequences can be implemented (typically in two-instruction sequences) without the need for instruction fusion, special provisions during the decoding of architectural instructions, or other microarchitectural provisions.



Integer conditional operations

A.59.3. Instructions

The following 2 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

czero.eqz	Conditional zero, if condition is equal to zero
czero.nez	Conditional zero, if condition is nonzero

A.60. Extension Zicsr

Long Name: Control and status register instructions
Version Requirement: ~> 2.0

A.60.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2019-04

A.60.2. Synopsis

Control and status register instructions

A.60.3. Instructions

The following 6 instructions are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

csrrc	Atomic Read and Clear Bits in CSR
csrrci	Atomic Read and Clear Bits in CSR with Immediate
csrrs	Atomic Read and Set Bits in CSR
csrrsi	Atomic Read and Set Bits in CSR with Immediate
csrrw	Atomic Read/Write CSR
csrrwi	Atomic Read/Write CSR Immediate

A.60.4. OUT-OF-SCOPE Parameters

TIME_CSR_IMPLEMENTED ⇒ **boolean**

- Whether or not a real hardware [time](#) CSR exists. Implementations can either provide a real CSR or emulate access at M-mode.
- Possible values:
- true**

[time/timeh](#) exists, and accessing it will not cause an IllegalInstruction trap
- false**

[time/timeh](#) does not exist. Accessing the CSR will cause an IllegalInstruction trap or enter an unpredictable state, depending on TRAP_ON_UNIMPLEMENTED_CSR. Privileged software may emulate the [time](#) CSR, or may pass the exception to a lower level.

A.61. Extension Zifencei

Long Name: Instruction fence
Version Requirement: ~> 1.0

A.61.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2019-04

A.61.2. Synopsis

This chapter defines the "Zifencei" extension, which includes the FENCE.I instruction that provides explicit synchronization between writes to instruction memory and instruction fetches on the same hart. Currently, this instruction is the only standard mechanism to ensure that stores visible to a hart will also be visible to its instruction fetches.



We considered but did not include a "store instruction word" instruction as in cite:[majc]. JIT compilers may generate a large trace of instructions before a single FENCE.I, and amortize any instruction cache snooping/invalidation overhead by writing translated instructions to memory regions that are known not to reside in the I-cache.



The FENCE.I instruction was designed to support a wide variety of implementations. A simple implementation can flush the local instruction cache and the instruction pipeline when the FENCE.I is executed. A more complex implementation might snoop the instruction (data) cache on every data (instruction) cache miss, or use an inclusive unified private L2 cache to invalidate lines from the primary instruction cache when they are being written by a local store instruction. If instruction and data caches are kept coherent in this way, or if the memory system consists of only uncached RAMs, then just the fetch pipeline needs to be flushed at a FENCE.I.

The FENCE.I instruction was previously part of the base I instruction set. Two main issues are driving moving this out of the mandatory base, although at time of writing it is still the only standard method for maintaining instruction-fetch coherence.

First, it has been recognized that on some systems, FENCE.I will be expensive to implement and alternate mechanisms are being discussed in the memory model task group. In particular, for designs that have an incoherent instruction cache and an incoherent data cache, or where the instruction cache refill does not snoop a coherent data cache, both caches must be completely flushed when a FENCE.I instruction is encountered. This problem is exacerbated when there are multiple levels of I and D cache in front of a unified cache or outer memory system.

Second, the instruction is not powerful enough to make available at user level in a Unix-like operating system environment. The FENCE.I only synchronizes the local hart, and the OS can reschedule the user hart to a different physical hart after the FENCE.I. This would require the OS to execute an additional FENCE.I as part of every context migration. For this reason, the standard Linux ABI has removed FENCE.I from user-level and now requires a system call to maintain instruction-fetch coherence, which allows the OS to minimize the number of FENCE.I executions required on current systems and provides forward-compatibility with future improved instruction-fetch coherence mechanisms.

Future approaches to instruction-fetch coherence under discussion include providing more restricted versions of FENCE.I that only target a given address specified in *rs1*, and/or allowing software to use an ABI that relies on machine-mode cache-maintenance operations.



Instruction-Fetch fence instruction.

Zifencei is mandated as it is the only standard way to support instruction-cache coherence in RVB23 application processors. A new instruction-cache coherence mechanism is under development (tentatively named Zjid), which might be added as an option in the future.

A.61.3. Instructions

The following 1 instructions are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

fence.i	Instruction fence

A.62. Extension Zihintntl

Long Name: Non-Temporal Locality Hints
Version Requirement: ~> 1.0

A.62.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-05

A.62.2. Synopsis

The NTL instructions are HINTs that indicate that the explicit memory accesses of the immediately subsequent instruction (henceforth "target instruction") exhibit poor temporal locality of reference. The NTL instructions do not change architectural state, nor do they alter the architecturally visible effects of the target instruction. Four variants are provided:

The NTL.P1 instruction indicates that the target instruction does not exhibit temporal locality within the capacity of the innermost level of private cache in the memory hierarchy. NTL.P1 is encoded as ADD *x0*, *x0*, *x2*.

The NTL.PALL instruction indicates that the target instruction does not exhibit temporal locality within the capacity of any level of private cache in the memory hierarchy. NTL.PALL is encoded as `ADD x0, x0, x3`.

The NTL.S1 instruction indicates that the target instruction does not exhibit temporal locality within the capacity of the innermost level of shared cache in the memory hierarchy. NTL.S1 is encoded as `ADD x0, x0, x4`.

The NTL.ALL instruction indicates that the target instruction does not exhibit temporal locality within the capacity of any level of cache in the memory hierarchy. NTL.ALL is encoded as `ADD x0, x0, x5`.



The NTL instructions can be used to avoid cache pollution when streaming data or traversing large data structures, or to reduce latency in producer-consumer interactions.

A microarchitecture might use the NTL instructions to inform the cache replacement policy, or to decide which cache to allocate into, or to avoid cache allocation altogether. For example, NTL.P1 might indicate that an implementation should not allocate a line in a private L1 cache, but should allocate in L2 (whether private or shared). In another implementation, NTL.P1 might allocate the line in L1, but in the least-recently used state.

NTL.ALL will typically inform implementations not to allocate anywhere in the cache hierarchy. Programmers should use NTL.ALL for accesses that have no exploitable temporal locality.

Like any HINTs, these instructions may be freely ignored. Hence, although they are described in terms of cache-based memory hierarchies, they do not mandate the provision of caches.

Some implementations might respect these HINTs for some memory accesses but not others: e.g., implementations that implement LR/SC by acquiring a cache line in the exclusive state in L1 might ignore NTL instructions on LR and SC, but might respect NTL instructions for AMOs and regular loads and stores.

Table 11 lists several software use cases and the recommended NTL variant that *portable* software i.e., software not tuned for any specific implementation’s memory hierarchy should use in each case.

Table 11. Recommended NTL variant for portable software to employ in various scenarios.

Scenario	Recommended NTL variant
Access to a working set between and in size	NTL.P1
Access to a working set between and in size	NTL.PALL
Access to a working set greater than in size	NTL.S1
Access with no exploitable temporal locality (e.g., streaming)	NTL.ALL
Access to a contended synchronization variable	NTL.PALL



The working-set sizes listed in Table 11 are not meant to constrain implementers' cache-sizing decisions. Cache sizes will obviously vary between implementations, and so software writers should only take these working-set sizes as rough guidelines.

Table 12 lists several sample memory hierarchies and recommends how each NTL variant maps onto each cache level. The table also recommends which NTL variant that implementation-tuned software should use to avoid allocating in a particular cache level. For example, for a system with a private L1 and a shared L2, it is recommended that NTL.P1 and NTL.PALL indicate that temporal locality cannot be exploited by the L1, and that NTL.S1 and NTL.ALL indicate that temporal locality cannot be exploited by the L2. Furthermore, software tuned for such a system should use NTL.P1 to indicate a lack of temporal locality exploitable by the L1, or should use NTL.ALL indicate a lack of temporal locality exploitable by the L2.

If the C extension is provided, compressed variants of these HINTs are also provided: C.NTL.P1 is encoded as `C.ADD x0, x2`; C.NTL.PALL is encoded as `C.ADD x0, x3`; C.NTL.S1 is encoded as `C.ADD x0, x4`; and C.NTL.ALL is encoded as `C.ADD x0, x5`.

The NTL instructions affect all memory-access instructions except the cache-management instructions in the Zicbom extension.



As of this writing, there are no other exceptions to this rule, and so the NTL instructions affect all memory-access instructions defined in the base ISAs and the A, F, D, Q, C, and V standard extensions, as well as those defined within the hypervisor extension in Volume II.

The NTL instructions can affect cache-management operations other than those in the Zicbom extension. For example, NTL.PALL followed by CBO.ZERO might indicate that the line should be allocated in L3 and zeroed, but not allocated in L1 or L2.

Table 12. Mapping of NTL variants to various memory hierarchies.

Memory hierarchy	Recommended mapping of NTL variant to actual cache level				Recommended NTL variant for explicit cache management			
	P1	PALL	S1	ALL	L1	L2	L3	L4/L5
Common Scenarios								
No caches	---				none			
Private L1 only	L1	L1	L1	L1	ALL	---	---	---
Private L1; shared L2	L1	L1	L2	L2	P1	ALL	---	---
Private L1; shared L2/L3	L1	L1	L2	L3	P1	S1	ALL	---
Private L1/L2	L1	L2	L2	L2	P1	ALL	---	---
Private L1/L2; shared L3	L1	L2	L3	L3	P1	PALL	ALL	---
Private L1/L2; shared L3/L4	L1	L2	L3	L4	P1	PALL	S1	ALL
Uncommon Scenarios								
Private L1/L2/L3; shared L4	L1	L3	L4	L4	P1	P1	PALL	ALL
Private L1; shared L2/L3/L4	L1	L1	L2	L4	P1	S1	ALL	ALL
Private L1/L2; shared L3/L4/L5	L1	L2	L3	L5	P1	PALL	S1	ALL
Private L1/L2/L3; shared L4/L5	L1	L3	L4	L5	P1	P1	PALL	ALL

When an NTL instruction is applied to a prefetch hint in the Zicbop extension, it indicates that a cache line should be prefetched into a cache that is *outer* from the level specified by the NTL.



For example, in a system with a private L1 and shared L2, NTL.P1 followed by PREFETCH.R might prefetch into L2 with read intent.

To prefetch into the innermost level of cache, do not prefix the prefetch instruction with an NTL instruction.

In some systems, NTL.ALL followed by a prefetch instruction might prefetch into a cache or prefetch buffer internal to a memory controller.

Software is discouraged from following an NTL instruction with an instruction that does not explicitly access memory. Nonadherence to this recommendation might reduce performance but otherwise has no architecturally visible effect.

In the event that a trap is taken on the target instruction, implementations are discouraged from applying the NTL to the first instruction in the trap handler. Instead, implementations are recommended to ignore the HINT in this case.



If an interrupt occurs between the execution of an NTL instruction and its target instruction, execution will normally resume at the target instruction. That the NTL instruction is not reexecuted does not change the semantics of the program.

Some implementations might prefer not to process the NTL instruction until the target instruction is seen (e.g., so that the NTL can be fused with the memory access it modifies). Such implementations might preferentially take the interrupt before the NTL, rather than between the NTL and the memory access.



Since the NTL instructions are encoded as ADDs, they can be used within LR/SC loops without voiding the forward-progress guarantee. But, since using other loads and stores within an LR/SC loop *does* void the forward-progress guarantee, the only reason to use an NTL within such a loop is to modify the LR or the SC.



Non-temporal memory-access locality hints

A.62.3. Instructions

The following 4 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

ntl.all	Non-temporal locality hint, all
ntl.p1	Non-temporal locality hint, innermost private
ntl.pall	Non-temporal locality hint, all private
ntl.s1	Non-temporal locality hint, innermost shared

A.63. Extension Zihintpause

Long Name: Pause Hint
Version Requirement: ~> 2.0

A.63.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2021-02

A.63.2. Synopsis

The PAUSE instruction is a HINT that indicates the current hart’s rate of instruction retirement should be temporarily reduced or paused. The duration of its effect must be bounded and may be zero.



Software can use the PAUSE instruction to reduce energy consumption while executing spin-wait code sequences. Multithreaded cores might temporarily relinquish execution resources to other harts when PAUSE is executed. It is recommended that a PAUSE instruction generally be included in the code sequence for a spin-wait loop.

A future extension might add primitives similar to the x86 MONITOR/MWAIT instructions, which provide a more efficient mechanism to wait on writes to a specific memory location. However, these instructions would not supplant PAUSE. PAUSE is more appropriate when polling for non-memory events, when polling for multiple events, or when software does not know precisely what events it is polling for.

The duration of a PAUSE instruction’s effect may vary significantly within and among implementations. In typical implementations this duration should be much less than the time to perform a context switch, probably more on the rough order of an on-chip cache miss latency or a cacheless access to main memory.

A series of PAUSE instructions can be used to create a cumulative delay loosely proportional to the number of PAUSE instructions. In spin-wait loops in portable code, however, only one PAUSE instruction should be used before re-evaluating loop conditions, else the hart might stall longer than optimal on some implementations, degrading system performance.

PAUSE is encoded as a FENCE instruction with *pred=W*, *succ=0*, *fm=0*, *rd=x0*, and *rs1=x0*.



PAUSE is encoded as a hint within the FENCE opcode because some implementations are expected to deliberately stall the PAUSE instruction until outstanding memory transactions have completed. Because the successor set is null, however, PAUSE does not *mandate* any particular memory ordering—hence, it truly is a HINT.

Like other FENCE instructions, PAUSE cannot be used within LR/SC sequences without voiding the forward-progress guarantee.

The choice of a predecessor set of W is arbitrary, since the successor set is null. Other HINTs similar to PAUSE might be encoded with other predecessor sets.



While the [pause](#) instruction is a HINT can be implemented as a NOP and hence trivially supported by hardware implementers, its inclusion in the mandatory extension list signifies that software should use the instruction whenever it would make sense and that implementers are expected to exploit this information to optimize hardware execution.

A.63.3. Instructions

The following 1 instructions are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

pause	Pause hint

A.64. Extension Zihpm

Long Name: Hardware Performance Counters

Version Requirement: ~> 2.0

A.64.1. Available Versions

Version 2.0.0	
State	ratified
Ratification date	2023-03

A.64.2. Synopsis

Hardware performance counters



The number of counters is platform-specific.

A.64.3. CSRs

The following 29 CSRs are added by extension version 2.0.0 (the minimum version of this extension that satisfies the extension requirement).

Name	Long Name	Address	Mode
hpmcounter10	User-mode Hardware Performance Counter 7	0xc0a	U
hpmcounter11	User-mode Hardware Performance Counter 8	0xc0b	U
hpmcounter12	User-mode Hardware Performance Counter 9	0xc0c	U
hpmcounter13	User-mode Hardware Performance Counter 10	0xc0d	U
hpmcounter14	User-mode Hardware Performance Counter 11	0xc0e	U
hpmcounter15	User-mode Hardware Performance Counter 12	0xc0f	U
hpmcounter16	User-mode Hardware Performance Counter 13	0xc10	U
hpmcounter17	User-mode Hardware Performance Counter 14	0xc11	U
hpmcounter18	User-mode Hardware Performance Counter 15	0xc12	U
hpmcounter19	User-mode Hardware Performance Counter 16	0xc13	U
hpmcounter20	User-mode Hardware Performance Counter 17	0xc14	U
hpmcounter21	User-mode Hardware Performance Counter 18	0xc15	U
hpmcounter22	User-mode Hardware Performance Counter 19	0xc16	U
hpmcounter23	User-mode Hardware Performance Counter 20	0xc17	U
hpmcounter24	User-mode Hardware Performance Counter 21	0xc18	U
hpmcounter25	User-mode Hardware Performance Counter 22	0xc19	U
hpmcounter26	User-mode Hardware Performance Counter 23	0xc1a	U
hpmcounter27	User-mode Hardware Performance Counter 24	0xc1b	U
hpmcounter28	User-mode Hardware Performance Counter 25	0xc1c	U
hpmcounter29	User-mode Hardware Performance Counter 26	0xc1d	U
hpmcounter3	User-mode Hardware Performance Counter 0	0xc03	U
hpmcounter30	User-mode Hardware Performance Counter 27	0xc1e	U
hpmcounter31	User-mode Hardware Performance Counter 28	0xc1f	U
hpmcounter4	User-mode Hardware Performance Counter 1	0xc04	U
hpmcounter5	User-mode Hardware Performance Counter 2	0xc05	U
hpmcounter6	User-mode Hardware Performance Counter 3	0xc06	U
hpmcounter7	User-mode Hardware Performance Counter 4	0xc07	U
hpmcounter8	User-mode Hardware Performance Counter 5	0xc08	U
hpmcounter9	User-mode Hardware Performance Counter 6	0xc09	U

A.65. Extension Zimop

Long Name: May-Be-Operations
Version Requirement: ~> 1.0

A.65.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2024-03

A.65.2. Synopsis

The "Zimop" extension introduces the concept of instructions that *may be operations* (MOPs). MOPs are initially defined to simply write zero to `x[rd]`, but are designed to be redefined by later extensions to perform some other action. The Zimop extension defines an encoding space for 40 MOPs.



It is sometimes desirable to define instruction-set extensions whose instructions, rather than raising illegal-instruction exceptions when the extension is not implemented, take no useful action (beyond writing `x[rd]`). For example, programs with control-flow integrity checks can execute correctly on implementations without the corresponding extension, provided the checks are simply ignored. Implementing these checks as MOPs allows the same programs to run on implementations with or without the corresponding extension.

Although similar in some respects to HINTs, MOPs cannot be encoded as HINTs, because unlike HINTs, MOPs are allowed to alter

architectural state.

Because MOPs may be redefined by later extensions, standard software should not execute a MOP unless it is deliberately targeting an extension that has redefined that MOP.

The Zimop extension defines 32 MOP instructions named MOP.R.*n*, where *n* is an integer between 0 and 31, inclusive. Unless redefined by another extension, these instructions simply write 0 to **x[rd]**. Their encoding allows future extensions to define them to read **x[rs1]**, as well as write **x[rd]**.

The Zimop extension additionally defines 8 MOP instructions named MOP.RR.*n*, where *n* is an integer between 0 and 7, inclusive. Unless redefined by another extension, these instructions simply write 0 to **x[rd]**. Their encoding allows future extensions to define them to read **x[rs1]** and **x[rs2]**, as well as write **x[rd]**.



The recommended assembly syntax for MOP.R.*n* is MOP.R.*n* rd, rs1, with any **x**-register specifier being valid for either argument. Similarly for MOP.RR.*n*, the recommended syntax is MOP.RR.*n* rd, rs1, rs2. The extension that redefines a MOP may define an alternate assembly mnemonic.



These MOPs are encoded in the SYSTEM major opcode in part because it is expected their behavior will be modulated by privileged CSR state.



These MOPs are defined to write zero to **x[rd]**, rather than performing no operation, to simplify instruction decoding and to allow testing the presence of features by branching on the zeroness of the result.

The MOPs defined in the Zimop extension do not carry a syntactic dependency from **x[rs1]** or **x[rs2]** to **x[rd]**, though an extension that redefines the MOP may impose such a requirement.



Not carrying a syntactic dependency relieves straightforward implementations of reading **x[rs1]** and **x[rs2]**.



May-be operations

A.65.3. Instructions

The following 2 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

mop.r.n	May-be-operation (1 source register)
mop.rr.n	May-be-operation (2 source registers)

A.66. Extension Zkn

Long Name: NIST Algorithm Suite

Version Requirement: ~> 1.0

A.66.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-12
Version 1.0.1	
State	ratified
Ratification date	2022-02

A.66.2. Synopsis

This extension is shorthand for the following set of other extensions:

- [Zbkb](#)
- [Zbkc](#)
- [Zbkx](#)
- [Zkne](#)
- [Zknd](#)
- [Zknh](#)



Scalar crypto NIST algorithms

A.67. Extension Zkr

Long Name: Entropy Source
Version Requirement: ~> 1.0

A.67.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-12
Version 1.0.1	
State	ratified
Ratification date	2022-02

A.67.2. Synopsis

Defines the **seed** CSR. This CSR provides up to 16 physical entropy bits that can be used to seed cryptographic random bit generators.



Entropy CSR



Technically, Zk is also a privileged-mode option, capturing that Zkr, Zkn, and Zkt are all implemented. However, the Zk rollup is less descriptive than specifying the individual extensions explicitly.

A.68. Extension Zks

Long Name: ShangMi Algorithm Suite
Version Requirement: ~> 1.0

A.68.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-12
Version 1.0.1	
State	ratified
Ratification date	2022-02

A.68.2. Synopsis

This extension is shorthand for the following set of other extensions:

- [Zbkb](#)
- [Zbkc](#)
- [Zbkx](#)
- [Zksed](#)
- [Zksh](#)



Scalar crypto Shang-Mi algorithms

A.69. Extension Zkt

Long Name: Data-independent execution latency
Version Requirement: ~> 1.0

A.69.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2021-12

State	ratified
Ratification date	2022-02
Changes	Fix typos to show that c.srli, c.srai, and c.slli are Zkt instructions in RV64.

A.69.2. Synopsis

The Zkt extension attests that the machine has data-independent execution time for a safe subset of instructions. This property is commonly called "constant-time" although should not be taken with that literal meaning.

All currently proposed cryptographic instructions (scalar **K** extension) are on this list, together with a set of relevant supporting instructions from **I**, **M**, **C**, and **B** extensions.



Failure to prevent leakage of sensitive parameters via the direct timing channel is considered a serious security vulnerability and will typically result in a CERT CVE security advisory.

Scope and Goal

An "ISA contract" is made between a programmer and the RISC-V implementation that Zkt instructions do not leak information about processed secret data (plaintext, keying information, or other "sensitive security parameters" — FIPS 140-3 term) through differences in execution latency. Zkt does *not* define a set of instructions available in the core; it just restricts the behaviour of certain instructions if those are implemented.

Currently, the scope of this document is within scalar RV32/RV64 processors. Vector cryptography instructions (and appropriate vector support instructions) will be added later, as will other security-related functions that wish to assert leakage-free execution latency properties.

Loads, stores, conditional branches are excluded, along with a set of instructions that are rarely necessary to process secret data. Also excluded are instructions for which workarounds exist in standard cryptographic middleware due to the limitations of other ISA processors.

The stated goal is that OpenSSL, BoringSSL (Android), the Linux Kernel, and similar trusted software will not have directly observable timing side channels when compiled and running on a [Zkt](#)-enabled RISC-V target. The Zkt extension explicitly states many of the common latency assumptions made by cryptography developers.

Vendors do not have to implement all of the list's instructions to be Zkt compliant; however, if they claim to have Zkt and implement any of the listed instructions, it must have data-independent latency.

For example, many simple RV32I and RV64I cores (without Multiply, Compressed, Bitmanip, or Cryptographic extensions) are technically compliant with Zkt. A constant-time AES can be implemented on them using "bit-slice" techniques, but it will be excruciatingly slow when compared to implementation with AES instructions. There are no guarantees that even a bit-sliced cipher implementation (largely based on boolean logic instructions) is secure on a core without Zkt attestation.

Out-of-order implementations adhering to Zkt are still free to fuse, crack, change or even ignore sequences of instructions, so long as the optimisations are applied deterministically, and not based on operand data. The guiding principle should be that no information about the data being operated on should be leaked based on the execution latency.



It is left to future extensions or other techniques to tackle the problem of data-independent execution in implementations which advanced out-of-order capabilities which use value prediction, or which are otherwise data-dependent.



Note to software developers

Programming techniques can only mitigate leakage directly caused by arithmetic, caches, and branches. Other ISAs have had micro-architectural issues such as Spectre, Meltdown, Speculative Store Bypass, Rogue System Register Read, Lazy FP State Restore, Bounds Check Bypass Store, TLBleed, and L1TF/Foreshadow, etc. See e.g. [NSA Hardware and Firmware Security Guidance](#)

It is not within the remit of this proposal to mitigate these *micro-architectural* leakages.

Background

- Timing attacks are much more powerful than was realised before the 2010s, which has led to a significant mitigation effort in current cryptographic code-bases.
- Cryptography developers use static and dynamic security testing tools to trace the handling of secret information and detect occasions where it influences a branch or is used for a table lookup.
- Architectural testing for Zkt can be pragmatic and semi-formal; *security by design* against basic timing attacks can usually be achieved via conscious implementation (of relevant iterative multi-cycle instructions or instructions composed of micro-ops) in way that avoids data-dependent latency.
- Laboratory testing may utilize statistical timing attack leakage analysis techniques such as those described in ISO/IEC 17825 cite:[IS16].
- Binary executables should not contain secrets in the instruction encodings (Kerckhoffs's principle), so instruction timing may leak information about immediates, ordering of input registers, etc. There may be an exception to this in systems where a binary loader modifies the executable for purposes of relocation — and it is desirable to keep the execution location (PC) secret. This is why instructions such as LUI, AUIPC, and ADDI are on the list.

- The rules used by audit tools are relatively simple to understand. Very briefly; we call the plaintext, secret keys, expanded keys, nonces, and other such variables "secrets". A secret variable (arithmetically) modifying any other variable/register turns that into a secret too. If a secret ends up in address calculation affecting a load or store, that is a violation. If a secret affects a branch's condition, that is also a violation. A secret variable location or register becomes a non-secret via specific zeroization/sanitisation or by being declared ciphertext (or otherwise no-longer-secret information). In essence, secrets can only "touch" instructions on the Zkt list while they are secrets.

Specific Instruction Rationale

- HINT instruction forms (typically encodings with `rd=x0`) are excluded from the data-independent time requirement.
- Floating point (F, D, Q, L extensions) are currently excluded from the constant-time requirement as they have very few applications in standardised cryptography. We may consider adding floating point add, sub, multiply as a constant time requirement for some floating point extension in case a specific algorithm (such as the PQC Signature algorithm Falcon) becomes critical.
- Cryptographers typically assume division to be variable-time (while multiplication is constant time) and implement their Montgomery reduction routines with that assumption.
- Zicsr, Zifencei are excluded.
- Some instructions are on the list simply because we see no harm in including them in testing scope.

Programming Information

For background information on secure programming "models", see:

- Thomas Pornin: *"Why Constant-Time Crypto?"* (A great introduction to timing assumptions.) www.bearssl.org/constanttime.html
- Jean-Philippe Aumasson: *"Guidelines for low-level cryptography software."* (A list of recommendations.) github.com/veorq/cryptocoding
- Peter Schwabe: *"Timing Attacks and Countermeasures."* (Lecture slides — nice references.) summerschool-croatia.cs.ru.nl/2016/slides/PeterSchwabe.pdf
- Adam Langley: *"ctgrind."* (This is from 2010 but is still relevant.) www.imperialviolet.org/2010/04/01/ctgrind.html
- Kris Kwiatkowski: *"Constant-time code verification with Memory Sanitizer."* www.amongbytes.com/post/20210709-testing-constant-time/
- For early examples of timing attack vulnerabilities, see www.kb.cert.org/vuls/id/997481 and related academic papers.

Zkt listings

The following instructions are included in the [Zkt](#) subset They are listed here grouped by their original parent extension.



Note to implementers

You do not need to implement all of these instructions to implement [Zkt](#). Rather, every one of these instructions that the core does implement must adhere to the requirements of [Zkt](#).

RVI (Base Instruction Set)

Only basic arithmetic and `slt*` (for carry computations) are included. The data-independent timing requirement does not apply to HINT instruction encoding forms of these instructions.

RV32	RV64	Mnemonic	Instruction
✓	✓	lui <i>rd, imm</i>	'lui'
✓	✓	auipc <i>rd, imm</i>	'auipc'
✓	✓	addi <i>rd, rs1, imm</i>	'addi'
✓	✓	slti <i>rd, rs1, imm</i>	'slti'
✓	✓	sltiu <i>rd, rs1, imm</i>	'sltiu'
✓	✓	xori <i>rd, rs1, imm</i>	'xori'
✓	✓	ori <i>rd, rs1, imm</i>	'ori'
✓	✓	andi <i>rd, rs1, imm</i>	'andi'
✓	✓	slli <i>rd, rs1, imm</i>	'slli'
✓	✓	srli <i>rd, rs1, imm</i>	'srli'
✓	✓	srai <i>rd, rs1, imm</i>	'srai'
✓	✓	add <i>rd, rs1, rs2</i>	'add'
✓	✓	sub <i>rd, rs1, rs2</i>	'sub'
✓	✓	sll <i>rd, rs1, rs2</i>	'sll'
✓	✓	slt <i>rd, rs1, rs2</i>	'slt'
✓	✓	sltu <i>rd, rs1, rs2</i>	'sltu'
✓	✓	xor <i>rd, rs1, rs2</i>	'xor'

RV32	RV64	Mnemonic	Instruction
✓	✓	srl <i>rd, rs1, rs2</i>	'srl'
✓	✓	sra <i>rd, rs1, rs2</i>	'sra'
✓	✓	or <i>rd, rs1, rs2</i>	'or'
✓	✓	and <i>rd, rs1, rs2</i>	'and'
	✓	addiw <i>rd, rs1, imm</i>	'addiw'
	✓	slliw <i>rd, rs1, imm</i>	'slliw'
	✓	srliw <i>rd, rs1, imm</i>	'srliw'
	✓	sraiw <i>rd, rs1, imm</i>	'sraiw'
	✓	addw <i>rd, rs1, rs2</i>	'addw'
	✓	subw <i>rd, rs1, rs2</i>	'subw'
	✓	sllw <i>rd, rs1, rs2</i>	'sllw'
	✓	srlw <i>rd, rs1, rs2</i>	'srlw'
	✓	sraw <i>rd, rs1, rs2</i>	'sraw'

RVM (Multiply)

Multiplication is included; division and remaindering excluded.

RV32	RV64	Mnemonic	Instruction
✓	✓	mul <i>rd, rs1, rs2</i>	'mul'
✓	✓	mulh <i>rd, rs1, rs2</i>	'mulh'
✓	✓	mulhsu <i>rd, rs1, rs2</i>	'mulhsu'
✓	✓	mulhu <i>rd, rs1, rs2</i>	'mulhu'
	✓	mulw <i>rd, rs1, rs2</i>	'mulw'

RVC (Compressed)

Same criteria as in RVI. Organised by quadrants.

RV32	RV64	Mnemonic	Instruction
✓	✓	c.nop	'c_nop'
✓	✓	c.addi	'c_addi'
	✓	c.addiw	'c_addiw'
✓	✓	c.lui	'c_lui'
✓	✓	c.srli	'c_srli'
✓	✓	c.srai	'c_srai'
✓	✓	c.andi	'c_andi'
✓	✓	c.sub	'c_sub'
✓	✓	c.xor	'c_xor'
✓	✓	c.or	'c_or'
✓	✓	c.and	'c_and'
	✓	c.subw	'c_subw'
	✓	c.addw	'c_addw'
✓	✓	c.slli	'c_slli'
✓	✓	c.mv	'c_mv'
✓	✓	c.add	'c_add'

RVK (Scalar Cryptography)

All K-specific instructions are included. Additionally, **seed** CSR latency should be independent of **ES16** state output **entropy** bits, as that is a sensitive security parameter. See <<crypto_scalar_appx_es_access'.

RV32	RV64	Mnemonic	Instruction
✓		aes32dsi	'aes32dsi'
✓		aes32dsmi	'aes32dsmi'

RV32	RV64	Mnemonic	Instruction
✓		aes32esi	'aes32esi'
✓		aes32esmi	'aes32esmi'
	✓	aes64ds	'aes64ds'
	✓	aes64dsm	'aes64dsm'
	✓	aes64es	'aes64es'
	✓	aes64esm	'aes64esm'
	✓	aes64im	'aes64im'
	✓	aes64ks1i	'aes64ks1i'
	✓	aes64ks2	'aes64ks2'
✓	✓	sha256sig0	'sha256sig0'
✓	✓	sha256sig1	'sha256sig1'
✓	✓	sha256sum0	'sha256sum0'
✓	✓	sha256sum1	'sha256sum1'
✓		sha512sig0h	'sha512sig0h'
✓		sha512sig0l	'sha512sig0l'
✓		sha512sig1h	'sha512sig1h'
✓		sha512sig1l	'sha512sig1l'
✓		sha512sum0r	'sha512sum0r'
✓		sha512sum1r	'sha512sum1r'
	✓	sha512sig0	'sha512sig0'
	✓	sha512sig1	'sha512sig1'
	✓	sha512sum0	'sha512sum0'
	✓	sha512sum1	'sha512sum1'
✓	✓	sm3p0	'sm3p0'
✓	✓	sm3p1	'sm3p1'
✓	✓	sm4ed	'sm4ed'
✓	✓	sm4ks	'sm4ks'

RVB (Bitmanip)

The [Zbkb](#), ``Zbkc'` and ``Zbkx'` extensions are included in their entirety.



Note to implementers

Recall that `rev`, `zip` and `unzip` are pseudoinstructions representing specific instances of `grevi`, `shfli` and `unshfli` respectively.

RV32	RV64	Mnemonic	Instruction
✓	✓	clmul	'clmul-sc'
✓	✓	clmulh	'clmulh-sc'
✓	✓	xperm4	'xperm4-sc'
✓	✓	xperm8	'xperm8-sc'
✓	✓	ror	'ror-sc'
✓	✓	rol	'rol-sc'
✓	✓	rori	'rori-sc'
	✓	rorw	'rorw-sc'
	✓	rolw	'rolw-sc'
	✓	roriw	'roriw-sc'
✓	✓	andn	'andn-sc'
✓	✓	orn	'orn-sc'
✓	✓	xnor	'xnor-sc'
✓	✓	pack	'pack-sc'
✓	✓	packh	'packh-sc'
	✓	packw	'packw-sc'

RV32	RV64	Mnemonic	Instruction
✓	✓	brev8	'brev8-sc'
✓	✓	rev8	'rev8-sc'
✓		zip	'zip-sc'
✓		unzip	'unzip-sc'



Zkt requires a certain subset of integer instructions execute with data-independent latency. Mandating this feature enables portable libraries for safe basic cryptographic operations. It is expected that application processors will naturally have this property and so implementation cost is low, if not zero, in most systems that would support RVA22.

A.70. Extension Zvbb

Long Name: Vector Basic Bit-manipulation
Version Requirement: ~> 1.0

A.70.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-09

A.70.2. Synopsis

Vector basic bit-manipulation instructions.



Vector basic bit-manipulation instructions

A.70.3. Instructions

The following 16 instructions are added by extension version 1.0.0 (the minimum version of this extension that satisfies the extension requirement).

vandn.vv	No synopsis available
vandn.vx	No synopsis available
vbrev.v	No synopsis available
vbrev8.v	No synopsis available
vclz.v	No synopsis available
vcpop.v	No synopsis available
vctz.v	No synopsis available
vrev8.v	No synopsis available
vrol.vv	No synopsis available
vrol.vx	No synopsis available
vror.vi	No synopsis available
vror.vv	No synopsis available
vror.vx	No synopsis available
vwsll.vi	No synopsis available
vwsll.vv	No synopsis available
vwsll.vx	No synopsis available

A.71. Extension Zvfhmin

Long Name: Vector Extension for Minimal Half-Precision Floating-Point
Version Requirement: ~> 1.0

A.71.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-06

A.71.2. Synopsis

This extension provides minimal support for vectors of IEEE 754-2008 binary16 values, adding conversions to and from binary32. When the Zvfhmin extension is implemented, the [vfwcvt.f.f.v](#) and [vfncvt.f.f.w](#) instructions become defined when SEW=16. The EEW=16 floating-point operands of these instructions use the binary16 format.

This extension depends on the Zve32f extension.



Vector minimal half-precision floating-point

A.72. Extension Zvkt

Long Name: Vector Data-Independent Execution Latency

Version Requirement: ~> 1.0

A.72.1. Available Versions

Version 1.0.0	
State	ratified
Ratification date	2023-09

A.72.2. Synopsis

The Zvkt extension requires all implemented instructions from the following list to be executed with data-independent execution latency.

Data-independent execution latency (DIEL) applies to all data operands of an instruction, even those that are not a part of the body or that are inactive. However, DIEL does not apply to other values such as vl, vtype, and the mask (when used to control execution of a masked vector instruction). Also, DIEL does not apply to constant values specified in the instruction encoding such as the use of the zero register (x0), and, in the case of immediate forms of an instruction, the values in the immediate fields (i.e., imm, and uimm).

In some cases --- which are explicitly specified in the lists below --- operands that are used as control rather than data are exempt from DIEL.



Vector data-independent execution latency

Appendix B: Instruction Details

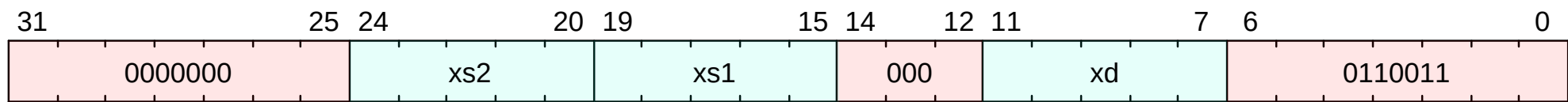
B.1. add

Integer add

This instruction is defined by:

I

B.1.1. Encoding



B.1.2. Description

Add the value in xs1 to xs2, and store the result in xd. Any overflow is thrown away.

B.1.3. Access

M	S	U
Always	Always	Always

B.1.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.1.5. IDL Operation

```
X[xd] = X[xs1] + X[xs2];
```

B.1.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD => xs1_val + xs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND => xs1_val & xs2_val,
    RISCV_OR  => xs1_val | xs2_val,
    RISCV_XOR => xs1_val ^ xs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB => xs1_val - xs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.1.7. Exceptions

This instruction does not generate synchronous exceptions.

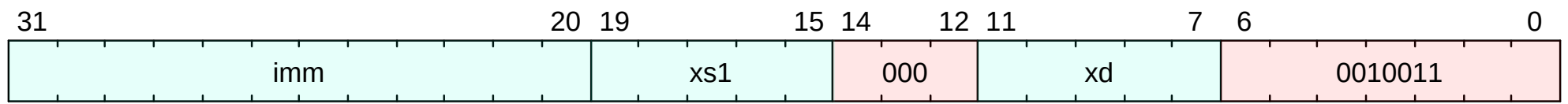
B.2. addi

Add immediate

This instruction is defined by:

I

B.2.1. Encoding



B.2.2. Description

Adds an immediate value to the value in xs1, and store the result in xd

B.2.3. Access

M	S	U
Always	Always	Always

B.2.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.2.5. IDL Operation

```
X[xd] = X[xs1] + $signed(imm);
```

B.2.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.2.7. Exceptions

This instruction does not generate synchronous exceptions.

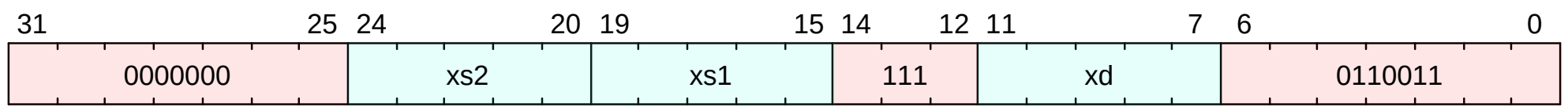
B.3. and

And

This instruction is defined by:

I

B.3.1. Encoding



B.3.2. Description

And xs1 with xs2, and store the result in xd

B.3.3. Access

M	S	U
Always	Always	Always

B.3.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.3.5. IDL Operation

```
X[xd] = X[xs1] & X[xs2];
```

B.3.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD => xs1_val + xs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND => xs1_val & xs2_val,
    RISCV_OR  => xs1_val | xs2_val,
    RISCV_XOR => xs1_val ^ xs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB => xs1_val - xs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.3.7. Exceptions

This instruction does not generate synchronous exceptions.

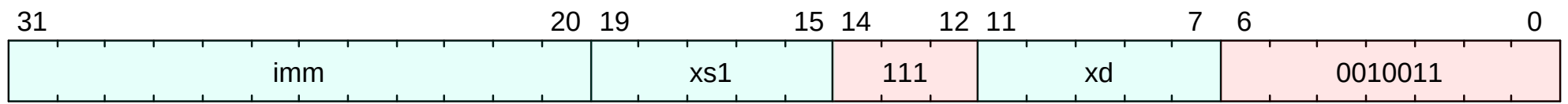
B.4. andi

And immediate

This instruction is defined by:

I

B.4.1. Encoding



B.4.2. Description

And an immediate to the value in xs1, and store the result in xd

B.4.3. Access

M	S	U
Always	Always	Always

B.4.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.4.5. IDL Operation

```
X[xd] = X[xs1] & $signed(imm);
```

B.4.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.4.7. Exceptions

This instruction does not generate synchronous exceptions.

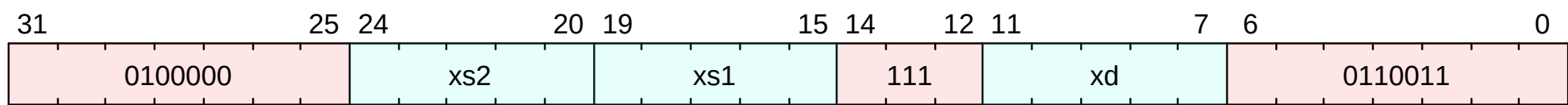
B.5. andn

AND with inverted operand

This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.5.1. Encoding



B.5.2. Description

Performs the bitwise logical AND operation between **xs1** and the bitwise inversion of **xs2**.

B.5.3. Access

M	S	U
Always	Always	Always

B.5.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.5.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs2] & ~X[xs1];
```

B.5.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.5.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

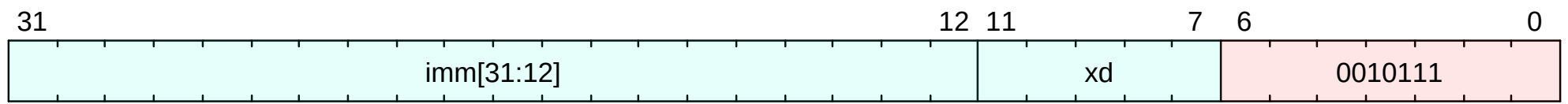
B.6. auipc

Add upper immediate to pc

This instruction is defined by:

I

B.6.1. Encoding



B.6.2. Description

Add an immediate to the current PC.

B.6.3. Access

M	S	U
Always	Always	Always

B.6.4. Decode Variables

```
Bits<32> imm = {$encoding[31:12], 12'd0};
Bits<5> xd = $encoding[11:7];
```

B.6.5. IDL Operation

```
X[xd] = $pc + $signed(imm);
```

B.6.6. Sail Operation

```
{
  let off : xlenbits = sign_extend(imm @ 0x000);
  let ret : xlenbits = match op {
    RISCV_LUI    => off,
    RISCV_AUIPC => get_arch_pc() + off
  };
  X(xd) = ret;
  RETIRE_SUCCESS
}
```

B.6.7. Exceptions

This instruction does not generate synchronous exceptions.

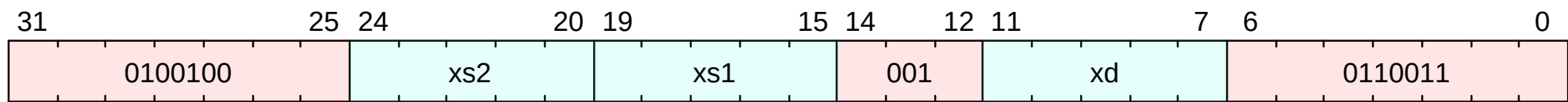
B.7. bclr

Single-Bit clear (Register)

This instruction is defined by:

Zbs

B.7.1. Encoding



B.7.2. Description

Returns xs1 with a single bit cleared at the index specified in xs2. The index is read from the lower log2(XLEN) bits of xs2.

B.7.3. Access

M	S	U
Always	Always	Always

B.7.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.7.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = X[xs2] & (xlen() - 1);
X[xd] = X[xs1] & ~(1 << index);
```

B.7.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << rs2_val[4..0]
    else zero_extend(0b1) << rs2_val[5..0];
  let result : xlenbits = match op {
    RISCV_BCLR => rs1_val & ~(mask),
    RISCV_BEXT => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINV => rs1_val ^ mask,
    RISCV_BSET => rs1_val | mask
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.7.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.8. bclri

Single-Bit clear (Immediate)

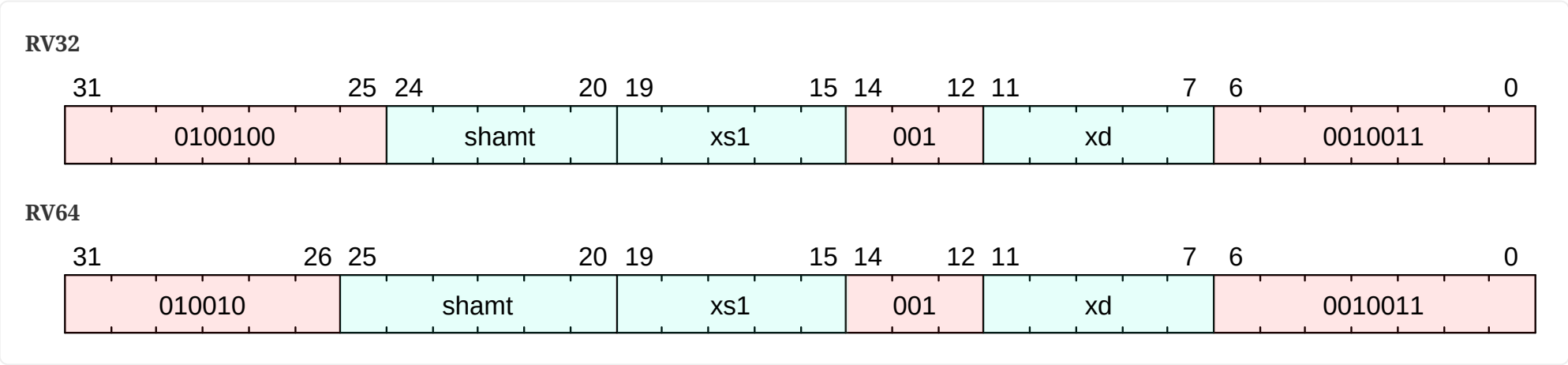
This instruction is defined by:

Zbs

B.8.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.8.2. Description

Returns xs1 with a single bit cleared at the index specified in shamt. The index is read from the lower log2(XLEN) bits of shamt. For RV32, the encodings corresponding to shamt[5]=1 are reserved.

B.8.3. Access

M	S	U
Always	Always	Always

B.8.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.8.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = shamt & (xlen() - 1);
X[xd] = X[xs1] & ~(1 << index);
```

B.8.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << shamt[4..0]
    else zero_extend(0b1) << shamt;
  let result : xlenbits = match op {
    RISCV_BCLRI => rs1_val & ~(mask),
    RISCV_BEXTI => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINVI => rs1_val ^ mask,
```

```
    RISC_V_BSETI => rs1_val | mask
};
X(rd) = result;
RETIRE_SUCCESS
}
```

B.8.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

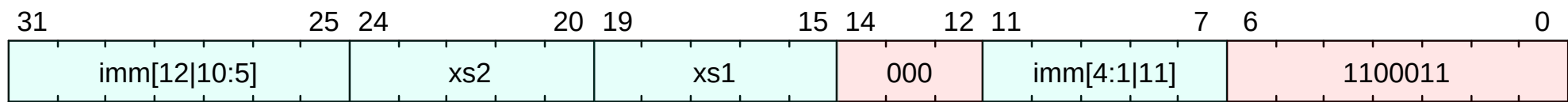
B.9. beq

Branch if equal

This instruction is defined by:

I

B.9.1. Encoding



B.9.2. Description

Branch to PC + imm if the value in register xs1 is equal to the value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.9.3. Access

M	S	U
Always	Always	Always

B.9.4. Decode Variables

```
signed Bits<13> imm = sext({$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0});
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.9.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if (lhs == rhs) {
    jump_halfword($pc + $signed(imm));
}
```

B.9.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let taken : bool = match op {
    RISCv_BEQ => xs1_val == xs2_val,
    RISCv_BNE => xs1_val != xs2_val,
    RISCv_BLT => xs1_val <_s xs2_val,
    RISCv_BGE => xs1_val >=_s xs2_val,
    RISCv_BLTU => xs1_val <_u xs2_val,
    RISCv_BGEU => xs1_val >=_u xs2_val
  };
  let t : xlenbits = PC + sign_extend(imm);
  if taken then {
    /* Extensions get the first checks on the prospective target address. */
    match ext_control_check_pc(t) {
      Ext_ControlAddr_Error(e) => {
        ext_handle_control_check_error(e);
        RETIRE_FAIL
      },
      Ext_ControlAddr_OK(target) => {
        if bit_to_bool(target[1]) & not(extension("C")) then {
          handle_mem_exception(target, E_Fetch_Addr_Align());
          RETIRE_FAIL;
        } else {
          set_next_pc(target);
          RETIRE_SUCCESS
        }
      }
    }
  }
}
```

```
    }  
    } else RETIRE_SUCCESS  
}
```

B.9.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

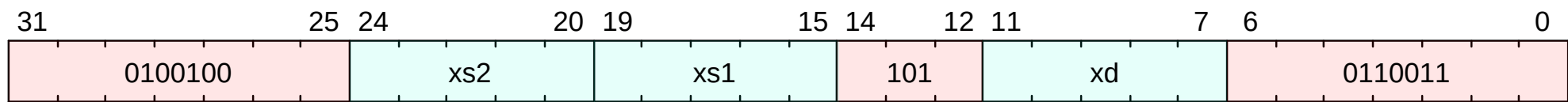
B.10. bext

Single-Bit extract (Register)

This instruction is defined by:

Zbs

B.10.1. Encoding



B.10.2. Description

Returns a single bit extracted from xs1 at the index specified in xs2. The index is read from the lower log2(XLEN) bits of xs2.

B.10.3. Access

M	S	U
Always	Always	Always

B.10.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.10.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = X[xs2] & (xlen() - 1);
X[xd] = (X[xs1] >> index) & 1;
```

B.10.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let mask : xlenbits = if sizeof(xlen) == 32
                            then zero_extend(0b1) << rs2_val[4..0]
                            else zero_extend(0b1) << rs2_val[5..0];
    let result : xlenbits = match op {
        RISCV_BCLR => rs1_val & ~(mask),
        RISCV_BEXT => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
        RISCV_BINV => rs1_val ^ mask,
        RISCV_BSET => rs1_val | mask
    };
    X(rd) = result;
    RETIRE_SUCCESS
}
```

B.10.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.11. bexti

Single-Bit extract (Immediate)

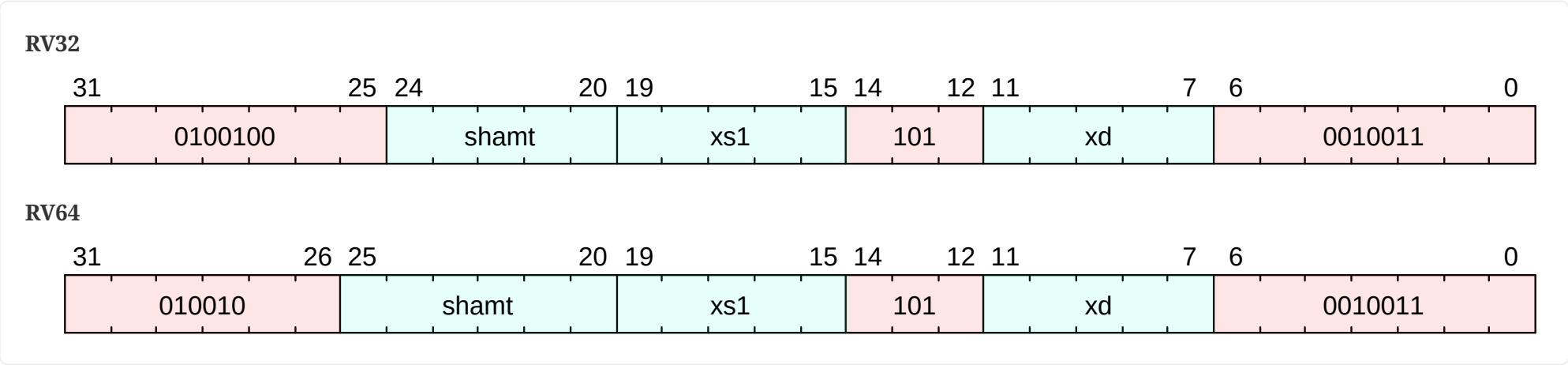
This instruction is defined by:

Zbs

B.11.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.11.2. Description

Returns a single bit extracted from xs1 at the index specified in xs2. The index is read from the lower log2(XLEN) bits of shamt. For RV32, the encodings corresponding to shamt[5]=1 are reserved.

B.11.3. Access

M	S	U
Always	Always	Always

B.11.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

B.11.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {  
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
}  
XReg index = shamt & (xlen() - 1);  
X[xd] = (X[xs1] >> index) & 1;
```

B.11.6. Sail Operation

```
{  
  let rs1_val = X(rs1);  
  let mask : xlenbits = if sizeof(xlen) == 32  
    then zero_extend(0b1) << shamt[4..0]  
    else zero_extend(0b1) << shamt;  
  let result : xlenbits = match op {  
    RISCV_BCLRI => rs1_val & ~(mask),  
    RISCV_BEXTI => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),  
    RISCV_BINVI => rs1_val ^ mask,  
  }
```

```
    RISCV_BSETI => rs1_val | mask
};
X(rd) = result;
RETIRE_SUCCESS
}
```

B.11.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

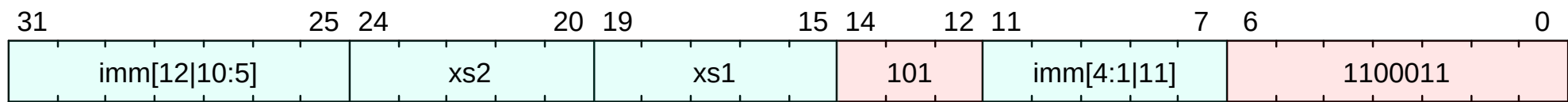
B.12. bge

Branch if greater than or equal

This instruction is defined by:

I

B.12.1. Encoding



B.12.2. Description

Branch to PC + imm if the signed value in register xs1 is greater than or equal to the signed value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.12.3. Access

M	S	U
Always	Always	Always

B.12.4. Decode Variables

```
signed Bits<13> imm = sext({$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0});
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.12.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if ($signed(lhs) >= $signed(rhs)) {
    jump_halfword($pc + $signed(imm));
}
```

B.12.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let taken : bool = match op {
    RISC_V_BEQ => xs1_val == xs2_val,
    RISC_V_BNE => xs1_val != xs2_val,
    RISC_V_BLT => xs1_val <_s xs2_val,
    RISC_V_BGE => xs1_val >=_s xs2_val,
    RISC_V_BLTU => xs1_val <_u xs2_val,
    RISC_V_BGEU => xs1_val >=_u xs2_val
  };
  let t : xlenbits = PC + sign_extend(imm);
  if taken then {
    /* Extensions get the first checks on the prospective target address. */
    match ext_control_check_pc(t) {
      Ext_ControlAddr_Error(e) => {
        ext_handle_control_check_error(e);
        RETIRE_FAIL
      },
      Ext_ControlAddr_OK(target) => {
        if bit_to_bool(target[1]) & not(extension("C")) then {
          handle_mem_exception(target, E_Fetch_Addr_Align());
          RETIRE_FAIL;
        } else {
          set_next_pc(target);
          RETIRE_SUCCESS
        }
      }
    }
  }
}
```

```
    }  
    } else RETIRE_SUCCESS  
}
```

B.12.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

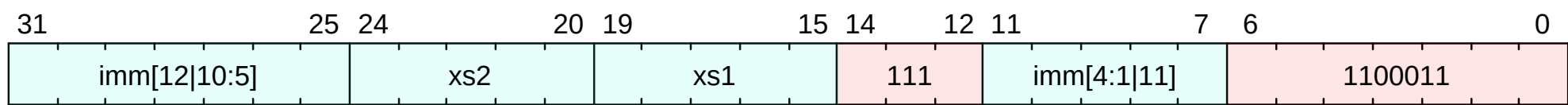
B.13. bgeu

Branch if greater than or equal unsigned

This instruction is defined by:

I

B.13.1. Encoding



B.13.2. Description

Branch to PC + imm if the unsigned value in register xs1 is greater than or equal to the unsigned value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.13.3. Access

M	S	U
Always	Always	Always

B.13.4. Decode Variables

```
Bits<13> imm = {$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.13.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if (lhs >= rhs) {
    jump_halfword($pc + $signed(imm));
}
```

B.13.6. Sail Operation

```
{
    let xs1_val = X(xs1);
    let xs2_val = X(xs2);
    let taken : bool = match op {
        RISCV_BEQ => xs1_val == xs2_val,
        RISCV_BNE => xs1_val != xs2_val,
        RISCV_BLT => xs1_val <_s xs2_val,
        RISCV_BGE => xs1_val >=_s xs2_val,
        RISCV_BLTU => xs1_val <_u xs2_val,
        RISCV_BGEU => xs1_val >=_u xs2_val
    };
    let t : xlenbits = PC + sign_extend(imm);
    if taken then {
        /* Extensions get the first checks on the prospective target address. */
        match ext_control_check_pc(t) {
            Ext_ControlAddr_Error(e) => {
                ext_handle_control_check_error(e);
                RETIRE_FAIL
            },
            Ext_ControlAddr_OK(target) => {
                if bit_to_bool(target[1]) & not(extension("C")) then {
                    handle_mem_exception(target, E_Fetch_Addr_Align());
                    RETIRE_FAIL;
                } else {
                    set_next_pc(target);
                    RETIRE_SUCCESS
                }
            }
        }
    }
}
```



```
    }  
    } else RETIRE_SUCCESS  
}
```

B.13.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

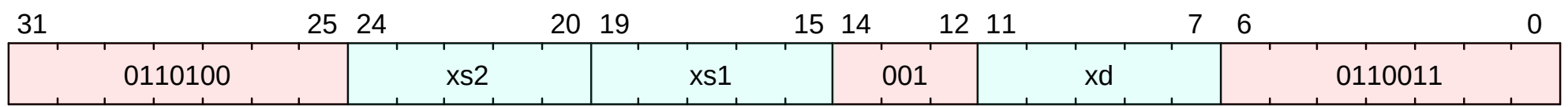
B.14. binv

Single-Bit invert (Register)

This instruction is defined by:

Zbs

B.14.1. Encoding



B.14.2. Description

Returns xs1 with a single bit inverted at the index specified in xs2. The index is read from the lower log2(XLEN) bits of xs2.

B.14.3. Access

M	S	U
Always	Always	Always

B.14.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.14.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = X[xs2] & (xlen() - 1);
X[xd] = X[xs1] ^ (1 << index);
```

B.14.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << rs2_val[4..0]
    else zero_extend(0b1) << rs2_val[5..0];
  let result : xlenbits = match op {
    RISCV_BCLR => rs1_val & ~(mask),
    RISCV_BEXT => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINV => rs1_val ^ mask,
    RISCV_BSET => rs1_val | mask
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.14.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.15. binvi

Single-Bit invert (Immediate)

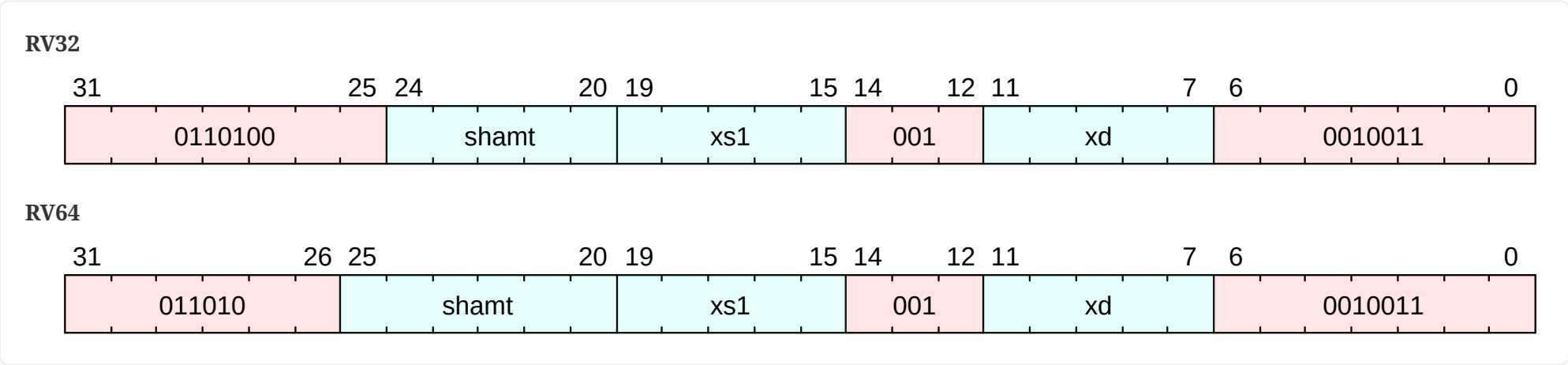
This instruction is defined by:

Zbs

B.15.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.15.2. Description

Returns xs1 with a single bit inverted at the index specified in shamt. The index is read from the lower log2(XLEN) bits of shamt. For RV32, the encodings corresponding to shamt[5]=1 are reserved.

B.15.3. Access

M	S	U
Always	Always	Always

B.15.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.15.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = shamt & (xlen() - 1);
X[xd] = X[xs1] ^ (1 << index);
```

B.15.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << shamt[4..0]
    else zero_extend(0b1) << shamt;
  let result : xlenbits = match op {
    RISCV_BCLRI => rs1_val & ~(mask),
    RISCV_BEXTI => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINVI => rs1_val ^ mask,
```

```
    RISC_V_BSETI => rs1_val | mask
};
X(rd) = result;
RETIRE_SUCCESS
}
```

B.15.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

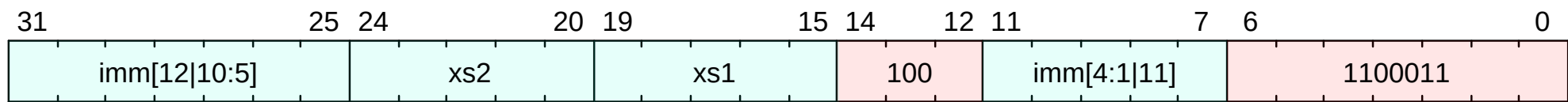
B.16. blt

Branch if less than

This instruction is defined by:

I

B.16.1. Encoding



B.16.2. Description

Branch to PC + imm if the signed value in register xs1 is less than the signed value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.16.3. Access

M	S	U
Always	Always	Always

B.16.4. Decode Variables

```
signed Bits<13> imm = sext({$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0});
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.16.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if ($signed(lhs) < $signed(rhs)) {
  jump_halfword($pc + $signed(imm));
}
```

B.16.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let taken : bool = match op {
    RISCv_BEQ => xs1_val == xs2_val,
    RISCv_BNE => xs1_val != xs2_val,
    RISCv_BLT => xs1_val <_s xs2_val,
    RISCv_BGE => xs1_val >=_s xs2_val,
    RISCv_BLTU => xs1_val <_u xs2_val,
    RISCv_BGEU => xs1_val >=_u xs2_val
  };
  let t : xlenbits = PC + sign_extend(imm);
  if taken then {
    /* Extensions get the first checks on the prospective target address. */
    match ext_control_check_pc(t) {
      Ext_ControlAddr_Error(e) => {
        ext_handle_control_check_error(e);
        RETIRE_FAIL
      },
      Ext_ControlAddr_OK(target) => {
        if bit_to_bool(target[1]) & not(extension("C")) then {
          handle_mem_exception(target, E_Fetch_Addr_Align());
          RETIRE_FAIL;
        } else {
          set_next_pc(target);
          RETIRE_SUCCESS
        }
      }
    }
  }
}
```

```
    }  
    } else RETIRE_SUCCESS  
}
```

B.16.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

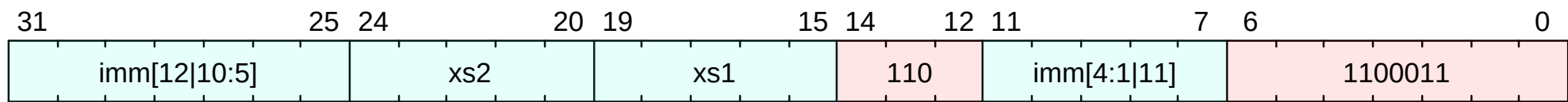
B.17. bltu

Branch if less than unsigned

This instruction is defined by:

I

B.17.1. Encoding



B.17.2. Description

Branch to PC + imm if the unsigned value in register xs1 is less than the unsigned value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.17.3. Access

M	S	U
Always	Always	Always

B.17.4. Decode Variables

```
Bits<13> imm = {$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.17.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if (lhs < rhs) {
    jump_halfword($pc + $signed(imm));
}
```

B.17.6. Sail Operation

```
{
    let xs1_val = X(xs1);
    let xs2_val = X(xs2);
    let taken : bool = match op {
        RISCv_BEQ => xs1_val == xs2_val,
        RISCv_BNE => xs1_val != xs2_val,
        RISCv_BLT => xs1_val <_s xs2_val,
        RISCv_BGE => xs1_val >=_s xs2_val,
        RISCv_BLTU => xs1_val <_u xs2_val,
        RISCv_BGEU => xs1_val >=_u xs2_val
    };
    let t : xlenbits = PC + sign_extend(imm);
    if taken then {
        /* Extensions get the first checks on the prospective target address. */
        match ext_control_check_pc(t) {
            Ext_ControlAddr_Error(e) => {
                ext_handle_control_check_error(e);
                RETIRE_FAIL
            },
            Ext_ControlAddr_OK(target) => {
                if bit_to_bool(target[1]) & not(extension("C")) then {
                    handle_mem_exception(target, E_Fetch_Addr_Align());
                    RETIRE_FAIL;
                } else {
                    set_next_pc(target);
                    RETIRE_SUCCESS
                }
            }
        }
    }
}
```

```
    }  
    } else RETIRE_SUCCESS  
}
```

B.17.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

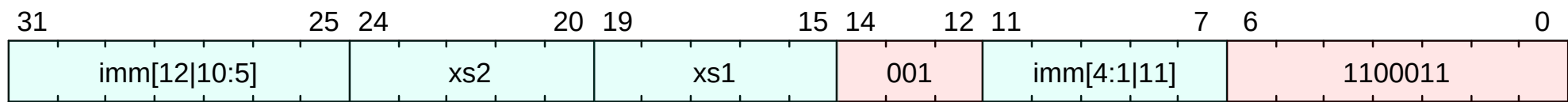
B.18. bne

Branch if not equal

This instruction is defined by:

I

B.18.1. Encoding



B.18.2. Description

Branch to PC + imm if the value in register xs1 is not equal to the value in register xs2.

Raise a **MisalignedAddress** exception if PC + imm is misaligned.

B.18.3. Access

M	S	U
Always	Always	Always

B.18.4. Decode Variables

```
signed Bits<13> imm = sext({$encoding[31], $encoding[7], $encoding[30:25], $encoding[11:8], 1'd0});
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.18.5. IDL Operation

```
XReg lhs = X[xs1];
XReg rhs = X[xs2];
if (lhs != rhs) {
    jump_halfword($pc + $signed(imm));
}
```

B.18.6. Sail Operation

```
{
    let xs1_val = X(xs1);
    let xs2_val = X(xs2);
    let taken : bool = match op {
        RISCV_BEQ => xs1_val == xs2_val,
        RISCV_BNE => xs1_val != xs2_val,
        RISCV_BLT => xs1_val <_s xs2_val,
        RISCV_BGE => xs1_val >=_s xs2_val,
        RISCV_BLTU => xs1_val <_u xs2_val,
        RISCV_BGEU => xs1_val >=_u xs2_val
    };
    let t : xlenbits = PC + sign_extend(imm);
    if taken then {
        /* Extensions get the first checks on the prospective target address. */
        match ext_control_check_pc(t) {
            Ext_ControlAddr_Error(e) => {
                ext_handle_control_check_error(e);
                RETIRE_FAIL
            },
            Ext_ControlAddr_OK(target) => {
                if bit_to_bool(target[1]) & not(extension("C")) then {
                    handle_mem_exception(target, E_Fetch_Addr_Align());
                    RETIRE_FAIL;
                } else {
                    set_next_pc(target);
                    RETIRE_SUCCESS
                }
            }
        }
    }
}
```

```
    }  
    } else RETIRE_SUCCESS  
}
```

B.18.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

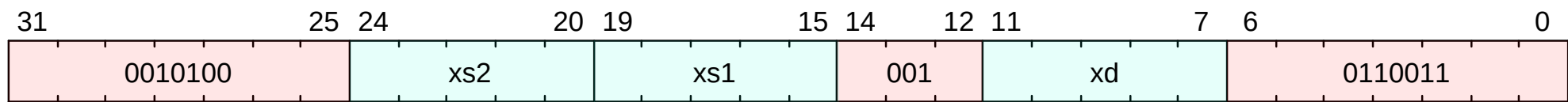
B.19. bset

Single-Bit set (Register)

This instruction is defined by:

Zbs

B.19.1. Encoding



B.19.2. Description

Returns xs1 with a single bit set at the index specified in xs2. The index is read from the lower log2(XLEN) bits of xs2.

B.19.3. Access

M	S	U
Always	Always	Always

B.19.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.19.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = X[xs2] & (xlen() - 1);
X[xd] = X[xs1] | (1 << index);
```

B.19.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << rs2_val[4..0]
    else zero_extend(0b1) << rs2_val[5..0];
  let result : xlenbits = match op {
    RISCV_BCLR => rs1_val & ~(mask),
    RISCV_BEXT => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINV => rs1_val ^ mask,
    RISCV_BSET => rs1_val | mask
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.19.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.20. bseti

Single-Bit set (Immediate)

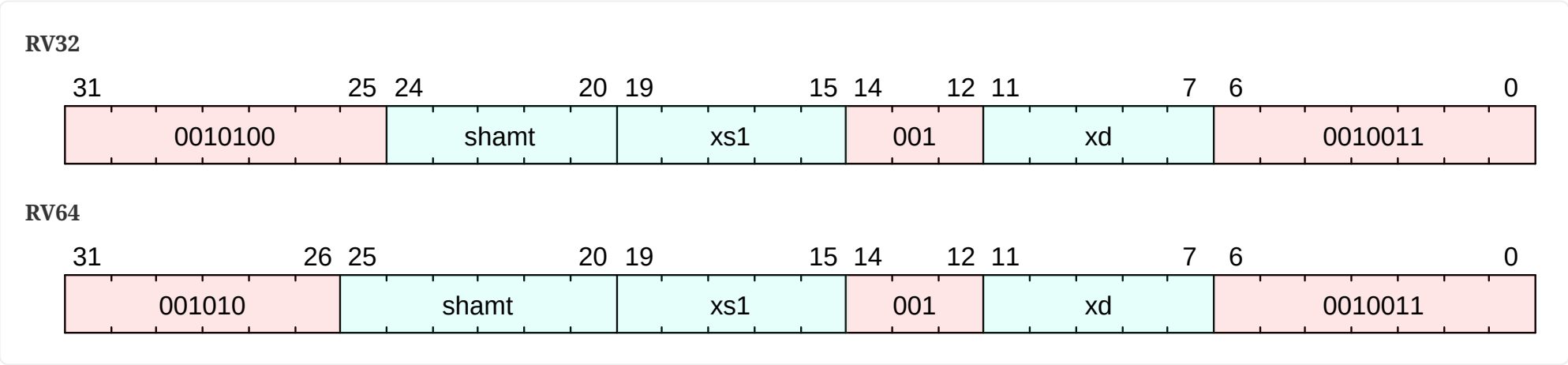
This instruction is defined by:

Zbs

B.20.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.20.2. Description

Returns xs1 with a single bit set at the index specified in shamt. The index is read from the lower log2(XLEN) bits of shamt. For RV32, the encodings corresponding to shamt[5]=1 are reserved.

B.20.3. Access

M	S	U
Always	Always	Always

B.20.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.20.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg index = shamt & (xlen() - 1);
X[xd] = X[xs1] | (1 << index);
```

B.20.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let mask : xlenbits = if sizeof(xlen) == 32
    then zero_extend(0b1) << shamt[4..0]
    else zero_extend(0b1) << shamt;
  let result : xlenbits = match op {
    RISCV_BCLRI => rs1_val & ~(mask),
    RISCV_BEXTI => zero_extend(bool_to_bits((rs1_val & mask) != zeros())),
    RISCV_BINVI => rs1_val ^ mask,
```



```
    RISC_V_BSETI => rs1_val | mask
};
X(rd) = result;
RETIRE_SUCCESS
}
```

B.20.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

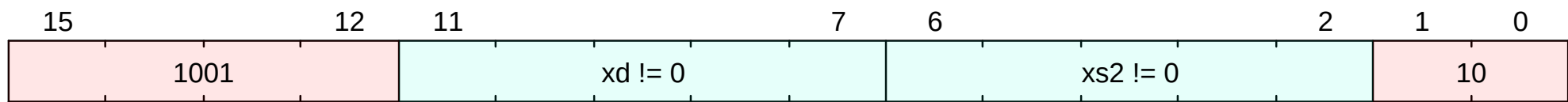
B.21. c.add

Add

This instruction is defined by:

Zca

B.21.1. Encoding



B.21.2. Description

Add the value in xs2 to xd, and store the result in xd. C.ADD expands into `add xd, xd, xs2`.

B.21.3. Access

M	S	U
Always	Always	Always

B.21.4. Decode Variables

```
Bits<5> xs2 = $encoding[6:2];
Bits<5> xd = $encoding[11:7];
```

B.21.5. IDL Operation

```
XReg t0 = X[xd];
XReg t1 = X[xs2];
X[xd] = t0 + t1;
```

B.21.6. Sail Operation

```
{
  let rs1_val = X(rd);
  let rs2_val = X(rs2);
  X(rd) = rs1_val + rs2_val;
  RETIRE_SUCCESS
}
```

B.21.7. Exceptions

This instruction does not generate synchronous exceptions.

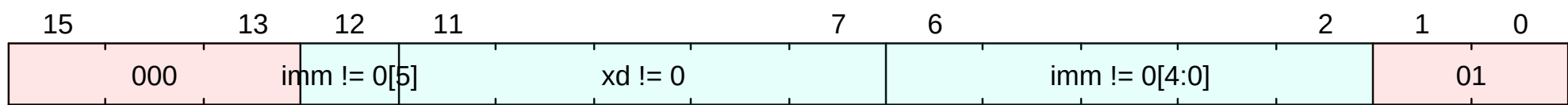
B.22. c.addi

Add a sign-extended non-zero immediate

This instruction is defined by:

Zca

B.22.1. Encoding



B.22.2. Description

C.ADDI adds the non-zero sign-extended 6-bit immediate to the value in register xd then writes the result to xd. C.ADDI expands into `<code>addi xd, xd, imm</code>.`

C.ADDI is only valid when xd != x0 and imm != 0. The code points with xd=x0 encode the C.NOP instruction; the remaining code points with imm=0 encode HINTs.

B.22.3. Access

M	S	U
Always	Always	Always

B.22.4. Decode Variables

```
Bits<6> imm = {$encoding[12], $encoding[6:2]};
Bits<5> xd = $encoding[11:7];
```

B.22.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xd] + $signed(imm);
```

B.22.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

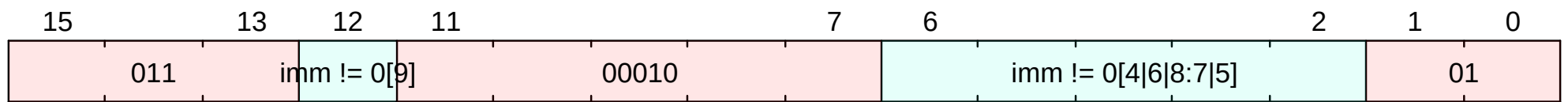
B.23. c.addi16sp

Add a sign-extended non-zero immediate

This instruction is defined by:

Zca

B.23.1. Encoding



B.23.2. Description

C.ADDI16SP adds the non-zero sign-extended 6-bit immediate to the value in the stack pointer (sp=x2), where the immediate is scaled to represent multiples of 16 in the range (-512,496). C.ADDI16SP is used to adjust the stack pointer in procedure prologues and epilogues. It expands into `<code>addi x2, x2, nzimm[9:4]</code> . C.ADDI16SP is only valid when nzimm ≠ 0; the code point with nzimm=0 is reserved.`

B.23.3. Access

M	S	U
Always	Always	Always

B.23.4. Decode Variables

```
Bits<10> imm = {$encoding[12], $encoding[4:3], $encoding[5], $encoding[2], $encoding[6], 4'd0};
```

B.23.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[2] = X[2] + $signed(imm);
```

B.23.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

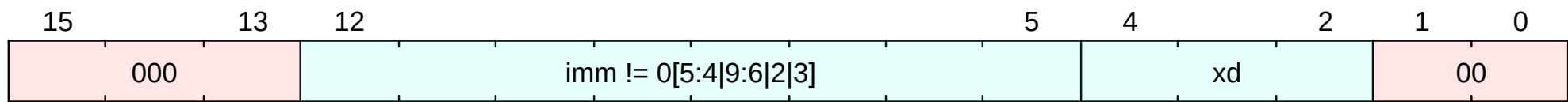
B.24. c.addi4spn

Add a zero-extended non-zero immediate, scaled by 4, to the stack pointer

This instruction is defined by:

Zca

B.24.1. Encoding



B.24.2. Description

Adds a zero-extended non-zero immediate, scaled by 4, to the stack pointer, x2, and writes the result to rd'. This instruction is used to generate pointers to stack-allocated variables. It expands to `addi rd', x2, nzuimm[9:2]`. C.ADDI4SPN is only valid when nzuimm ≠ 0; the code points with nzuimm=0 are reserved.

B.24.3. Access

M	S	U
Always	Always	Always

B.24.4. Decode Variables

```
Bits<10> imm = {$encoding[10:7], $encoding[12:11], $encoding[5], $encoding[6], 2'd0};
Bits<3> xd = $encoding[4:2];
```

B.24.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[creg2reg(xd)] = X[2] + imm;
```

B.24.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

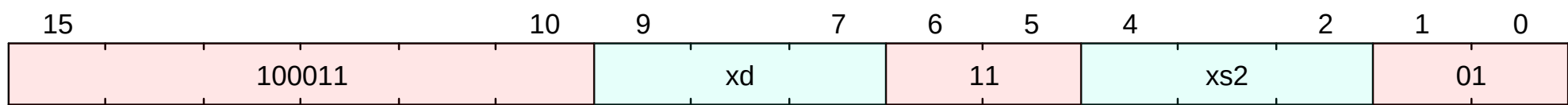
B.25. c.and

And

This instruction is defined by:

Zca

B.25.1. Encoding



B.25.2. Description

And xd with xs2, and store the result in xd The xd and xs2 register indexes should be used as xd+8 and xs2+8 (registers x8-x15). C.AND expands into and xd, xd, xs2.

B.25.3. Access

M	S	U
Always	Always	Always

B.25.4. Decode Variables

```
Bits<3> xs2 = $encoding[4:2];
Bits<3> xd = $encoding[9:7];
```

B.25.5. IDL Operation

```
XReg t0 = X[creg2reg(xd)];
XReg t1 = X[creg2reg(xs2)];
X[creg2reg(xd)] = t0 & t1;
```

B.25.6. Sail Operation

```
{
  let rs1_val = X(rd+8);
  let rs2_val = X(rs2+8);
  let result : xlenbits = match op {
    RISCV_ADD  => rs1_val + rs2_val,
    RISCV_SLT  => zero_extend(bool_to_bits(rs1_val <_s rs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(rs1_val <_u rs2_val)),
    RISCV_AND  => rs1_val & rs2_val,
    RISCV_OR   => rs1_val | rs2_val,
    RISCV_XOR  => rs1_val ^ rs2_val,
    RISCV_SLL  => if  sizeof(xlen) == 32
                  then rs1_val << (rs2_val[4..0])
                  else rs1_val << (rs2_val[5..0]),
    RISCV_SRL  => if  sizeof(xlen) == 32
                  then rs1_val >> (rs2_val[4..0])
                  else rs1_val >> (rs2_val[5..0]),
    RISCV_SUB  => rs1_val - rs2_val,
    RISCV_SRA  => if  sizeof(xlen) == 32
                  then shift_right_arith32(rs1_val, rs2_val[4..0])
                  else shift_right_arith64(rs1_val, rs2_val[5..0])
  };
  X(rd+8) = result;
  RETIRE_SUCCESS
}
```

B.25.7. Exceptions

This instruction does not generate synchronous exceptions.

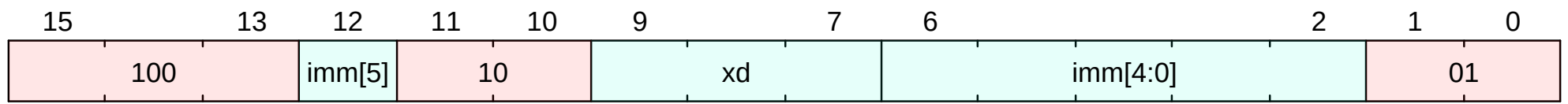
B.26. c.andi

And immediate

This instruction is defined by:

Zca

B.26.1. Encoding



B.26.2. Description

And an immediate to the value in xd, and store the result in xd. The xd register index should be used as xd+8 (registers x8-x15). C.ANDI expands into `andi xd, xd, imm`.

B.26.3. Access

M	S	U
Always	Always	Always

B.26.4. Decode Variables

```
Bits<6> imm = {$encoding[12], $encoding[6:2]};
Bits<3> xd = $encoding[9:7];
```

B.26.5. IDL Operation

```
X[creg2reg(xd)] = X[creg2reg(xd)] & $signed(imm);
```

B.26.6. Sail Operation

```
{
  let rd_val = X(rd+8);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => rd_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(rd_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(rd_val <_u immext)),
    RISCV_ANDI => rd_val & immext,
    RISCV_ORI  => rd_val | immext,
    RISCV_XORI => rd_val ^ immext
  };
  X(rd+8) = result;
  RETIRE_SUCCESS
}
```

B.26.7. Exceptions

This instruction does not generate synchronous exceptions.

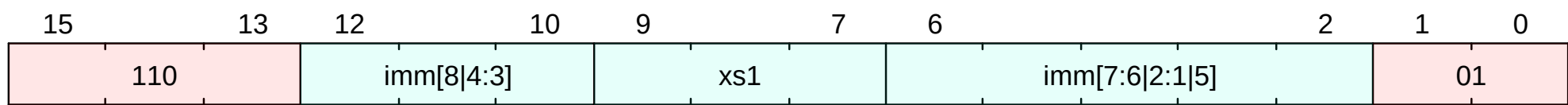
B.27. c.beqz

Branch if Equal Zero

This instruction is defined by:

Zca

B.27.1. Encoding



B.27.2. Description

C.BEQZ performs conditional control transfers. The offset is sign-extended and added to the pc to form the branch target address. It can therefore target a ±256 B range. C.BEQZ takes the branch if the value in register xs1' is zero. It expands to `<a anchor="udb:doc:inst:beq">beq</a> xs1, x0, offset</code>.`

B.27.3. Access

M	S	U
Always	Always	Always

B.27.4. Decode Variables

```
signed Bits<9> imm = sext({$encoding[12], $encoding[6:5], $encoding[2], $encoding[11:10], $encoding[4:3], 1'd0});
Bits<3> xs1 = $encoding[9:7];
```

B.27.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (X[creg2reg(xs1)] == 0) {
  jump($pc + $signed(imm));
}
```

B.27.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(0);
  let taken : bool = match op {
    RISCV_BEQ => rs1_val == rs2_val,
    RISCV_BNE => rs1_val != rs2_val,
    RISCV_BLT => rs1_val <_s rs2_val,
    RISCV_BGE => rs1_val >=_s rs2_val,
    RISCV_BLTU => rs1_val <_u rs2_val,
    RISCV_BGEU => rs1_val >=_u rs2_val
  };
  let t : xlenbits = PC + sign_extend(imm);
  if taken then {
    /* Extensions get the first checks on the prospective target address. */
    match ext_control_check_pc(t) {
      Ext_ControlAddr_Error(e) => {
        ext_handle_control_check_error(e);
        RETIRE_FAIL
      },
      Ext_ControlAddr_OK(target) => {
        if bit_to_bool(target[1]) & not(extension("C")) then {
          handle_mem_exception(target, E_Fetch_Addr_Align());
          RETIRE_FAIL;
        } else {
          set_next_pc(target);
          RETIRE_SUCCESS
        }
      }
    }
  }
}
```



```
    }  
    } else RETIRE_SUCCESS  
}
```

B.27.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- InstructionAddressMisaligned

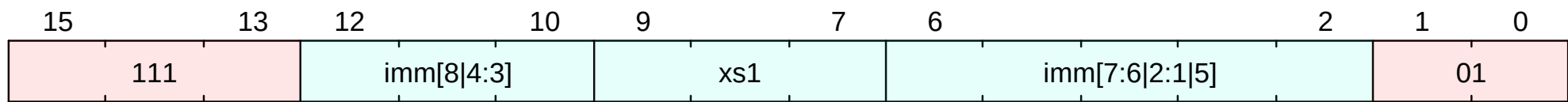
B.28. c.bnez

Branch if NOT Equal Zero

This instruction is defined by:

Zca

B.28.1. Encoding



B.28.2. Description

C.BEQZ performs conditional control transfers. The offset is sign-extended and added to the pc to form the branch target address. It can therefore target a ±256 B range. C.BEQZ takes the branch if the value in register xs1' is NOT zero. It expands to beq
<code>xs1, x0, offset</code>.

B.28.3. Access

M	S	U
Always	Always	Always

B.28.4. Decode Variables

```
signed Bits<9> imm = sext({$encoding[12], $encoding[6:5], $encoding[2], $encoding[11:10], $encoding[4:3], 1'd0});
Bits<3> xs1 = $encoding[9:7];
```

B.28.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (X[creg2reg(xs1)] != 0) {
    jump($pc + $signed(imm));
}
```

B.28.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    let rs2_val = X(0);
    let taken : bool = match op {
        RISCV_BEQ => rs1_val == rs2_val,
        RISCV_BNE => rs1_val != rs2_val,
        RISCV_BLT => rs1_val <_s rs2_val,
        RISCV_BGE => rs1_val >=_s rs2_val,
        RISCV_BLTU => rs1_val <_u rs2_val,
        RISCV_BGEU => rs1_val >=_u rs2_val
    };
    let t : xlenbits = PC + sign_extend(imm);
    if taken then {
        /* Extensions get the first checks on the prospective target address. */
        match ext_control_check_pc(t) {
            Ext_ControlAddr_Error(e) => {
                ext_handle_control_check_error(e);
                RETIRE_FAIL
            },
            Ext_ControlAddr_OK(target) => {
                if bit_to_bool(target[1]) & not(extension("C")) then {
                    handle_mem_exception(target, E_Fetch_Addr_Align());
                    RETIRE_FAIL;
                } else {
                    set_next_pc(target);
                    RETIRE_SUCCESS
                }
            }
        }
    }
}
```

```
    }  
  } else RETIRE_SUCCESS  
}
```

B.28.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- InstructionAddressMisaligned

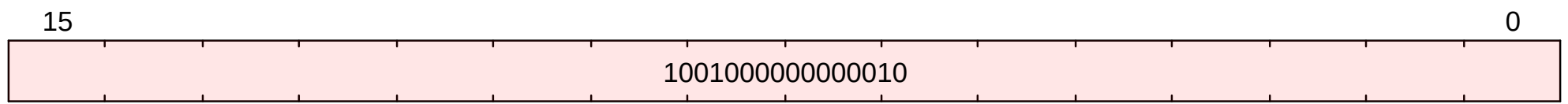
B.29. c.ebreak

Breakpoint exception

This instruction is defined by:

Zca

B.29.1. Encoding



B.29.2. Description

The C.EBREAK instruction is used by debuggers to cause control to be transferred back to a debugging environment. Unless overridden by an external debug environment, C.EBREAK raises a breakpoint exception and performs no other operation.

i

As described in the [C](#) Standard Extension for Compressed Instructions, the [c.ebreak](#) instruction performs the same operation as the EBREAK instruction.

EBREAK causes the receiving privilege mode’s epc register to be set to the address of the EBREAK instruction itself, not the address of the following instruction. As EBREAK causes a synchronous exception, it is not considered to retire, and should not increment the [minstret](#) CSR.

B.29.3. Access

M	S	U
Always	Always	Always

B.29.4. Decode Variables

B.29.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (TRAP_ON_EBREAK) {
  raise_precise(ExceptionCode::Breakpoint, mode(), $pc);
} else {
  eei_ebreak();
}
```

B.29.6. Sail Operation

```
{
  handle_mem_exception(PC, E_Breakpoint());
  RETIRE_FAIL
}
```

B.29.7. Exceptions

This instruction may result in the following synchronous exceptions:

- Breakpoint
- IllegalInstruction

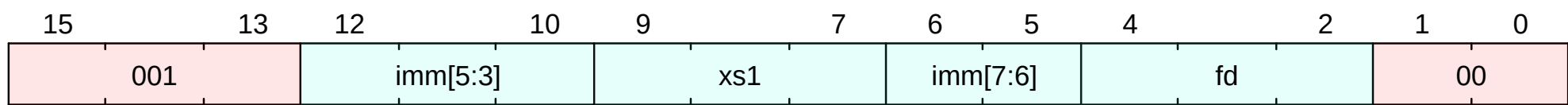
B.30. c.fld

Load double-precision

This instruction is defined by:

Zcd

B.30.1. Encoding



B.30.2. Description

Loads a double precision floating-point value from memory into register fd. It computes an effective address by adding the zero-extended offset, scaled by 8, to the base address in register xs1. It expands to `fld fd, offset(xs1)`.

B.30.3. Access

M	S	U
Always	Always	Always

B.30.4. Decode Variables

```
Bits<8> imm = {$encoding[6:5], $encoding[12:10], 3'd0};
Bits<3> fd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.30.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
f[fd] = sext(read_memory<64>(virtual_address, $encoding), 64);
```

B.30.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

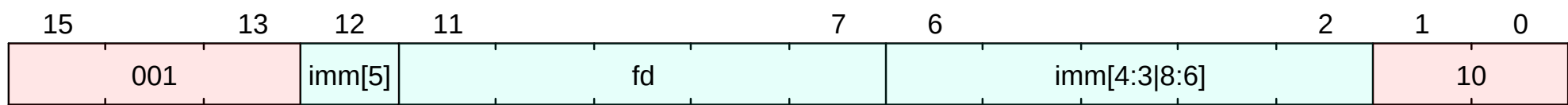
B.31. c.fldsp

Load doubleword into floating-point register from stack

This instruction is defined by:

Zcd

B.31.1. Encoding



B.31.2. Description

Loads a double-precision floating-point value from memory into floating-point register fd. It computes its effective address by adding the zero-extended offset, scaled by 8, to the stack pointer, x2. It expands to `fld fd, offset(x2)`.

B.31.3. Access

M	S	U
Always	Always	Always

B.31.4. Decode Variables

```
Bits<9> imm = {$encoding[4:2], $encoding[12], $encoding[6:5], 3'd0};
Bits<5> fd = $encoding[11:7];
```

B.31.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (implemented?(ExtensionName::D) && (CSR[misa].D == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
f[fd] = read_memory<64>(virtual_address, $encoding);
```

B.31.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

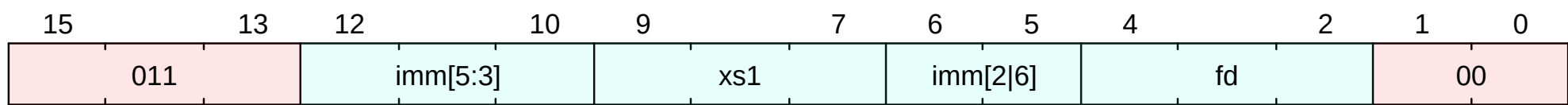
B.32. c.flw

Load single-precision

This instruction is defined by:

Zcf

B.32.1. Encoding



B.32.2. Description

Loads a single precision floating-point value from memory into register fd. It computes an effective address by adding the zero-extended offset, scaled by 4, to the base address in register xs1. It expands to `flw fd, offset(xs1)`.

B.32.3. Access

M	S	U
Always	Always	Always

B.32.4. Decode Variables

```
Bits<7> imm = {$encoding[5], $encoding[12:10], $encoding[6], 2'd0};
Bits<3> fd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.32.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
X[creg2reg(fd)] = sext(read_memory<32>(virtual_address, $encoding), 32);
```

B.32.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

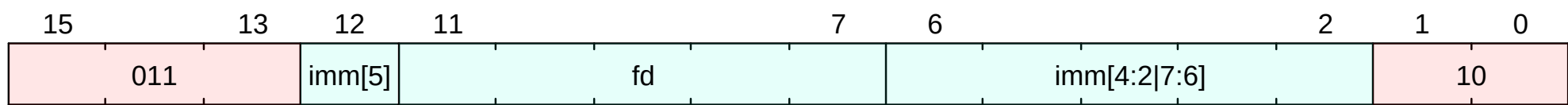
B.33. c.flwsp

Load word into floating-point register from stack

This instruction is defined by:

Zcf

B.33.1. Encoding



B.33.2. Description

Loads a single-precision floating-point value from memory into floating-point register fd. It computes its effective address by adding the zero-extended offset, scaled by 4, to the stack pointer, x2. It expands to `flw fd, offset(x2)`.

B.33.3. Access

M	S	U
Always	Always	Always

B.33.4. Decode Variables

```
Bits<8> imm = {$encoding[3:2], $encoding[12], $encoding[6:4], 2'd0};
Bits<5> fd = $encoding[11:7];
```

B.33.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (implemented?(ExtensionName::F) && (CSR[misa].F == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
f[fd] = read_memory<32>(virtual_address, $encoding);
```

B.33.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

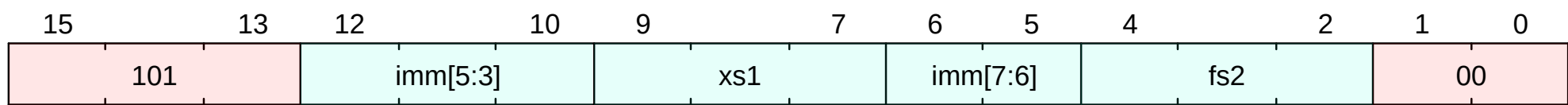
B.34. c.fsd

Store double-precision

This instruction is defined by:

Zcd

B.34.1. Encoding



B.34.2. Description

Stores a double precision floating-point value in register fs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 8, to the base address in register xs1. It expands to `fsd fs2, offset(xs1)`.

B.34.3. Access

M	S	U
Always	Always	Always

B.34.4. Decode Variables

```
Bits<8> imm = {$encoding[6:5], $encoding[12:10], 3'd0};
Bits<3> fs2 = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.34.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
write_memory<64>(virtual_address, X[creg2reg(fs2)], $encoding);
```

B.34.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

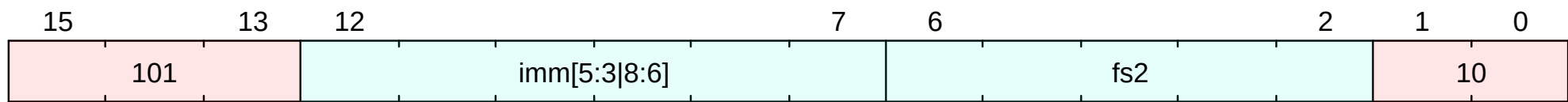
B.35. c.fsdsp

Store double-precision value to stack

This instruction is defined by:

Zcd

B.35.1. Encoding



B.35.2. Description

Stores a double-precision floating-point value in floating-point register fs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 8, to the stack pointer, x2. It expands to `fsd fs2, offset(x2)`.

B.35.3. Access

M	S	U
Always	Always	Always

B.35.4. Decode Variables

```
Bits<9> imm = {$encoding[9:7], $encoding[12:10], 3'd0};
Bits<5> fs2 = $encoding[6:2];
```

B.35.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (implemented?(ExtensionName::D) && (CSR[misa].D == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
write_memory<64>(virtual_address, f[fs2][63:0], $encoding);
```

B.35.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

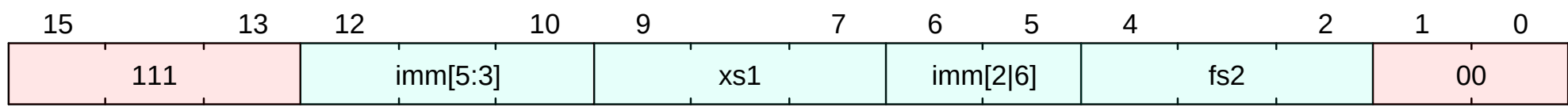
B.36. c.fsw

Store single-precision

This instruction is defined by:

Zcf

B.36.1. Encoding



B.36.2. Description

Stores a single precision floating-point value in register fs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 4, to the base address in register xs1. It expands to `fsw fs2, offset(xs1)`.

B.36.3. Access

M	S	U
Always	Always	Always

B.36.4. Decode Variables

```
Bits<7> imm = {$encoding[5], $encoding[12:10], $encoding[6], 2'd0};
Bits<3> fs2 = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.36.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
write_memory<32>(virtual_address, X[creg2reg(fs2)][31:0], $encoding);
```

B.36.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

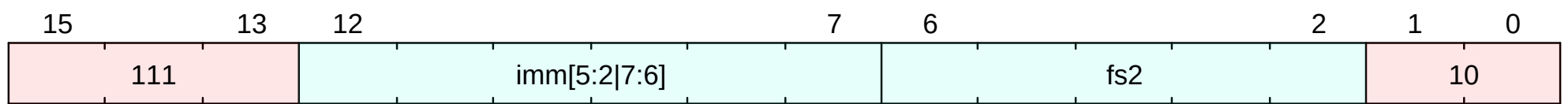
B.37. c.fswsp

Store single-precision value to stack

This instruction is defined by:

Zcf

B.37.1. Encoding



B.37.2. Description

Stores a single-precision floating-point value in floating-point register fs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 4, to the stack pointer, x2. It expands to `fsw fs2, offset(x2)`.

B.37.3. Access

M	S	U
Always	Always	Always

B.37.4. Decode Variables

```
Bits<8> imm = {$encoding[8:7], $encoding[12:9], 2'd0};
Bits<5> fs2 = $encoding[6:2];
```

B.37.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (implemented?(ExtensionName::F) && (CSR[misa].F == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
write_memory<32>(virtual_address, f[fs2][31:0], $encoding);
```

B.37.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

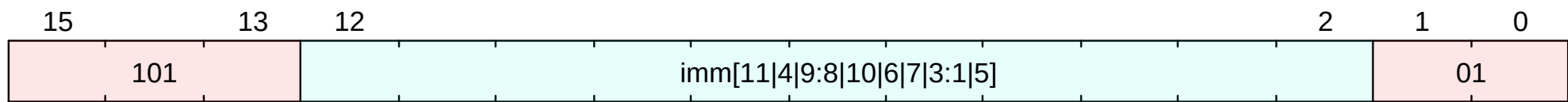
B.38. c.j

Jump

This instruction is defined by:

Zca

B.38.1. Encoding



B.38.2. Description

C.J performs an unconditional control transfer. The offset is sign-extended and added to the pc to form the jump target address. C.J can therefore target a ±2 KiB range. It expands to [jal](#) `x0, offset`.

B.38.3. Access

M	S	U
Always	Always	Always

B.38.4. Decode Variables

```
signed Bits<12> imm = sext({$encoding[12], $encoding[8], $encoding[10:9], $encoding[6], $encoding[7], $encoding[2], $encoding[11], $encoding[5:3], 1'd0});
```

B.38.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
jump($pc + $signed(imm));
```

B.38.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- InstructionAddressMisaligned

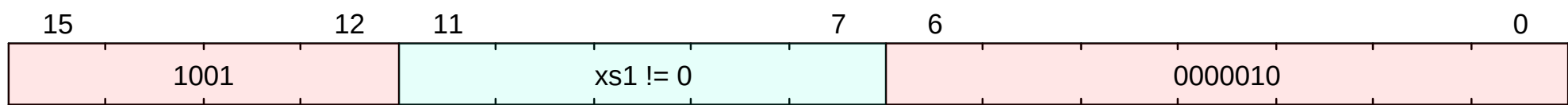
B.39. c.jalr

Jump and Link Register

This instruction is defined by:

Zca

B.39.1. Encoding



B.39.2. Description

C.JALR (jump and link register) performs the same operation as C.JR, but additionally writes the address of the instruction following the jump (pc+2) to the link register, x1. C.JALR expands to jalr x1, 0(xs1).

B.39.3. Access

M	S	U
Always	Always	Always

B.39.4. Decode Variables

```
Bits<5> xs1 = $encoding[11:7];
```

B.39.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg addr = X[xs1];
XReg returnaddr;
returnaddr = $pc + 2;
X[1] = returnaddr;
jump(addr);
```

B.39.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- InstructionAddressMisaligned

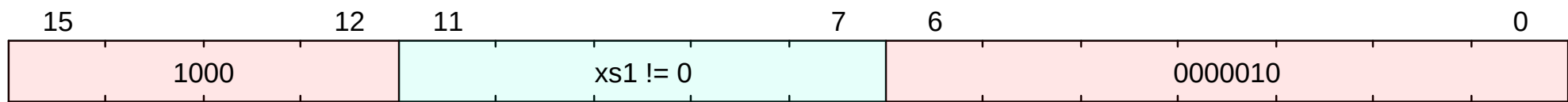
B.40. c.jr

Jump Register

This instruction is defined by:

Zca

B.40.1. Encoding



B.40.2. Description

C.JR (jump register) performs an unconditional control transfer to the address in register xs1. C.JR expands to jalr x0, 0(xs1).

B.40.3. Access

M	S	U
Always	Always	Always

B.40.4. Decode Variables

```
Bits<5> xs1 = $encoding[11:7];
```

B.40.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
jump(X[xs1]);
```

B.40.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- InstructionAddressMisaligned

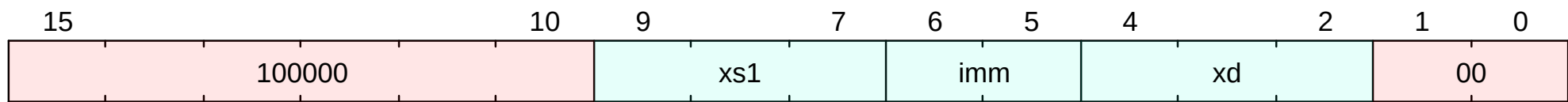
B.41. c.lbu

Load unsigned byte, 16-bit encoding

This instruction is defined by:

Zcb

B.41.1. Encoding



B.41.2. Description

Loads a 8-bit value from memory into register xd. It computes an effective address by adding the zero-extended offset, to the base address in register xs1. It expands to `lbu xd, offset(xs1)`.

B.41.3. Access

M	S	U
Always	Always	Always

B.41.4. Decode Variables

```
Bits<2> imm = {$encoding[5], $encoding[6]};
Bits<3> xd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.41.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
X[creg2reg(xd)] = read_memory<8>(virtual_address, $encoding);
```

B.41.6. Sail Operation

```
{
  let offset : xlenbits = zero_extend(imm);
  /* Get the address, X(rs1c) + offset.
   Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1c, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.41.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

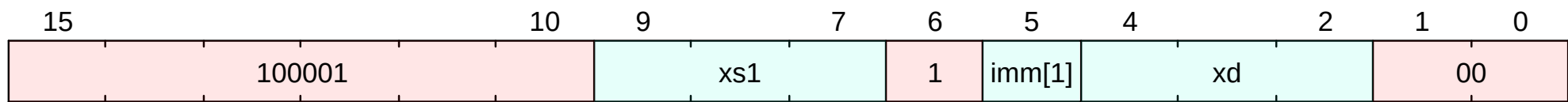
B.42. c.lh

Load signed halfword, 16-bit encoding

This instruction is defined by:

Zcb

B.42.1. Encoding



B.42.2. Description

Loads a 16-bit value from memory into register xd. It computes an effective address by adding the zero-extended offset, to the base address in register xs1. It expands to `lh xd, offset(xs1)`.

B.42.3. Access

M	S	U
Always	Always	Always

B.42.4. Decode Variables

```
Bits<2> imm = {$encoding[5], 1'd0};
Bits<3> xd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.42.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
X[creg2reg(xd)] = sext(read_memory<16>(virtual_address, $encoding), 16);
```

B.42.6. Sail Operation

```
{
  let offset : xlenbits = zero_extend(imm);
  /* Get the address, X(rs1c) + offset.
   Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1c, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.42.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

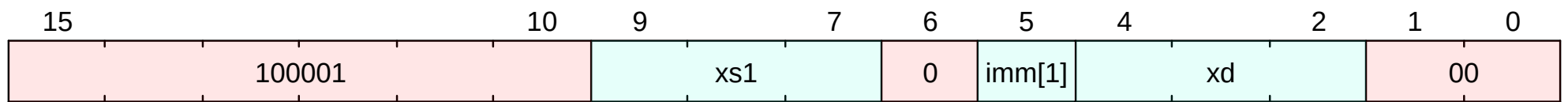
B.43. c.lhu

Load unsigned halfword, 16-bit encoding

This instruction is defined by:

Zcb

B.43.1. Encoding



B.43.2. Description

Loads a 16-bit value from memory into register xd. It computes an effective address by adding the zero-extended offset, to the base address in register xs1. It expands to `lhu xd, offset(xs1)`.

B.43.3. Access

M	S	U
Always	Always	Always

B.43.4. Decode Variables

```
Bits<2> imm = {$encoding[5], 1'd0};
Bits<3> xd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.43.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
X[creg2reg(xd)] = read_memory<16>(virtual_address, $encoding);
```

B.43.6. Sail Operation

```
{
  let offset : xlenbits = zero_extend(imm);
  /* Get the address, X(rs1c) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1c, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(rdc, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```


B.43.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

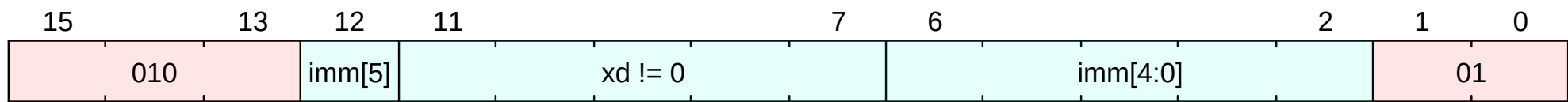
B.44. c.li

Load the sign-extended 6-bit immediate

This instruction is defined by:

Zca

B.44.1. Encoding



B.44.2. Description

C.LI loads the sign-extended 6-bit immediate, imm, into register xd. C.LI expands into `addi xd, x0, imm`. C.LI is only valid when xd != x0; the code points with xd=x0 encode HINTs.

B.44.3. Access

M	S	U
Always	Always	Always

B.44.4. Decode Variables

```
Bits<6> imm = {$encoding[12], $encoding[6:2]};
Bits<5> xd = $encoding[11:7];
```

B.44.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = $signed(imm);
```

B.44.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

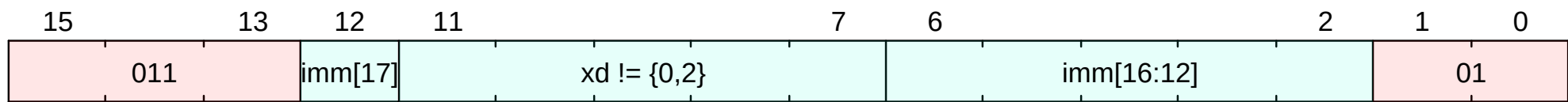
B.45. c.lui

Load Upper Immediate

This instruction is defined by:

Zca

B.45.1. Encoding



B.45.2. Description

C.LUI loads the non-zero 6-bit immediate field into bits 17-12 of the destination register, clears the bottom 12 bits, and sign-extends bit 17 into all higher bits of the destination. C.LUI expands into `<code>lui xd, imm</code>.`

C.LUI is only valid when $xd \neq x0$ and $xd \neq x2$, and when the immediate is not equal to zero. The code points with $imm=0$ are reserved; the remaining code points with $xd=x0$ are HINTs; and the remaining code points with $xd=x2$ correspond to the C.ADDI16SP instruction

B.45.3. Access

M	S	U
Always	Always	Always

B.45.4. Decode Variables

```
Bits<18> imm = {$encoding[12], $encoding[6:2], 12'd0};
Bits<5> xd = $encoding[11:7];
```

B.45.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = $signed(imm);
```

B.45.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

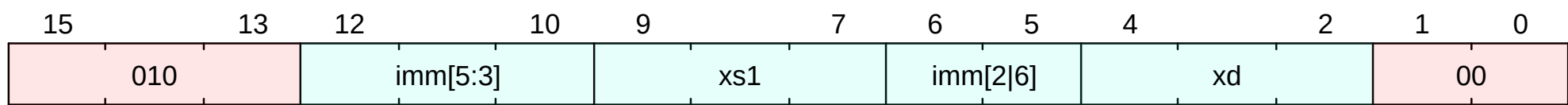
B.46. c.lw

Load word

This instruction is defined by:

Zca

B.46.1. Encoding



B.46.2. Description

Loads a 32-bit value from memory into register xd. It computes an effective address by adding the zero-extended offset, scaled by 4, to the base address in register xs1. It expands to `lw xd, offset(xs1)`.

B.46.3. Access

M	S	U
Always	Always	Always

B.46.4. Decode Variables

```
Bits<7> imm = {$encoding[5], $encoding[12:10], $encoding[6], 2'd0};
Bits<3> xd = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.46.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
X[creg2reg(xd)] = sext(read_memory<32>(virtual_address, $encoding), 32);
```

B.46.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(rs1) + offset.
   Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(rd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(rd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(rd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(rd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.46.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

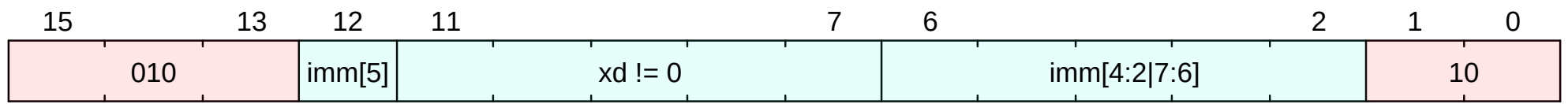
B.47. c.lwsp

Load word from stack pointer

This instruction is defined by:

Zca

B.47.1. Encoding



B.47.2. Description

Loads a 32-bit value from memory into register xd. It computes an effective address by adding the zero-extended offset, scaled by 4, to the stack pointer, x2. It expands to lw <code>xd, offset(x2)</code>. C.LWSP is only valid when xd ≠ x0. The code points with xd=x0 are reserved.

B.47.3. Access

M	S	U
Always	Always	Always

B.47.4. Decode Variables

```
Bits<8> imm = {$encoding[3:2], $encoding[12], $encoding[6:4], 2'd0};
Bits<5> xd = $encoding[11:7];
```

B.47.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
X[xd] = sext(read_memory<32>(virtual_address, $encoding), 32);
```

B.47.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

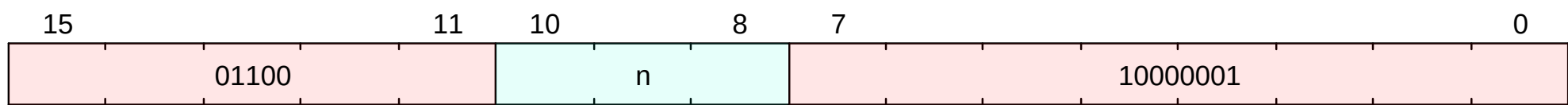
B.48. c.mop.n

Compressed May-Be-Operation

This instruction is defined by:

[Zcmop](#)

B.48.1. Encoding



B.48.2. Description

C.MOP.n is encoded in the reserved encoding space corresponding to C.LUI xn, 0. Unlike the MOPs defined in the Zimop extension, the C.MOP.n instructions are defined to not write any register. Their encoding allows future extensions to define them to read register x[n].

B.48.3. Access

M	S	U
Always	Always	Always

B.48.4. Decode Variables

```
Bits<3> n = $encoding[10:8];
```

B.48.5. IDL Operation

B.48.6. Exceptions

This instruction does not generate synchronous exceptions.

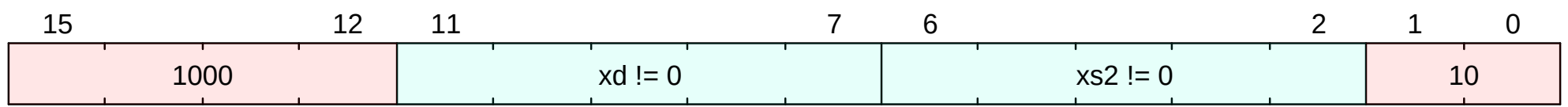
B.49. c.mv

Move Register

This instruction is defined by:

Zca

B.49.1. Encoding



B.49.2. Description

C.MV (move register) performs copy of the data in register xs2 to register xd C.MV expands to addi xd, x0, xs2.

B.49.3. Access

M	S	U
Always	Always	Always

B.49.4. Decode Variables

```
Bits<5> xd = $encoding[11:7];
Bits<5> xs2 = $encoding[6:2];
```

B.49.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs2];
```

B.49.6. Sail Operation

```
{
  let xs2_val = X(xs2);
  X(rs) = xs2_val
  RETIRE_SUCCESS
}
```

B.49.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

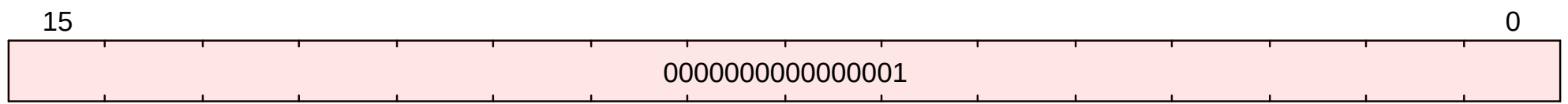
B.50. c.nop

Non-operation

This instruction is defined by:

Zca

B.50.1. Encoding



B.50.2. Description

C.NOP expands into `addi x0, x0, 0`.

B.50.3. Access

M	S	U
Always	Always	Always

B.50.4. Decode Variables

B.50.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {  
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
}
```

B.50.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

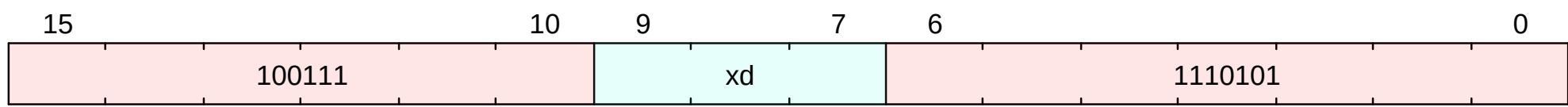
B.51. c.not

Bitwise not, 16-bit encoding

This instruction is defined by:

Zcb

B.51.1. Encoding



B.51.2. Description

Takes a single source/destination operand. This instruction takes the one’s complement of xd'/xs1' and writes the result to the same register.

B.51.3. Access

M	S	U
Always	Always	Always

B.51.4. Decode Variables

```
Bits<3> xd = $encoding[9:7];
```

B.51.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[creg2reg(xd)] = ~X[creg2reg(xd)];
```

B.51.6. Sail Operation

```
{
    X(rsdc) = X(rsdc) XOR -1;
    RETIRE_SUCCESS
}
```

B.51.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

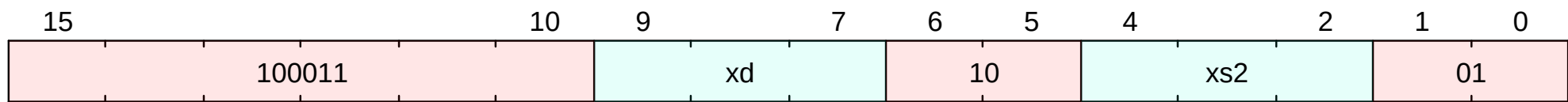
B.52. c.or

Or

This instruction is defined by:

Zca

B.52.1. Encoding



B.52.2. Description

Or xd with xs2, and store the result in xd The xd and xs2 register indexes should be used as xd+8 and xs2+8 (registers x8-x15). C.OR expands into **or** **xd**, **xd**, **xs2**.

B.52.3. Access

M	S	U
Always	Always	Always

B.52.4. Decode Variables

```
Bits<3> xs2 = $encoding[4:2];
Bits<3> xd = $encoding[9:7];
```

B.52.5. IDL Operation

```
XReg t0 = X[creg2reg(xd)];
XReg t1 = X[creg2reg(xs2)];
X[creg2reg(xd)] = t0 | t1;
```

B.52.6. Sail Operation

```
{
  let rs1_val = X(rd+8);
  let rs2_val = X(rs2+8);
  let result : xlenbits = match op {
    RISCV_ADD => rs1_val + rs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(rs1_val <_s rs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(rs1_val <_u rs2_val)),
    RISCV_AND => rs1_val & rs2_val,
    RISCV_OR => rs1_val | rs2_val,
    RISCV_XOR => rs1_val ^ rs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then rs1_val << (rs2_val[4..0])
                  else rs1_val << (rs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then rs1_val >> (rs2_val[4..0])
                  else rs1_val >> (rs2_val[5..0]),
    RISCV_SUB => rs1_val - rs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(rs1_val, rs2_val[4..0])
                  else shift_right_arith64(rs1_val, rs2_val[5..0])
  };
  X(rd+8) = result;
  RETIRE_SUCCESS
}
```

B.52.7. Exceptions

This instruction does not generate synchronous exceptions.

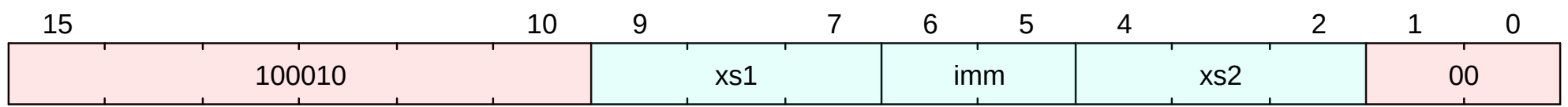
B.53. c.sb

Store unsigned byte, 16-bit encoding

This instruction is defined by:

Zcb

B.53.1. Encoding



B.53.2. Description

Stores a 8-bit value from register xs2 into memory. It computes an effective address by adding the zero-extended offset, to the base address in register xs1. It expands to `sb xs2, offset(xs1)`.

B.53.3. Access

M	S	U
Always	Always	Always

B.53.4. Decode Variables

```
Bits<2> imm = {$encoding[5], $encoding[6]};
Bits<3> xs2 = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.53.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
write_memory<8>(virtual_address, X[creg2reg(xs2)][7:0], $encoding);
```

B.53.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

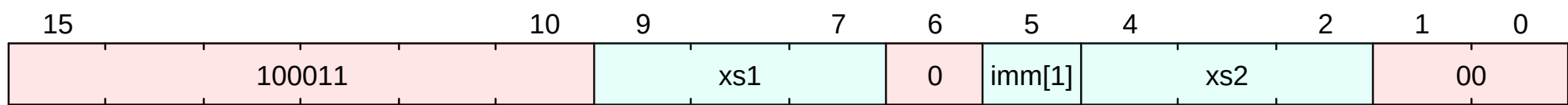
B.54. c.sh

Store unsigned halfword, 16-bit encoding

This instruction is defined by:

Zcb

B.54.1. Encoding



B.54.2. Description

Stores a 16-bit value from register xs2 into memory. It computes an effective address by adding the zero-extended offset, to the base address in register xs1. It expands to `sh xs2, offset(xs1)`.

B.54.3. Access

M	S	U
Always	Always	Always

B.54.4. Decode Variables

```
Bits<2> imm = {$encoding[5], 1'd0};
Bits<3> xs2 = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.54.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
write_memory<16>(virtual_address, X[creg2reg(xs2)][15:0], $encoding);
```

B.54.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

B.55. c.slli

Shift left logical immediate

This instruction is defined by:

Zca

B.55.1. Encoding

This instruction has different encodings in RV32 and RV64.

RV32

15121176210

0000

xd

shamt != 0

10

RV64

1513121176210

000shamt != 0[5]xdshamt != 0[4:0]10

B.55.2. Description

Shift the value in xd left by shamt, and store the result back in xd. C.SLLI expands into `slli xd, xd, shamt`.

B.55.3. Access

M	S	U
Always	Always	Always

B.55.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[6:2];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = {\$encoding[12], \$encoding[6:2]};

Bits<5> xd = \$encoding[11:7];

B.55.5. IDL Operation

```
X[xd] = X[xd] << shamt;
```

B.55.6. Sail Operation

```
{
  let rd_val = X(rd);
  /* the decoder guard should ensure that shamt[5] = 0 for RV32 */
  let result : xlenbits = match op {
    RISC_V_SLLI => if sizeof(xlen) == 32
      then rd_val << shamt[4..0]
      else rd_val << shamt,
    RISC_V_SRLI => if sizeof(xlen) == 32
      then rd_val >> shamt[4..0]
      else rd_val >> shamt,
    RISC_V_SRAI => if sizeof(xlen) == 32
      then shift_right_arith32(rd_val, shamt[4..0])
      else shift_right_arith64(rd_val, shamt)
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

```
}
```

B.55.7. Exceptions

This instruction does not generate synchronous exceptions.

B.56. c.srai

Shift right arithmetical immediate

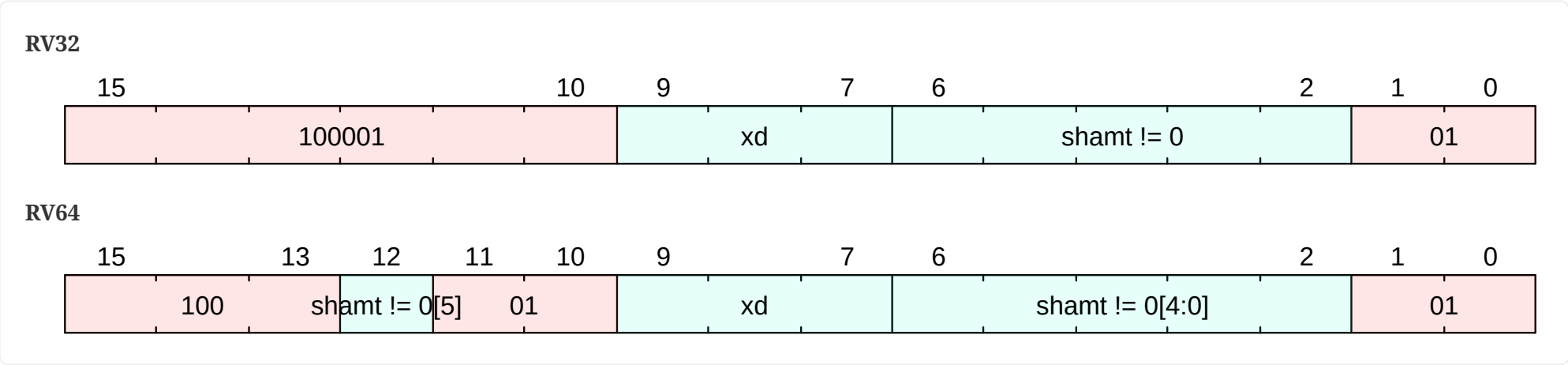
This instruction is defined by:

Zca

B.56.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.56.2. Description

Arithmetic shift (the original sign bit is copied into the vacated upper bits) the value in xd right by shamt, and store the result in xd. The xd register index should be used as xd+8 (registers x8-x15). C.SRAI expands into `srai xd, xd, shamt`.

B.56.3. Access

M	S	U
Always	Always	Always

B.56.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[6:2];
Bits<3> xd = \$encoding[9:7];

RV64

Bits<6> shamt = {\$encoding[12], \$encoding[6:2]};
Bits<3> xd = \$encoding[9:7];

B.56.5. IDL Operation

```
X[creg2reg(xd)] = X[creg2reg(xd)] >>> shamt;
```

B.56.6. Sail Operation

```
{  
  let rd_val = X(rd+8);  
  /* the decoder guard should ensure that shamt[5] = 0 for RV32 */  
  let result : xlenbits = match op {  
    RISCV_SLLI => if sizeof(xlen) == 32  
                  then rd_val << shamt[4..0]  
                  else rd_val << shamt,  
    RISCV_SRLI => if sizeof(xlen) == 32  
                  then rd_val >> shamt[4..0]  
                  else rd_val >> shamt,  
    RISCV_SRAI => if sizeof(xlen) == 32  
                  then shift_right_arith32(rd_val, shamt[4..0])  
                  else shift_right_arith64(rd_val, shamt)  
  };  
  X(rd+8) = result;  
}
```

```
RETIRE_SUCCESS
}
```

B.56.7. Exceptions

This instruction does not generate synchronous exceptions.

B.57. c.srli

Shift right logical immediate

This instruction is defined by:

Zca

B.57.1. Encoding

This instruction has different encodings in RV32 and RV64.

RV32

1510976210

100000

xd

shamt != 0

01

RV64

1513121110976210

100shamt != 0[5]00

xd

shamt != 0[4:0]

01

B.57.2. Description

Shift the value in `xd` right by `shamt`, and store the result back in `xd`. The `xd` register index should be used as `xd+8` (registers `x8-x15`). C.SRLI expands into `srli xd, xd, shamt`.

B.57.3. Access

M	S	U
Always	Always	Always

B.57.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[6:2];

Bits<3> xd = \$encoding[9:7];

RV64

Bits<6> shamt = {\$encoding[12], \$encoding[6:2]};

Bits<3> xd = \$encoding[9:7];

B.57.5. IDL Operation

```
X[creg2reg(xd)] = X[creg2reg(xd)] >> shamt;
```

B.57.6. Sail Operation

```
{
  let rd_val = X(rd+8);
  /* the decoder guard should ensure that shamt[5] = 0 for RV32 */
  let result : xlenbits = match op {
    RISCV_SLLI => if sizeof(xlen) == 32
      then rd_val << shamt[4..0]
      else rd_val << shamt,
    RISCV_SRLI => if sizeof(xlen) == 32
      then rd_val >> shamt[4..0]
      else rd_val >> shamt,
    RISCV_SRAI => if sizeof(xlen) == 32
      then shift_right_arith32(rd_val, shamt[4..0])
      else shift_right_arith64(rd_val, shamt)
  };
  X(rd+8) = result;
```

```
RETIRE_SUCCESS
}
```

B.57.7. Exceptions

This instruction does not generate synchronous exceptions.

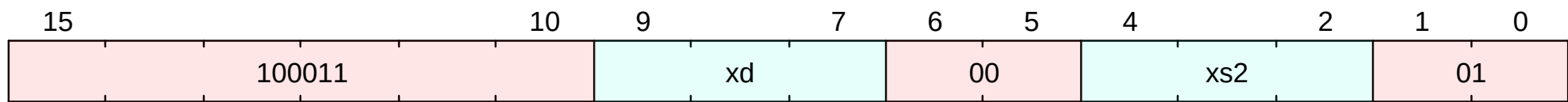
B.58. c.sub

Subtract

This instruction is defined by:

Zca

B.58.1. Encoding



B.58.2. Description

Subtract the value in xs2 from xd, and store the result in xd. The xd and xs2 register indexes should be used as xd+8 and xs2+8 (registers x8-x15). C.SUB expands into **sub xd, xd, xs2**.

B.58.3. Access

M	S	U
Always	Always	Always

B.58.4. Decode Variables

```
Bits<3> xs2 = $encoding[4:2];
Bits<3> xd = $encoding[9:7];
```

B.58.5. IDL Operation

```
XReg t0 = X[creg2reg(xd)];
XReg t1 = X[creg2reg(xs2)];
X[creg2reg(xd)] = t0 - t1;
```

B.58.6. Sail Operation

```
{
  let rs1_val = X(rd+8);
  let rs2_val = X(rs2+8);
  let result : xlenbits = match op {
    RISCV_ADD => rs1_val + rs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(rs1_val <_s rs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(rs1_val <_u rs2_val)),
    RISCV_AND => rs1_val & rs2_val,
    RISCV_OR  => rs1_val | rs2_val,
    RISCV_XOR => rs1_val ^ rs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then rs1_val << (rs2_val[4..0])
                  else rs1_val << (rs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then rs1_val >> (rs2_val[4..0])
                  else rs1_val >> (rs2_val[5..0]),
    RISCV_SUB => rs1_val - rs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(rs1_val, rs2_val[4..0])
                  else shift_right_arith64(rs1_val, rs2_val[5..0])
  };
  X(rd+8) = result;
  RETIRE_SUCCESS
}
```

B.58.7. Exceptions

This instruction does not generate synchronous exceptions.

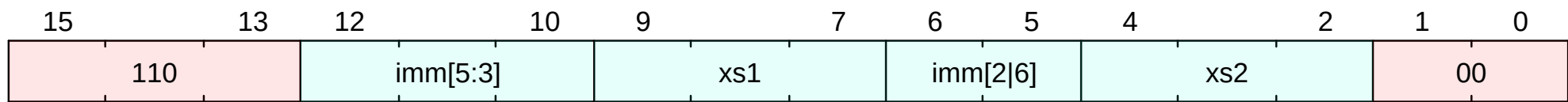
B.59. c.sw

Store word

This instruction is defined by:

Zca

B.59.1. Encoding



B.59.2. Description

Stores a 32-bit value in register xs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 4, to the base address in register xs1. It expands to `sw rs2, offset(xs1)`.

B.59.3. Access

M	S	U
Always	Always	Always

B.59.4. Decode Variables

```
Bits<7> imm = {$encoding[5], $encoding[12:10], $encoding[6], 2'd0};
Bits<3> xs2 = $encoding[4:2];
Bits<3> xs1 = $encoding[9:7];
```

B.59.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[creg2reg(xs1)] + imm;
write_memory<32>(virtual_address, X[creg2reg(xs2)][31:0], $encoding);
```

B.59.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

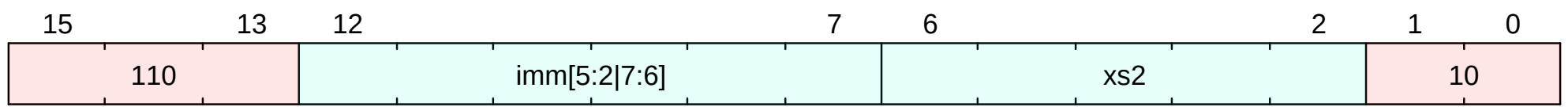
B.60. c.swsp

Store word to stack

This instruction is defined by:

Zca

B.60.1. Encoding



B.60.2. Description

Stores a 32-bit value in register xs2 to memory. It computes an effective address by adding the zero-extended offset, scaled by 4, to the stack pointer, x2. It expands to `sw xs2, offset(x2)`.

B.60.3. Access

M	S	U
Always	Always	Always

B.60.4. Decode Variables

```
Bits<8> imm = {$encoding[8:7], $encoding[12:9], 2'd0};
Bits<5> xs2 = $encoding[6:2];
```

B.60.5. IDL Operation

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg virtual_address = X[2] + imm;
write_memory<32>(virtual_address, X[xs2][31:0], $encoding);
```

B.60.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

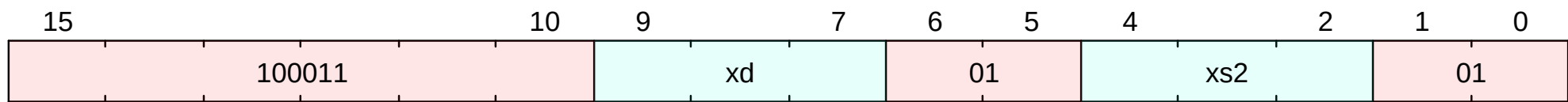
B.61. c.xor

Exclusive Or

This instruction is defined by:

Zca

B.61.1. Encoding



B.61.2. Description

Exclusive or xd with xs2, and store the result in xd The xd and xs2 register indexes should be used as xd+8 and xs2+8 (registers x8-x15). C.XOR expands into `xor xd, xd, xs2`.

B.61.3. Access

M	S	U
Always	Always	Always

B.61.4. Decode Variables

```
Bits<3> xs2 = $encoding[4:2];
Bits<3> xd = $encoding[9:7];
```

B.61.5. IDL Operation

```
XReg t0 = X[creg2reg(xd)];
XReg t1 = X[creg2reg(xs2)];
X[creg2reg(xd)] = t0 ^ t1;
```

B.61.6. Sail Operation

```
{
  let rs1_val = X(rd+8);
  let rs2_val = X(rs2+8);
  let result : xlenbits = match op {
    RISCV_ADD => rs1_val + rs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(rs1_val <_s rs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(rs1_val <_u rs2_val)),
    RISCV_AND => rs1_val & rs2_val,
    RISCV_OR  => rs1_val | rs2_val,
    RISCV_XOR => rs1_val ^ rs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then rs1_val << (rs2_val[4..0])
                  else rs1_val << (rs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then rs1_val >> (rs2_val[4..0])
                  else rs1_val >> (rs2_val[5..0]),
    RISCV_SUB => rs1_val - rs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(rs1_val, rs2_val[4..0])
                  else shift_right_arith64(rs1_val, rs2_val[5..0])
  };
  X(rd+8) = result;
  RETIRE_SUCCESS
}
```

B.61.7. Exceptions

This instruction does not generate synchronous exceptions.

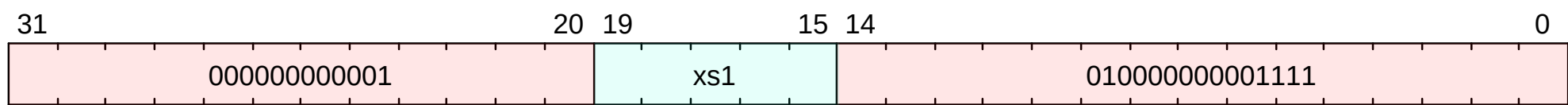
B.62. cbo.clean

Cache Block Clean

This instruction is defined by:

Zicbom

B.62.1. Encoding



B.62.2. Description

Cleans an entire cache block globally throughout the system.

Exactly what happens is coherence protocol-dependent, but in general it is expected that after this operation():

- The cache block will be in the clean (not dirty) state in any coherent cache holding a valid copy of the line.
- The data will be cleaned to a point such that an incoherent load can observe the cleaned data.

cbo.clean is ordered by FENCE instructions but not FENCE.I or SFENCE.VMA.

<%- if CACHE_BLOCK_SIZE.bit_length > [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Both PMP and PMA access control must be the same for all bytes in the block; otherwise, cbo.clean has UNSPECIFIED behavior. <%- end -%>

Clean operations are treated as stores for page and access permissions. If permission checks fail, one of the following exceptions will occur:

<%- if ext?(:H) -%>
* `Store/AMO Guest-Page Fault` if virtual memory translation fails during G-stage translation.
<%- end -%>
* `Store/AMO Page Fault` if virtual memory translation fails <% if ext?(:H) %>when V=0 or during VS-stage translation<% end %>
* `Store/AMO Access Fault` if a PMP or PMA access check fails

<%- if CACHE_BLOCK_SIZE.bit_length ≤ [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Because cache blocks are naturally aligned and always fit in a single PMP or PMA regions, the PMP and PMA access checks only need to check a single address in the line. <%- end -%>

CBO operations never raise a misaligned address fault.

B.62.3. Access

M	S	U
Always	Sometimes	Sometimes

Access is controlled through menvcfg.CBZE, senvcfg.CBZE, and henvcfg.CBZE. When access is denied, the instruction either raises an Illegal Instruction or Virtual Instruction exception according to the table below.

menvcfg.CBCFE	senvcfg.CBCFE	henvcfg.CBCFE	cbo.clean Instruction Behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	Illegal Instruction	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	0	0	executes	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	1	0	executes	executes	Virtual Instruction	Virtual Instruction
1	0	1	executes	Illegal Instruction	executes	Virtual Instruction
1	1	1	executes	executes	executes	executes

B.62.4. Decode Variables

Bits<5> xs1 = \$encoding[19:15];

B.62.5. Exceptions

This instruction does not generate synchronous exceptions.

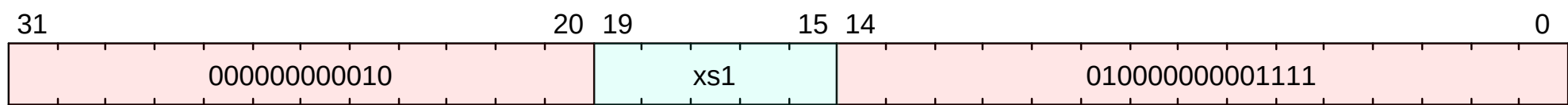
B.63. cbo.flush

Cache Block Flush

This instruction is defined by:

Zicbom

B.63.1. Encoding



B.63.2. Description

Flushes an entire cache block by cleaning it and then invalidating it in all caches.

`cbo.flush` is ordered by `FENCE` instructions but not `FENCE.I` or `SFENCE.VMA`.

<%- if CACHE_BLOCK_SIZE.bit_length > [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Both PMP and PMA access control must be the same for all bytes in the block; otherwise, `cbo.flush` has UNSPECIFIED behavior. <%- end -%>

Flush operations are treated as stores for page and access permissions. If permission checks fail, one of the following exceptions will occur:

<%- if ext?(:H) -%>
* `Store/AMO Guest-Page Fault` if virtual memory translation fails during G-stage translation.
<%- end -%>
* `Store/AMO Page Fault` if virtual memory translation fails <% if ext?(:H) %>when V=0 or during VS-stage translation<% end %>
* `Store/AMO Access Fault` if a PMP or PMA access check fails.

<%- if CACHE_BLOCK_SIZE.bit_length ≤ [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Because cache blocks are naturally aligned and always fit in a single PMP or PMA regions, the PMP and PMA access checks only need to check a single address in the line. <%- end -%>

CBO operations never raise a misaligned address fault.

B.63.3. Access

M	S	U
Always	Sometimes	Sometimes

Access is controlled through `menvcfg.CBZE`, `senvcfg.CBZE`, and `henvcfg.CBZE`. When access is denied, the instruction either raises an `Illegal Instruction` or `Virtual Instruction` exception according to the table below.

menvcfg.CBCFE	senvcfg.CBCFE	henvcfg.CBCFE	cbo.flush Instruction Behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	Illegal Instruction	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	0	0	executes	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	1	0	executes	executes	Virtual Instruction	Virtual Instruction
1	0	1	executes	Illegal Instruction	executes	Virtual Instruction
1	1	1	executes	executes	executes	executes

B.63.4. Decode Variables

Bits<5> xs1 = \$encoding[19:15];

B.63.5. Exceptions

This instruction does not generate synchronous exceptions.

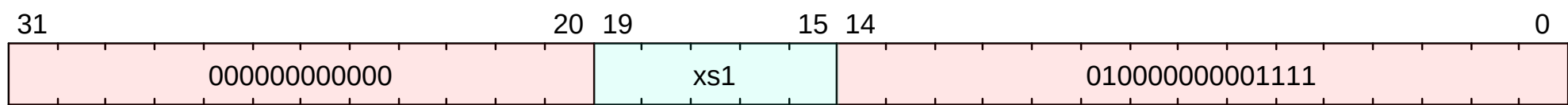
B.64. cbo.inval

Cache Block Invalidate

This instruction is defined by:

Zicbom

B.64.1. Encoding



B.64.2. Description

Either invalidates or flushes (clean + invalidate) a cache block, depending on the current mode and value of [menvcfg.CBIE](#), [senvcfg.CBIE](#), and/or [henvcfg.CBIE](#).

The instruction is an invalidate (without a clean) when:

- In M-mode
- In (H)S-mode and [menvcfg.CBIE](#) == 11
- In U-mode and [menvcfg.CBIE](#) == 11 and [senvcfg.CBIE](#) == 11
- In VS-mode and [menvcfg.CBIE](#) == 11 and [henvcfg.CBIE](#) == 11
- In VU-mode and [menvcfg.CBIE](#) == 11 and [henvcfg.CBIE](#) == 11 and [senvcfg.CBIE](#) == 11

Otherwise, if the instruction does not trap (see Access section), the operation is a flush. The table below summarizes the options.

menvcfg.CBIE	senvcfg.CBIE	henvcfg.CBIE	cbe.inval Operation				
			M-mode	S-mode	U-mode	VS-mode	VU-mode
00	-	-	Invalidate	Illegal Instruction	Illegal Instruction	Illegal Instruction	Illegal Instruction
01	00	00	Invalidate	Flush	Illegal Instruction	Virtual Instruction	Virtual Instruction
01	00	01	Invalidate	Flush	Illegal Instruction	Flush	Virtual Instruction
01	00	11	Invalidate	Flush	Illegal Instruction	Flush	Virtual Instruction
01	01	00	Invalidate	Flush	Flush	Virtual Instruction	Virtual Instruction
01	01	01	Invalidate	Flush	Flush	Flush	Flush
01	01	11	Invalidate	Flush	Flush	Flush	Flush
01	11	00	Invalidate	Flush	Flush	Virtual Instruction	Virtual Instruction
01	11	01	Invalidate	Flush	Flush	Flush	Flush
01	11	11	Invalidate	Flush	Flush	Flush	Flush
11	00	00	Invalidate	Invalidate	Illegal Instruction	Virtual Instruction	Virtual Instruction
11	00	01	Invalidate	Invalidate	Illegal Instruction	Flush	Virtual Instruction
11	00	11	Invalidate	Invalidate	Illegal Instruction	Invalidate	Virtual Instruction
11	01	00	Invalidate	Invalidate	Flush	Virtual Instruction	Virtual Instruction
11	01	01	Invalidate	Invalidate	Flush	Flush	Flush
11	01	11	Invalidate	Invalidate	Flush	Invalidate	Flush
11	11	00	Invalidate	Invalidate	Invalidate	Virtual Instruction	Virtual Instruction
11	11	01	Invalidate	Invalidate	Invalidate	Flush	Flush
11	11	11	Invalidate	Invalidate	Invalidate	Invalidate	Invalidate

[cbo.inval](#) is ordered by [FENCE](#) instructions but not [FENCE.I](#) or [SFENCE.VMA](#).

<%- if CACHE_BLOCK_SIZE.bit_length > [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Both PMP and PMA access control must be the same for all bytes in the block; otherwise, [cbo.zero](#) has UNSPECIFIED behavior. <%- end -%>

Invalidate operations are treated as stores for page and access permissions. If permission checks fail, one of the following exceptions will occur:

<%- if ext?(:H) -%>
* `Store/AMO Guest-Page Fault` if virtual memory translation fails during G-stage translation.
<%- end -%>
* `Store/AMO Page Fault` if virtual memory translation fails <% if ext?(:H) %>when V=0 or during VS-stage translation<% end %>

* `Store/AMO Access Fault` if a PMP or PMA access check fails.

<%- if CACHE_BLOCK_SIZE.bit_length <= [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Because cache blocks are naturally aligned and always fit in a single PMP or PMA regions, the PMP and PMA access checks only need to check a single address in the line. <%- end -%>

CBO operations never raise a misaligned address fault.

B.64.3. Access

M	S	U
Always	Sometimes	Sometimes

Access is controlled through [menvcfg.CBIE](#), [senvcfg.CBIE](#), and [henvcfg.CBIE](#). When access is denied, the instruction either raises an **Illegal Instruction** or **Virtual Instruction** exception according to the table below.



`xenvcfg.CBIE == 10` is reserved, and cannot be written by software. As such, that pattern is excluded from the table below.

menvcfg.CBIE	senvcfg.CBIE	henvcfg.CBIE	cbo.inval Instruction Behavior			
			S-mode	U-mode	VS-mode	VU-mode
00	-	-	Illegal Instruction	Illegal Instruction	Illegal Instruction	Illegal Instruction
01/11	00	00	executes	Illegal Instruction	Virtual Instruction	Virtual Instruction
01/11	01/11	00	executes	executes	Virtual Instruction	Virtual Instruction
01/11	00	01/11	executes	Illegal Instruction	executes	Virtual Instruction
01/11	01/11	01/11	executes	executes	executes	executes

B.64.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
```

B.64.5. Exceptions

This instruction does not generate synchronous exceptions.

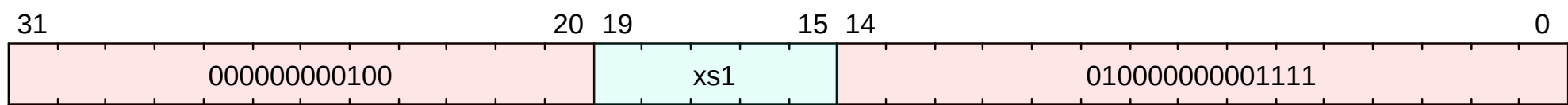
B.65. cbo.zero

Cache Block Zero

This instruction is defined by:

Zicboz

B.65.1. Encoding



B.65.2. Description

Zeros an entire cache block

The block zeroing does not need to be atomic.

cbo.zero is ordered by FENCE instructions but not FENCE.I or SFENCE.VMA.

<%- if CACHE_BLOCK_SIZE.bit_length > [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Both PMP and PMA access control must be the same for all bytes in the block; otherwise, cbo.zero has UNSPECIFIED behavior. <%- end -%>

Clean operations are treated as stores for page and access permissions. If permission checks fail, one of the following exceptions will occur:

<%- if ext?(:H) -%>
* `Store/AMO Guest-Page Fault` if virtual memory translation fails during G-stage translation.
<%- end -%>
* `Store/AMO Page Fault` if virtual memory translation fails <% if ext?(:H) %>when V=0 or during VS-stage translation<% end %>
* `Store/AMO Access Fault` if a PMP or PMA access check fails.

<%- if CACHE_BLOCK_SIZE.bit_length ≤ [PMP_GRANULARITY, PMA_GRANULARITY].min -%> Because cache blocks are naturally aligned and always fit in a single PMP or PMA regions, the PMP and PMA access checks only need to check a single address in the line. <%- end -%>

CBO operations never raise a misaligned address fault.

B.65.3. Access

M	S	U
Always	Sometimes	Sometimes

Access is controlled through menvcfg.CBZE, senvcfg.CBZE, and henvcfg.CBZE. When access is denied, the instruction either raises an Illegal Instruction or Virtual Instruction exception according to the table below.

menvcfg.CBZE	senvcfg.CBZE	henvcfg.CBZE	cbo.zero Instruction Behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	Illegal Instruction	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	0	0	executes	Illegal Instruction	Virtual Instruction	Virtual Instruction
1	1	0	executes	executes	Virtual Instruction	Virtual Instruction
1	0	1	executes	Illegal Instruction	executes	Virtual Instruction
1	1	1	executes	executes	executes	executes

B.65.4. Decode Variables

Bits<5> xs1 = \$encoding[19:15];

B.65.5. IDL Operation

if ((mode() == PrivilegeMode::M && CSR[menvcfg].CBZE == 0) || (mode() == PrivilegeMode::U && CSR[senvcfg].CBZE == 0)) {
 raise(ExceptionCode::IllegalInstruction, mode(), \$encoding);
} else if ((mode() == PrivilegeMode::VS && CSR[henvcfg].CBZE == 0) || (mode() == PrivilegeMode::VU && (CSR[henvcfg].CBZE | CSR[senvcfg].CBZE) == 0)) {
 raise(ExceptionCode::VirtualInstruction, mode(), \$encoding);
} else {

```
XReg mask = CACHE_BLOCK_SIZE - 1;
XReg cache_block_vaddr = X[xs1] & ~mask;
TranslationResult result;
result = translate(cache_block_vaddr, MemoryOperation::Write, effective_ldst_mode(), $encoding);
access_check(result.paddr, CACHE_BLOCK_SIZE * 8, cache_block_vaddr, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
cache_block_zero(result.paddr);
}
```

B.65.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoPageFault
- VirtualInstruction

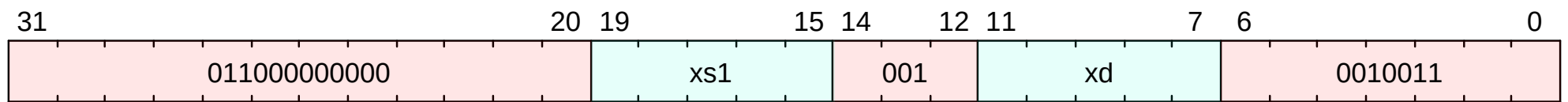
B.66. clz

Count leading zero bits

This instruction is defined by:

Zbb

B.66.1. Encoding



B.66.2. Description

Counts the number of 0’s before the first 1, starting at the most-significant bit (i.e., XLEN-1) and progressing to bit 0. Accordingly, if the input is 0, the output is XLEN, and if the most-significant bit of the input is a 1, the output is 0.

B.66.3. Access

M	S	U
Always	Always	Always

B.66.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.66.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = (xlen() - 1) - $signed(highest_set_bit(X[xs1]));
```

B.66.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    result : nat = 0;
    done : bool = false;
    foreach (i from (sizeof(xlen) - 1) downto 0)
        if not(done) then if rs1_val[i] == bitzero
            then result = result + 1
            else done = true;
    X(rd) = to_bits(sizeof(xlen), result);
    RETIRE_SUCCESS
}
```

B.66.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

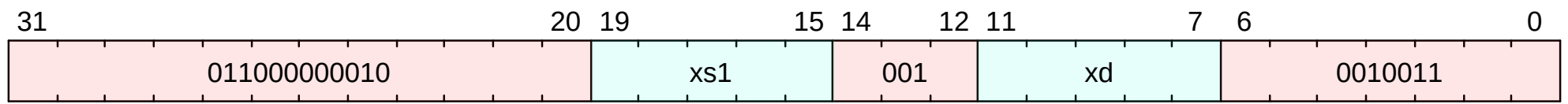
B.67. cpop

Count set bits

This instruction is defined by:

Zbb

B.67.1. Encoding



B.67.2. Description

Counts the number of 1’s (i.e., set bits) in the source register.

Listing 1. Software Hint

This operations is known as population count, popcount, sideways sum, bit summation, or Hamming weight.

The GCC builtin function `__builtin_popcount (unsigned int x)` is implemented by cpop on RV32 and by cpopw on RV64. The GCC builtin function `__builtin_popcountl (unsigned long x)` for LP64 is implemented by cpop on RV64.

B.67.3. Access

M	S	U
Always	Always	Always

B.67.4. Decode Variables

Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

B.67.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {  
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
}  
XReg bitcount = 0;  
XReg xs1_val = X[xs1];  
for (U32 i = 0; i < xlen(); i++) {  
    if (xs1_val[i] == 1'b1) {  
        bitcount = bitcount + 1;  
    }  
}  
X[xd] = bitcount;
```

B.67.6. Sail Operation

```
{  
    let rs1_val = X(rs1);  
    result : nat = 0;  
    foreach (i from 0 to (xlen_val - 1))  
        if rs1_val[i] == bitone then result = result + 1;  
    X(rd) = to_bits(sizeof(xlen), result);  
    RETIRE_SUCCESS  
}
```

B.67.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

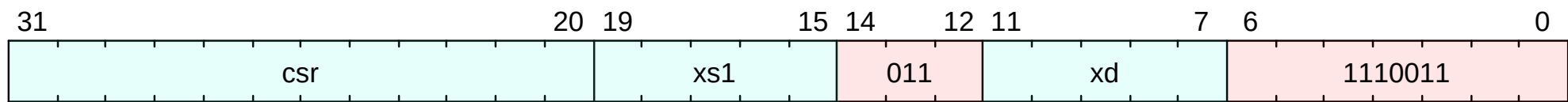
B.68. csrrc

Atomic Read and Clear Bits in CSR

This instruction is defined by:

[Zicsr](#)

B.68.1. Encoding



B.68.2. Description

The CSRRC (Atomic Read and Clear Bits in CSR) instruction reads the value of the CSR, zero-extends the value to XLEN bits, and writes it to integer register **xd**. The initial value in integer register **xs1** is treated as a bit mask that specifies bit positions to be cleared in the CSR. Any bit that is high in **xs1** will cause the corresponding bit to be cleared in the CSR, if that CSR bit is writable.

For CSRRC, if **xs1**=**x0**, then the instruction will not write to the CSR at all, and so shall not cause any of the side effects that might otherwise occur on a CSR write, nor raise illegal- instruction exceptions on accesses to read-only CSRs. CSRRC always reads the addressed CSR and cause any read side effects regardless of **xs1** and **xd** fields. Note that if **xs1** specifies a register other than **x0**, and that register holds a zero value, the instruction will not action any attendant per-field side effects, but will action any side effects caused by writing to the entire CSR.

B.68.3. Access

M	S	U
Always	Always	Always

B.68.4. Decode Variables

```
Bits<12> csr = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.68.5. IDL Operation

```
Csr csr_handle = direct_csr_lookup(csr);
Boolean will_write = xs1 != 0;
if (csr_handle.valid == false) {
    unimplemented_csr($encoding);
} else if (!compatible_mode?(csr_handle.mode, mode())) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
} else if (will_write && csr_handle.writable == false) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg initial_csr_value = csr_sw_read(csr_handle);
if (xs1 != 0) {
    XReg mask = X[xs1];
    csr_sw_write(csr_handle, initial_csr_value & ~mask);
}
X[xd] = initial_csr_value;
```

B.68.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

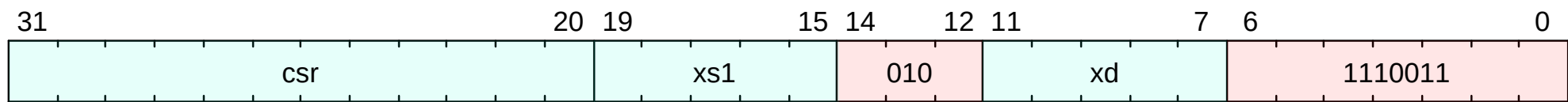
B.70. csrrs

Atomic Read and Set Bits in CSR

This instruction is defined by:

[Zicsr](#)

B.70.1. Encoding



B.70.2. Description

Atomically read and set bits in a CSR.

Reads the value of the CSR, zero-extends the value to **XLEN** bits, and writes it to integer register **xd**. The initial value in integer register **xs1** is treated as a bit mask that specifies bit positions to be set in the CSR. Any bit that is high in **xs1** will cause the corresponding bit to be set in the CSR, if that CSR bit is writable. Other bits in the CSR are not explicitly written.

B.70.3. Access

M	S	U
Always	Always	Always

B.70.4. Decode Variables

```
Bits<12> csr = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.70.5. IDL Operation

```
Boolean will_write = xs1 != 0;
Csr csr_handle = direct_csr_lookup(csr);
if (csr_handle.valid == false) {
    unimplemented_csr($encoding);
} else if (!compatible_mode?(csr_handle.mode, mode())) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
} else if (will_write && csr_handle.writable == false) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg initial_csr_value = csr_sw_read(csr_handle);
if (will_write) {
    XReg mask = X[xs1];
    csr_sw_write(csr_handle, initial_csr_value | mask);
}
X[xd] = initial_csr_value;
```

B.70.6. Sail Operation

```
{
  let rs1_val : xlenbits = if is_imm then zero_extend(rs1) else X(rs1);
  let isWrite : bool = match op {
    CSRRW => true,
    _      => if is_imm then unsigned(rs1_val) != 0 else unsigned(rs1) != 0
  };
  if not(check_CSR(csr, cur_privilege, isWrite))
  then { handle_illegal(); RETIRE_FAIL }
  else if not(ext_check_CSR(csr, cur_privilege, isWrite))
  then { ext_check_CSR_fail(); RETIRE_FAIL }
  else {
    let csr_val = readCSR(csr); /* could have side-effects, so technically shouldn't perform for CSRW[I] with rd == 0 */
    if isWrite then {
      let new_val : xlenbits = match op {
        CSRRW => rs1_val,
        CSRRS => csr_val | rs1_val,
```

```
        CSRRC => csr_val & ~(rs1_val)
    };
    writeCSR(csr, new_val)
};
X(rd) = csr_val;
RETIRE_SUCCESS
}
}
```

B.70.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

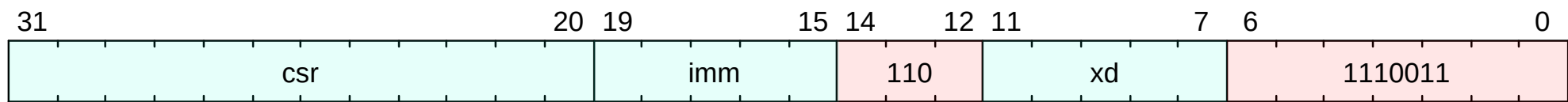
B.71. csrrsi

Atomic Read and Set Bits in CSR with Immediate

This instruction is defined by:

[Zicsr](#)

B.71.1. Encoding



B.71.2. Description

The CSRRSI variant is similar to CSRRS, except this updates the CSR using an XLEN-bit value obtained by zero-extending a 5-bit unsigned immediate (imm[4:0]) field encoded in the **xs1** field instead of a value from an integer register. For CSRRSI, if the **imm[4:0]** field is zero, then this instruction will not write to the CSR, and shall not cause any of the side effects that might otherwise occur on a CSR write, nor raise illegal-instruction exceptions on accesses to read-only CSRs. The CSRRSI will always read the CSR and cause any read side effects regardless of **xd** and **xs1** fields.

B.71.3. Access

M	S	U
Always	Always	Always

B.71.4. Decode Variables

```
Bits<12> csr = $encoding[31:20];
Bits<5> imm = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.71.5. IDL Operation

```
Boolean will_write = imm != 0;
Csr csr_handle = direct_csr_lookup(csr);
if (csr_handle.valid == false) {
    unimplemented_csr($encoding);
} else if (!compatible_mode?(csr_handle.mode, mode())) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
} else if (will_write && csr_handle.writable == false) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg initial_csr_value = csr_sw_read(csr_handle);
if (will_write) {
    XReg mask = imm;
    csr_sw_write(csr_handle, initial_csr_value | mask);
}
X[xd] = initial_csr_value;
```

B.71.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

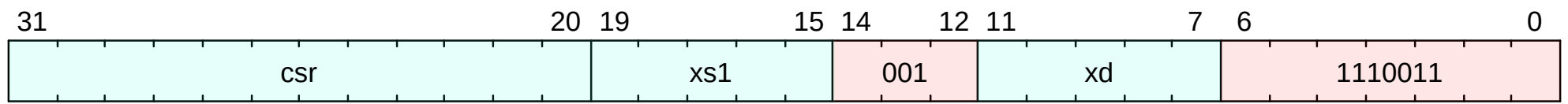
B.72. csrrw

Atomic Read/Write CSR

This instruction is defined by:

Zicsr

B.72.1. Encoding



B.72.2. Description

Atomically swap values in the CSRs and integer registers.

Read the old value of the CSR, zero-extends the value to **XLEN** bits, and then write it to integer register xd. The initial value in xs1 is written to the CSR. If **xd=x0**, then the instruction shall not read the CSR and shall not cause any of the side effects that might occur on a CSR read.

B.72.3. Access

M	S	U
Always	Always	Always

B.72.4. Decode Variables

```
Bits<12> csr = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.72.5. IDL Operation

```
Csr csr_handle = direct_csr_lookup(csr);
Bits<MXLEN> initial_value = X[xs1];
if (csr_handle.valid == false) {
    unimplemented_csr($encoding);
} else if (!compatible_mode?(csr_handle.mode, mode())) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
} else if (csr_handle.writable == false) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (xd != 0) {
    X[xd] = csr_sw_read(csr_handle);
}
csr_sw_write(csr_handle, initial_value);
```

B.72.6. Sail Operation

```
{
  let rs1_val : xlenbits = if is_imm then zero_extend(rs1) else X(rs1);
  let isWrite : bool = match op {
    CSRRW => true,
    _      => if is_imm then unsigned(rs1_val) != 0 else unsigned(rs1) != 0
  };
  if not(check_CSR(csr, cur_privilege, isWrite))
  then { handle_illegal(); RETIRE_FAIL }
  else if not(ext_check_CSR(csr, cur_privilege, isWrite))
  then { ext_check_CSR_fail(); RETIRE_FAIL }
  else {
    let csr_val = readCSR(csr); /* could have side-effects, so technically shouldn't perform for CSRW[I] with rd == 0 */
    if isWrite then {
      let new_val : xlenbits = match op {
        CSRRW => rs1_val,
        CSRRS => csr_val | rs1_val,
        CSRRC => csr_val & ~(rs1_val)
      };
      writeCSR(csr, new_val)
    }
  }
```

```
};  
X(rd) = csr_val;  
RETIRE_SUCCESS  
}  
}
```

B.72.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

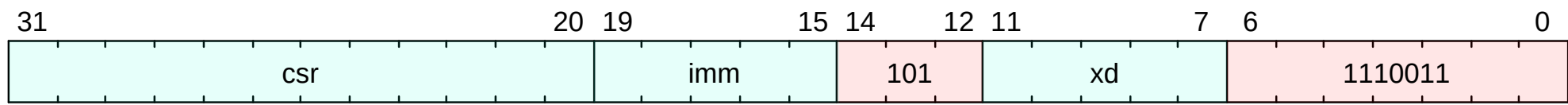
B.73. csrrwi

Atomic Read/Write CSR Immediate

This instruction is defined by:

[Zicsr](#)

B.73.1. Encoding



B.73.2. Description

Atomically write CSR using a 5-bit immediate, and load the previous value into 'xd'.

Read the old value of the CSR, zero-extends the value to **XLEN** bits, and then write it to integer register xd. The 5-bit uimm field is zero-extended and written to the CSR. If **xd=x0**, then the instruction shall not read the CSR and shall not cause any of the side effects that might occur on a CSR read.

B.73.3. Access

M	S	U
Always	Always	Always

B.73.4. Decode Variables

```
Bits<12> csr = $encoding[31:20];
Bits<5> imm = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.73.5. IDL Operation

```
Csr csr_handle = direct_csr_lookup(csr);
if (csr_handle.valid == false) {
    unimplemented_csr($encoding);
} else if (!compatible_mode?(csr_handle.mode, mode())) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
} else if (csr_handle.writable == false) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (xd != 0) {
    X[xd] = csr_sw_read(csr_handle);
}
csr_sw_write(csr_handle, {{MXLEN - 5{1'b0}}}, imm);
```

B.73.6. Sail Operation

```
{
  let rs1_val : xlenbits = if is_imm then zero_extend(rs1) else X(rs1);
  let isWrite : bool = match op {
    CSRRW => true,
    _      => if is_imm then unsigned(rs1_val) != 0 else unsigned(rs1) != 0
  };
  if not(check_CSR(csr, cur_privilege, isWrite))
  then { handle_illegal(); RETIRE_FAIL }
  else if not(ext_check_CSR(csr, cur_privilege, isWrite))
  then { ext_check_CSR_fail(); RETIRE_FAIL }
  else {
    let csr_val = readCSR(csr); /* could have side-effects, so technically shouldn't perform for CSRW[I] with rd == 0 */
    if isWrite then {
      let new_val : xlenbits = match op {
        CSRRW => rs1_val,
        CSRRS => csr_val | rs1_val,
        CSRRC => csr_val & ~(rs1_val)
      };
      writeCSR(csr, new_val)
    }
  }
};
```

```
    X(rd) = csr_val;  
    RETIRE_SUCCESS  
}  
}
```

B.73.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

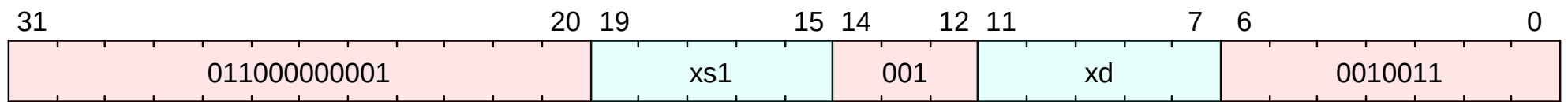
B.74. ctz

Count trailing zero bits

This instruction is defined by:

Zbb

B.74.1. Encoding



B.74.2. Description

Counts the number of 0’s before the first 1, starting at the least-significant bit (i.e., 0) and progressing to the most-significant bit (i.e., XLEN-1). Accordingly, if the input is 0, the output is XLEN, and if the least-significant bit of the input is a 1, the output is 0.

B.74.3. Access

M	S	U
Always	Always	Always

B.74.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.74.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (xlen() == 32) {
    X[xd] = lowest_set_bit(X[xs1][31:0]);
} else {
    X[xd] = lowest_set_bit(X[xs1]);
}
```

B.74.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    result : nat = 0;
    done : bool = false;
    foreach (i from 0 to (sizeof(xlen) - 1))
        if not(done) then if rs1_val[i] == bitzero
            then result = result + 1
            else done = true;
    X(rd) = to_bits(sizeof(xlen), result);
    RETIRE_SUCCESS
}
```

B.74.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

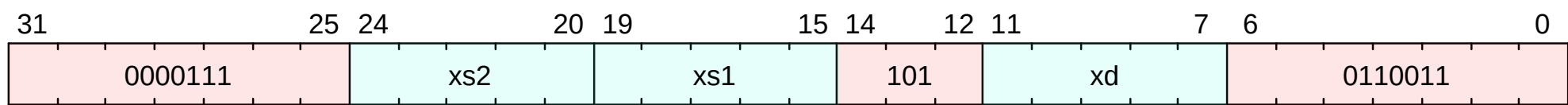
B.75. czero.eqz

Conditional zero, if condition is equal to zero

This instruction is defined by:

Zicond

B.75.1. Encoding



B.75.2. Description

If xs2 contains the value zero, this instruction writes the value zero to xd. Otherwise, this instruction copies the contents of xs1 to xd. This instruction carries a syntactic dependency from both xs1 and xs2 to xd. Furthermore, if the Zkt extension is implemented, this instruction’s timing is independent of the data values in xs1 and xs2.

B.75.3. Access

M	S	U
Always	Always	Always

B.75.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.75.5. IDL Operation

```
X[xd] = (X[xs2] == 0) ? 0 : X[xs1];
```

B.75.6. Sail Operation

```
{
  let value = X(rs1);
  let condition = X(rs2);
  let result : xlenbits = if (condition == zeros()) then zeros()
                          else value;

  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.75.7. Exceptions

This instruction does not generate synchronous exceptions.

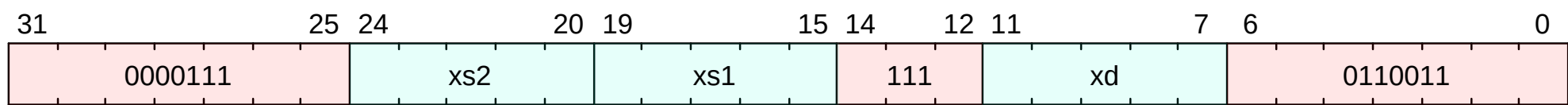
B.76. czero.nez

Conditional zero, if condition is nonzero

This instruction is defined by:

Zicond

B.76.1. Encoding



B.76.2. Description

If xs2 contains a nonzero value, this instruction writes the value zero to xd. Otherwise, this instruction copies the contents of xs1 to xd. This instruction carries a syntactic dependency from both xs1 and xs2 to xd. Furthermore, if the Zkt extension is implemented, this instruction’s timing is independent of the data values in xs1 and xs2.

B.76.3. Access

M	S	U
Always	Always	Always

B.76.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.76.5. IDL Operation

```
X[xd] = (X[xs2] != 0) ? 0 : X[xs1];
```

B.76.6. Sail Operation

```
{
  let value = X(rs1);
  let condition = X(rs2);
  let result : xlenbits = if (condition != zeros()) then zeros()
                           else value;

  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.76.7. Exceptions

This instruction does not generate synchronous exceptions.

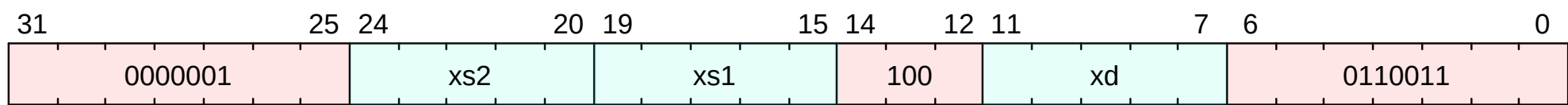
B.77. div

Signed division

This instruction is defined by:

M

B.77.1. Encoding



B.77.2. Description

Divide xs1 by xs2, and store the result in xd. The remainder is discarded.

Division by zero will put -1 into xd.

Division resulting in signed overflow (when most negative number is divided by -1) will put the most negative number into xd;

B.77.3. Access

M	S	U
Always	Always	Always

B.77.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.77.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg src1 = X[xs1];
XReg src2 = X[xs2];
XReg signed_min = (xlen() == 32) ? $signed({1'b1, {31{1'b0}}}) : {1'b1, {63{1'b0}}};
if (src2 == 0) {
    X[xd] = {MXLEN{1'b1}};
} else if ((src1 == signed_min) && (src2 == {MXLEN{1'b1}})) {
    X[xd] = signed_min;
} else {
    X[xd] = $signed(src1) / $signed(src2);
}
```

B.77.6. Sail Operation

```
{
  if extension("M") then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if s then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if s then signed(rs2_val) else unsigned(rs2_val);
    let q : int = if rs2_int == 0 then -1 else quot_round_zero(rs1_int, rs2_int);
    /* check for signed overflow */
    let q': int = if s & q > xlen_max_signed then xlen_min_signed else q;
    X(rd) = to_bits(sizeof(xlen), q');
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```

B.77.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

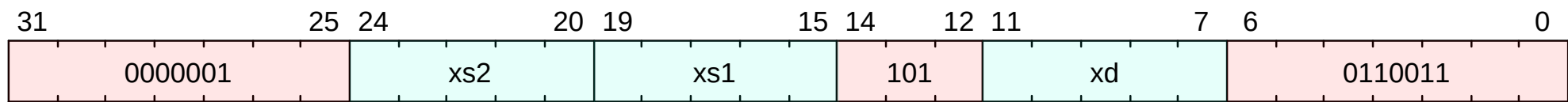
B.78. divu

Unsigned division

This instruction is defined by:

M

B.78.1. Encoding



B.78.2. Description

Divide unsigned values in xs1 by xs2, and store the result in xd.

The remainder is discarded.

If the value in xs2 is zero, xd gets the largest unsigned value.

B.78.3. Access

M	S	U
Always	Always	Always

B.78.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.78.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg src1 = X[xs1];
XReg src2 = X[xs2];
if (src2 == 0) {
  X[xd] = {MXLEN{1'b1}};
} else {
  X[xd] = src1 / src2;
}
```

B.78.6. Sail Operation

```
{
  if extension("M") then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if s then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if s then signed(rs2_val) else unsigned(rs2_val);
    let q : int = if rs2_int == 0 then -1 else quot_round_zero(rs1_int, rs2_int);
    /* check for signed overflow */
    let q': int = if s & q > xlen_max_signed then xlen_min_signed else q;
    X(rd) = to_bits(sizeof(xlen), q');
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```

B.78.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

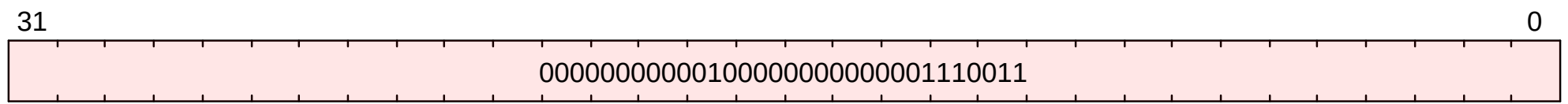
B.79. ebreak

Breakpoint exception

This instruction is defined by:

I

B.79.1. Encoding



B.79.2. Description

The EBREAK instruction is used by debuggers to cause control to be transferred back to a debugging environment. Unless overridden by an external debug environment, EBREAK raises a breakpoint exception and performs no other operation.



As described in the [C](#) Standaxd Extension for Compressed Instructions, the [c.ebreak](#) instruction performs the same operation as the EBREAK instruction.

EBREAK causes the receiving privilege mode’s epc register to be set to the address of the EBREAK instruction itself, not the address of the following instruction. As EBREAK causes a synchronous exception, it is not considered to retire, and should not increment the [minstret](#) CSR.

B.79.3. Access

M	S	U
Always	Always	Always

B.79.4. Decode Variables

B.79.5. IDL Operation

```
if (TRAP_ON_EBREAK) {
  raise_precise(ExceptionCode::Breakpoint, mode(), $pc);
} else {
  eei_ebreak();
}
```

B.79.6. Sail Operation

```
{
  handle_mem_exception(PC, E_Breakpoint());
  RETIRE_FAIL
}
```

B.79.7. Exceptions

This instruction may result in the following synchronous exceptions:

- Breakpoint

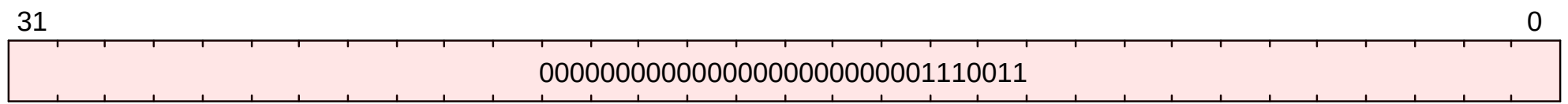
B.80. ecall

Environment call

This instruction is defined by:

I

B.80.1. Encoding



B.80.2. Description

Makes a request to the supporting execution environment. When executed in U-mode, S-mode, or M-mode, it generates an environment-call-from-U-mode exception, environment-call-from-S-mode exception, or environment-call-from-M-mode exception, respectively, and performs no other operation.



ECALL generates a different exception for each originating privilege mode so that environment call exceptions can be selectively delegated. A typical use case for Unix-like operating systems is to delegate to S-mode the environment-call-from-U-mode exception but not the others.

ECALL causes the receiving privilege mode’s epc register to be set to the address of the ECALL instruction itself, not the address of the following instruction. As ECALL causes a synchronous exception, it is not considered to retire, and should not increment the [minstret](#) CSR.

B.80.3. Access

M	S	U
Always	Always	Always

B.80.4. Decode Variables

B.80.5. IDL Operation

```
if (mode() == PrivilegeMode::M) {
  if (TRAP_ON_ECALL_FROM_M) {
    raise_precise(ExceptionCode::Mcall, PrivilegeMode::M, 0);
  } else {
    eei_ecall_from_m();
  }
} else if (mode() == PrivilegeMode::S) {
  if (TRAP_ON_ECALL_FROM_S) {
    raise_precise(ExceptionCode::Scall, PrivilegeMode::S, 0);
  } else {
    eei_ecall_from_s();
  }
} else if (mode() == PrivilegeMode::U || mode() == PrivilegeMode::VU) {
  if (TRAP_ON_ECALL_FROM_U) {
    raise_precise(ExceptionCode::Ucall, mode(), 0);
  } else {
    eei_ecall_from_u();
  }
} else if (mode() == PrivilegeMode::VS) {
  if (TRAP_ON_ECALL_FROM_VS) {
    raise_precise(ExceptionCode::VScall, PrivilegeMode::VS, 0);
  } else {
    eei_ecall_from_vs();
  }
}
```

B.80.6. Sail Operation

```
{
  let t : sync_exception =
    struct { trap = match (cur_privilege) {
```

```

        User      => E_U_EnvCall(),
        Supervisor => E_S_EnvCall(),
        Machine    => E_M_EnvCall()
    },
    excinfo = (None() : option(xlenbits)),
    ext     = None() };
set_next_pc(exception_handler(cur_privilege, CTL_TRAP(t), PC));
RETIRE_FAIL
}

```

B.80.7. Exceptions

This instruction may result in the following synchronous exceptions:

- Mcall
- Scall
- Ucall
- VScall

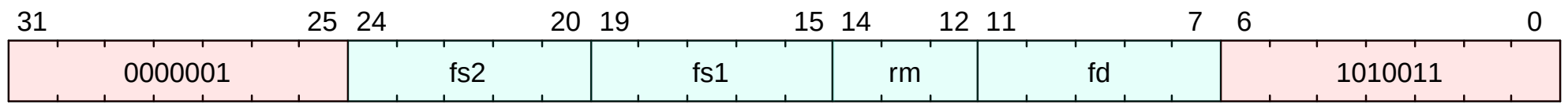
B.81. fadd.d

Floating-Point Add Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.81.1. Encoding



B.81.2. Description

The [fadd.d](#) instruction is analogous to [fadd.s](#) and performs double-precision floating-point addition of [fs1](#) and [fs2](#) and writes the final result to [fd](#).

B.81.3. Access

M	S	U
Always	Always	Always

B.81.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.81.5. IDL Operation

B.81.6. Exceptions

This instruction does not generate synchronous exceptions.

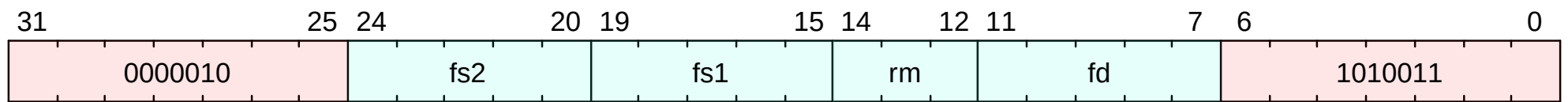
B.82. fadd.h

No synopsis available

This instruction is defined by:

(Zfh | | Zhinx)

B.82.1. Encoding



B.82.2. Description

No description available.

B.82.3. Access

M	S	U
Always	Always	Always

B.82.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.82.5. IDL Operation

B.82.6. Exceptions

This instruction does not generate synchronous exceptions.

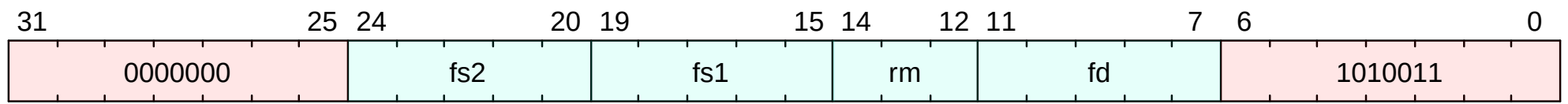
B.83. fadd.s

Floating-Point Add Single-Precision

This instruction is defined by:

F

B.83.1. Encoding



B.83.2. Description

The [fadd.s](#) instruction performs single-precision floating-point addition of **fs1** and **fs2** and writes the final result to **fd**.

B.83.3. Access

M	S	U
Always	Always	Always

B.83.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3>  rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.83.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode mode = rm_to_mode(rm, $encoding);
f[fd] = f32_add(f[fs1], f[fs2], mode);
```

B.83.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) = match op {
        FADD_S  => riscv_f32Add (rm_3b, rs1_val_32b, rs2_val_32b),
        FSUB_S  => riscv_f32Sub (rm_3b, rs1_val_32b, rs2_val_32b),
        FMUL_S  => riscv_f32Mul (rm_3b, rs1_val_32b, rs2_val_32b),
        FDIV_S  => riscv_f32Div (rm_3b, rs1_val_32b, rs2_val_32b)
      };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.83.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

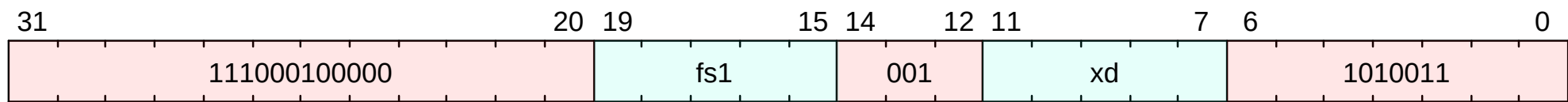
B.84. fclass.d

Floating-Point Classify Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.84.1. Encoding



B.84.2. Description

The `fclass.d` instruction is defined analogously to its single-precision counterpart, but operates on double-precision operands. It examines the value in floating-point register `fs1` and writes to integer register `xd` a 10-bit mask that indicates the class of the floating point number.

The format of the mask is described in the table below. The corresponding bit in `xd` will be set if the property is true and clear otherwise. All other bits in `xd` are cleared. Note that exactly one bit in `xd` will be set.

Table 13. Format of result of `fclass` instruction.

xd bit	Meaning
0	fs1 is $-\infty$.
1	fs1 is a negative normal number.
2	fs1 is a negative subnormal number.
3	fs1 is -0 .
4	fs1 is $+0$.
5	fs1 is a positive subnormal number.
6	fs1 is a positive normal number.
7	fs1 is $+\infty$.
8	fs1 is a signaling NaN.
9	fs1 is a quiet NaN.

B.84.3. Access

M	S	U
Always	Always	Always

B.84.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.84.5. IDL Operation

B.84.6. Exceptions

This instruction does not generate synchronous exceptions.

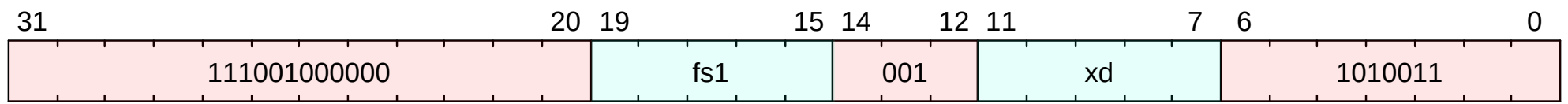
B.85. fclass.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.85.1. Encoding



B.85.2. Description

No description available.

B.85.3. Access

M	S	U
Always	Always	Always

B.85.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.85.5. IDL Operation

B.85.6. Exceptions

This instruction does not generate synchronous exceptions.

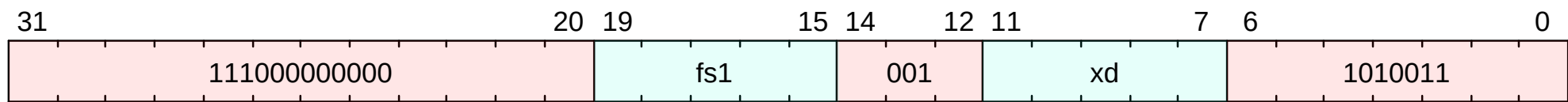
B.86. fclass.s

Floating-Point Classify Single-Precision

This instruction is defined by:

F

B.86.1. Encoding



B.86.2. Description

The `fclass.s` instruction examines the value in floating-point register `fs1` and writes to integer register `xd` a 10-bit mask that indicates the class of the floating-point number.

The format of the mask is described in the table below. The corresponding bit in `xd` will be set if the property is true and clear otherwise. All other bits in `xd` are cleared. Note that exactly one bit in `xd` will be set. `fclass.s` does not set the floating-point exception flags.

Table 14. Format of result of `fclass` instruction.

xd bit	Meaning
0	fs1 is <code>-∞</code> .
1	fs1 is a negative normal number.
2	fs1 is a negative subnormal number.
3	fs1 is <code>-0</code> .
4	fs1 is <code>+0</code> .
5	fs1 is a positive subnormal number.
6	fs1 is a positive normal number.
7	fs1 is <code>+∞</code> .
8	fs1 is a signaling NaN.
9	fs1 is a quiet NaN.

B.86.3. Access

M	S	U
Always	Always	Always

B.86.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.86.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = f[fs1][31:0];
if (is_sp_neg_inf?(sp_value)) {
    X[xd] = 1 << 0;
} else if (is_sp_neg_norm?(sp_value)) {
    X[xd] = 1 << 1;
} else if (is_sp_neg_subnorm?(sp_value)) {
    X[xd] = 1 << 2;
} else if (is_sp_neg_zero?(sp_value)) {
    X[xd] = 1 << 3;
} else if (is_sp_pos_zero?(sp_value)) {
    X[xd] = 1 << 4;
} else if (is_sp_pos_subnorm?(sp_value)) {
    X[xd] = 1 << 5;
} else if (is_sp_pos_norm?(sp_value)) {
    X[xd] = 1 << 6;
} else if (is_sp_pos_inf?(sp_value)) {
    X[xd] = 1 << 7;
```



```

} else if (is_sp_signaling_nan?(sp_value)) {
  X[xd] = 1 << 8;
} else {
  assert(is_sp_quiet_nan?(sp_value), "Unexpected SP value");
  X[xd] = 1 << 9;
}

```

B.86.6. Sail Operation

```

{
  let rs1_val_X      = X(rs1);
  let rd_val_S       = rs1_val_X [31..0];
  F(rd) = nan_box (rd_val_S);
  RETIRE_SUCCESS
}

```

B.86.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

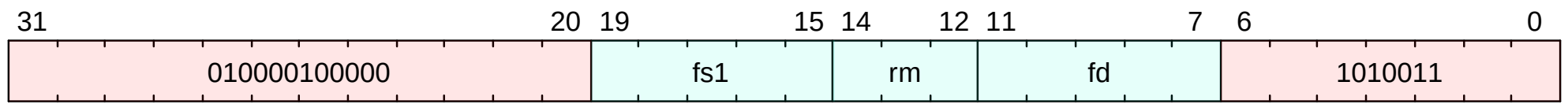
B.87. fcvt.d.s

Floating-Point Convert Single-Precision to Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.87.1. Encoding



B.87.2. Description

The single-precision to double-precision conversion instruction, [fcvt.d.s](#) is encoded in the OP-FP major opcode space and both the source and destination are floating-point registers. The [xs2](#) field encodes the datatype of the source, and the [fmt](#) field encodes the datatype of the destination. [fcvt.d.s](#) will never round.

B.87.3. Access

M	S	U
Always	Always	Always

B.87.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.87.5. IDL Operation

B.87.6. Exceptions

This instruction does not generate synchronous exceptions.

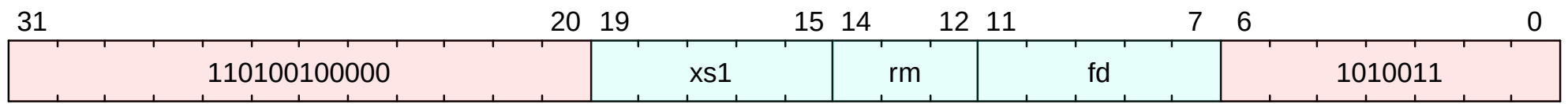
B.88. fcvt.d.w

Floating-Point Convert Word to Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.88.1. Encoding



B.88.2. Description

The `fcvt.d.w` instruction converts a 32-bit signed integer, in integer register `xs1` into a double-precision floating-point number in floating-point register `fd`. Note `fcvt.d.w` always produces an exact result and is unaffected by rounding mode.

B.88.3. Access

M	S	U
Always	Always	Always

B.88.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.88.5. IDL Operation

B.88.6. Exceptions

This instruction does not generate synchronous exceptions.

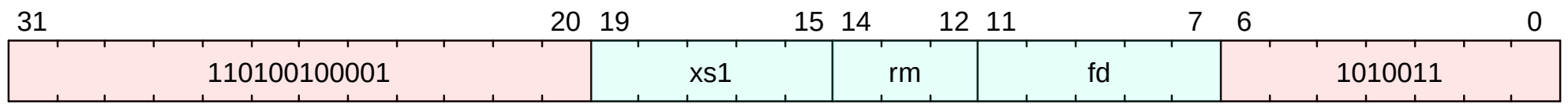
B.89. fcvt.d.wu

Floating-Point Convert Unsigned Word to Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.89.1. Encoding



B.89.2. Description

The `fcvt.d.wu` instruction converts a 32-bit unsigned integer in integer register `xs1` into a double-precision floating-point number in floating-point register `fd`. Note `fcvt.d.wu` always produces an exact result and is unaffected by rounding mode.

B.89.3. Access

M	S	U
Always	Always	Always

B.89.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.89.5. IDL Operation

B.89.6. Exceptions

This instruction does not generate synchronous exceptions.

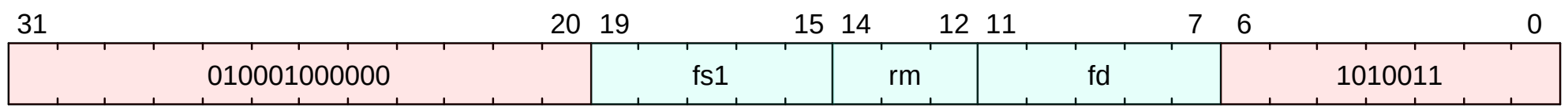
B.90. fcvt.h.s

Convert half-precision float to a single-precision float

This instruction is defined by:

(Zfhmin $\square$ Zhinxmin)

B.90.1. Encoding



B.90.2. Description

Converts a half-precision number in floating-point register *fs1* into a single-precision floating-point number in floating-point register *fd*.

[fcvt.h.s](#) rounds according to the *rm* field.

All floating-point conversion instructions set the Inexact exception flag if the rounded result differs from the operand value and the Invalid exception flag is not set.

B.90.3. Access

M	S	U
Always	Always	Always

B.90.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.90.5. IDL Operation

```
check_f_ok($encoding);
Bits<16> hp_value = f[fs1][15:0];
Bits<1> sign = hp_value[15];
Bits<5> exp = hp_value[14:10];
Bits<10> frac = hp_value[9:0];
if (exp == 0x1F) {
    if (frac != 0) {
        if ((hp_value & 0x0200) != 0) {
            set_fp_flag(FpFlag::NV);
        }
        f[fd] = HP_CANONICAL_NAN;
    } else {
        f[fd] = packToF32UI(sign, 0xFF, 0);
    }
} else {
    if (exp != 0) {
        if (frac != 0) {
            f[fd] = packToF32UI(sign, 0, 0);
        } else {
            Bits<6> norm_exp;
            (norm_exp, frac = softfloat_normSubnormalF16Sig(frac));
            exp = norm_exp - 1;
            f[fd] = packToF32UI(sign, exp + 0x70, frac << 13);
        }
    } else {
        f[fd] = packToF32UI(sign, exp + 0x70, frac << 13);
    }
}
mark_f_state_dirty();
```

B.90.6. Sail Operation

```
{
```

```

assert(sizeof(xlen) >= 64);
let rs1_val_LU = X(rs1)[63..0];
match (select_instr_or_fcsr_rm (rm)) {
  None() => { handle_illegal(); RETIRE_FAIL },
  Some(rm') => {
    let rm_3b = encdec_rounding_mode(rm');
    let (fflags, rd_val_H) = riscv_ui64ToF16 (rm_3b, rs1_val_LU);

    accrue_fflags(fflags);
    F_or_X_H(rd) = rd_val_H;
    RETIRE_SUCCESS
  }
}
}

```

B.90.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

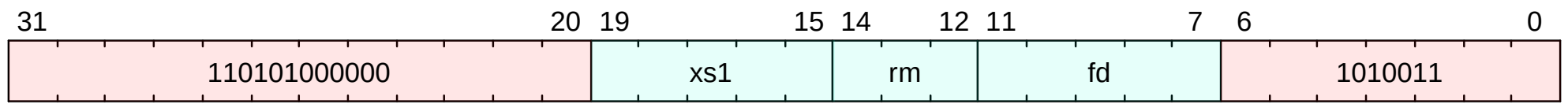
B.91. fcvt.h.w

Floating-point Convert Word to Half-precision

This instruction is defined by:

(Zfh $\square$ Zhinx)

B.91.1. Encoding



B.91.2. Description

fcvt.h.w converts a 32-bit signed integer to a half-precision floating-point number.

B.91.3. Access

M	S	U
Always	Always	Always

B.91.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.91.5. IDL Operation

B.91.6. Exceptions

This instruction does not generate synchronous exceptions.

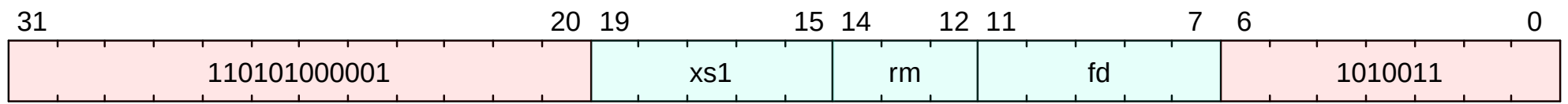
B.92. fcvt.h.wu

Floating-point Convert Unsigned Word to Half-precision

This instruction is defined by:

(Zfh $\square$ Zhinx)

B.92.1. Encoding



B.92.2. Description

fcvt.h.wu converts a 32-bit unsigned integer to a half-precision floating-point number.

B.92.3. Access

M	S	U
Always	Always	Always

B.92.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.92.5. IDL Operation

B.92.6. Exceptions

This instruction does not generate synchronous exceptions.

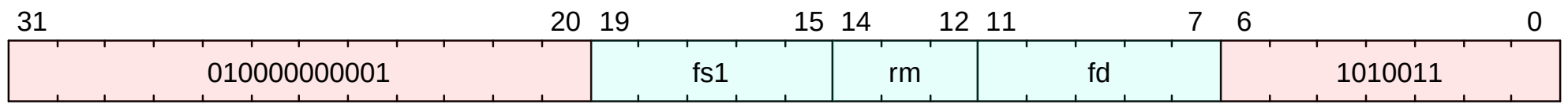
B.93. fcvt.s.d

Floating-Point Convert Double-Precision to Single-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.93.1. Encoding



B.93.2. Description

The `fcvt.s.d` instruction converts a double-precision floating-point number to a single-precision floating-point number. This is encoded in the OP-FP major opcode space and both the source and destination are floating-point registers. The `xs2` field encodes the datatype of the source, and the `fmt` field encodes the datatype of the destination. `fcvt.s.d` rounds according to the `rm` field.

B.93.3. Access

M	S	U
Always	Always	Always

B.93.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.93.5. IDL Operation

B.93.6. Exceptions

This instruction does not generate synchronous exceptions.

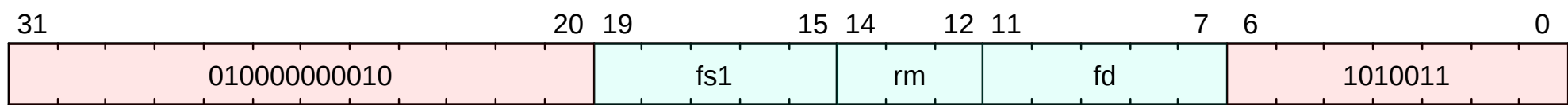
B.94. fcvt.s.h

Convert single-precision float to a half-precision float

This instruction is defined by:

(Zfhmin $\square$ Zhinxmin)

B.94.1. Encoding



B.94.2. Description

Converts a single-precision number in floating-point register *fs1* into a half-precision floating-point number in floating-point register *fd*.

[fcvt.s.h](#) will never round, and so the 'rm' field is effectively ignored.

B.94.3. Access

M	S	U
Always	Always	Always

B.94.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.94.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = f[fs1][31:0];
Bits<1> sign = sp_value[31];
Bits<8> exp = sp_value[30:23];
Bits<23> frac = sp_value[22:0];
if (exp == 0xFF) {
  if (frac != 0) {
    if ((sp_value & 0x00400000) != 0) {
      set_fp_flag(FpFlag::NV);
    }
    f[fd] = nan_box<16, FLEN>(HP_CANONICAL_NAN);
  } else {
    f[fd] = nan_box<16, FLEN>(packToF16UI(sign, 0x1F, 0));
  }
} else {
  Bits<16> frac16 = (frac >> 9) | frac & 0x1ff) != 0 ? 1 : 0);   if ((exp | frac16) == 0) {      f[fd] = nan_box<16,
FLEN>(packToF16UI(sign, 0, 0;
  } else {
    assert(false, "TODO: implement roundPackToF16");
  }
}
mark_f_state_dirty();
```

B.94.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_H) = riscv_ui64ToF16 (rm_3b, rs1_val_LU);

      accrue_fflags(fflags);
      F_or_X_H(rd) = rd_val_H;
```

```
    RETIRE_SUCCESS
  }
}
```

B.94.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

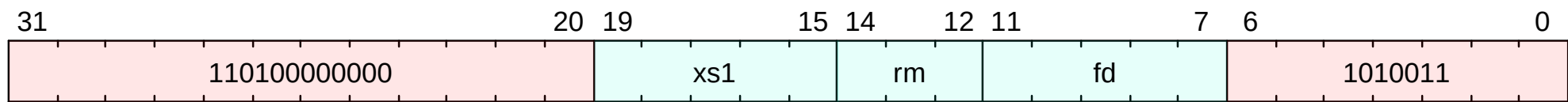
B.95. fcvt.s.w

Floating-Point Convert Word to Single-Precision

This instruction is defined by:

F

B.95.1. Encoding



B.95.2. Description

The `fcvt.s.w` instruction converts a 32-bit signed integer in integer register `xs1` into a floating-point number in floating-point register `fd`.

All floating-point to integer and integer to floating-point conversion instructions round according to the `rm` field.

A floating-point register can be initialized to floating-point positive zero using `fcvt.s.w fd, x0`, which will never set any exception flags.

All floating-point conversion instructions set the Inexact exception flag if the rounded result differs from the operand value and the Invalid exception flag is not set.

B.95.3. Access

M	S	U
Always	Always	Always

B.95.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.95.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode rounding_mode = rm_to_mode(rm, $encoding);
f[fd] = i32_to_f32(X[xs1], rounding_mode);
mark_f_state_dirty();
```

B.95.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_ui64ToF32 (rm_3b, rs1_val_LU);

      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_S;
      RETIRE_SUCCESS
    }
  }
}
```

B.95.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

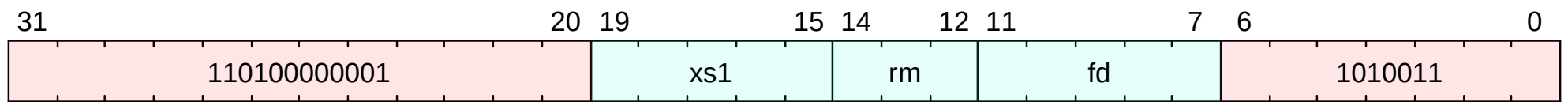
B.96. fcvt.s.wu

Floating-Point Convert Unsigned Word to Single-Precision

This instruction is defined by:

F

B.96.1. Encoding



B.96.2. Description

The `fcvt.s.wu` instruction converts a 32-bit unsigned integer in integer register `xs1` into a floating-point number in floating-point register `fd`.

All floating-point to integer and integer to floating-point conversion instructions round according to the `rm` field.

A floating-point register can be initialized to floating-point positive zero using `fcvt.s.w rd, x0`, which will never set any exception flags.

All floating-point conversion instructions set the Inexact exception flag if the rounded result differs from the operand value and the Invalid exception flag is not set.

B.96.3. Access

M	S	U
Always	Always	Always

B.96.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.96.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode rounding_mode = rm_to_mode(rm, $encoding);
f[fd] = ui32_to_f32(X[xs1], rounding_mode);
mark_f_state_dirty();
```

B.96.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_ui64ToF32 (rm_3b, rs1_val_LU);

      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_S;
      RETIRE_SUCCESS
    }
  }
}
```

B.96.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

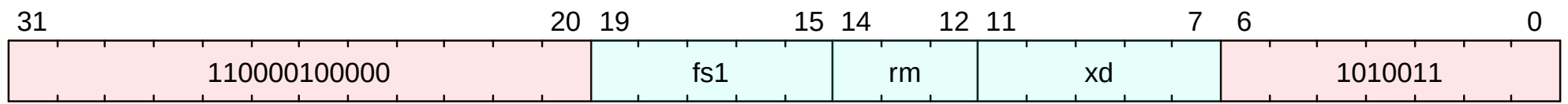
B.97. fcvt.w.d

Floating-Point Convert Double-Precision to Word

This instruction is defined by:

(D $\square$ Zdinx)

B.97.1. Encoding



B.97.2. Description

The `fcvt.w.d` instruction converts a double-precision floating-point number in floating-point register `fs1` to a signed 32-bit integer, in integer register `xd`.

B.97.3. Access

M	S	U
Always	Always	Always

B.97.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.97.5. IDL Operation

B.97.6. Exceptions

This instruction does not generate synchronous exceptions.

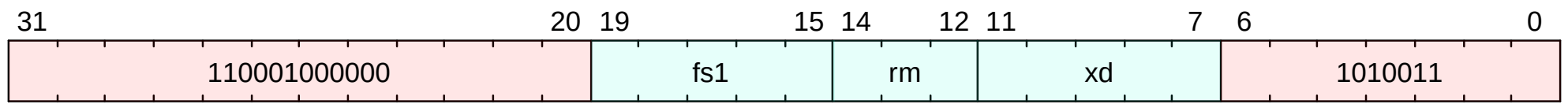
B.98. fcvt.w.h

Floating-point Convert Half-precision to Word

This instruction is defined by:

(Zfh $\square$ Zhinx)

B.98.1. Encoding



B.98.2. Description

fcvt.w.h converts a half-precision floating-point number to a signed 32-bit integer.

B.98.3. Access

M	S	U
Always	Always	Always

B.98.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.98.5. IDL Operation

B.98.6. Exceptions

This instruction does not generate synchronous exceptions.

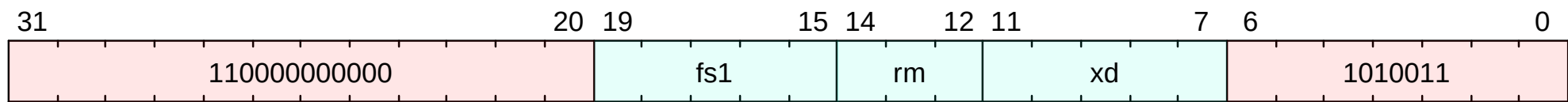
B.99. fcvt.w.s

Floating-Point Convert Single-Precision to Word

This instruction is defined by:

F

B.99.1. Encoding



B.99.2. Description

The `fcvt.w.s` instruction converts a floating-point number in floating-point register `fs1` to a signed 32-bit integer in integer register `xd`. For `XLEN > 32`, `fcvt.w.s` sign-extends the 32-bit result to the destination register width.

If the rounded result is not representable as a 32-bit signed integer, it is clipped to the nearest value and the invalid flag is set.

The range of valid inputs and behavior for invalid inputs are:

	Value
Minimum valid input (after rounding)	-2^{31}
Maximum valid input (after rounding)	$2^{31} - 1$
Output for out-of-range negative input	-2^{31}
Output for <code><code>-&infin;</code></code>	-2^{31}
Output for out-of-range positive input	$2^{31} - 1$
Output for <code><code>+&infin;</code></code> for <code><code>NaN</code></code>	$2^{31} - 1$

All floating-point to integer and integer to floating-point conversion instructions round according to the `rm` field.

A floating-point register can be initialized to floating-point positive zero using `fcvt.s.w xd, x0`, which will never set any exception flags.

All floating-point conversion instructions set the Inexact exception flag if the rounded result differs from the operand value and the Invalid exception flag is not set.

B.99.3. Access

M	S	U
Always	Always	Always

B.99.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.99.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode rounding_mode = rm_to_mode(rm, $encoding);
X[xd] = f32_to_i32(f[fs1], rounding_mode);
```

B.99.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_ui64ToF32 (rm_3b, rs1_val_LU);
```



```
    accrue_fflags(fflags);
    F_or_X_S(rd) = rd_val_S;
    RETIRE_SUCCESS
  }
}
```

B.99.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

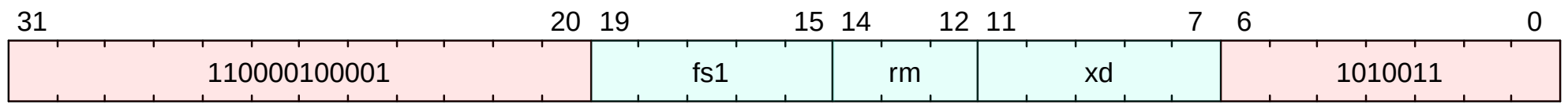
B.100. fcvt.wu.d

Floating-Point Convert Double-Precision to Unsigned Word

This instruction is defined by:

(D $\square$ Zdinx)

B.100.1. Encoding



B.100.2. Description

The `fcvt.wu.d` instruction converts a double-precision floating-point number in floating-point register `fs1` to an unsigned 32-bit integer, in integer register `xd`.

B.100.3. Access

M	S	U
Always	Always	Always

B.100.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.100.5. IDL Operation

B.100.6. Exceptions

This instruction does not generate synchronous exceptions.

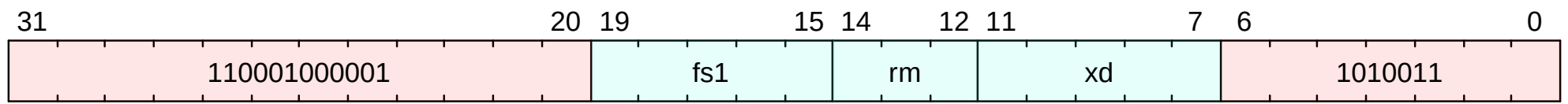
B.101. fcvt.wu.h

Floating-point Convert Half-precision to Word

This instruction is defined by:

(Zfh ☐ Zhinx)

B.101.1. Encoding



B.101.2. Description

fcvt.wu.h converts a half-precision floating-point number to a signed 32-bit unsigned integer.

B.101.3. Access

M	S	U
Always	Always	Always

B.101.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.101.5. IDL Operation

B.101.6. Exceptions

This instruction does not generate synchronous exceptions.

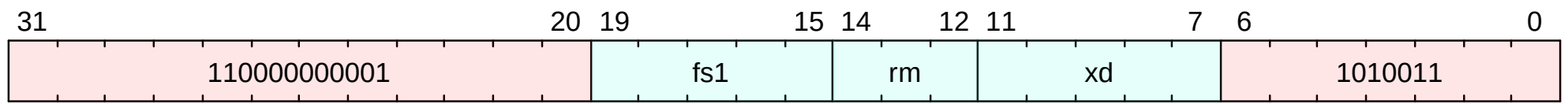
B.102. fcvt.wu.s

Floating-Point Convert Single-Precision to Unsigned Word

This instruction is defined by:

F

B.102.1. Encoding



B.102.2. Description

Converts a floating-point number in floating-point register `fs1` to an unsigned 32-bit integer in integer register `xd`. For $XLEN > 32$, `fcvt.wu.s` sign-extends the 32-bit result to the destination register width.

If the rounded result is not representable as a 32-bit unsigned integer, it is clipped to the nearest value and the invalid flag is set.

The range of valid inputs and behavior for invalid inputs are:

	Value
Minimum valid input (after rounding)	0
Maximum valid input (after rounding)	$2^{32} - 1$
Output for out-of-range negative input	0
Output for <code><code>-&infin;</code></code>	0
Output for out-of-range positive input	$2^{32} - 1$
Output for <code><code>+&infin;</code></code> for <code><code>NaN</code></code>	$2^{32} - 1$

All floating-point to integer and integer to floating-point conversion instructions round according to the `rm` field.

A floating-point register can be initialized to floating-point positive zero using `fcvt.s.w xd, x0`, which will never set any exception flags.

All floating-point conversion instructions set the Inexact exception flag if the rounded result differs from the operand value and the Invalid exception flag is not set.

B.102.3. Access

M	S	U
Always	Always	Always

B.102.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> xd = $encoding[11:7];
```

B.102.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode rounding_mode = rm_to_mode(rm, $encoding);
X[xd] = f32_to_ui32(f[fs1], rounding_mode);
```

B.102.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_ui64ToF32 (rm_3b, rs1_val_LU);
```

```
    accrue_fflags(fflags);
    F_or_X_S(rd) = rd_val_S;
    RETIRE_SUCCESS
  }
}
```

B.102.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

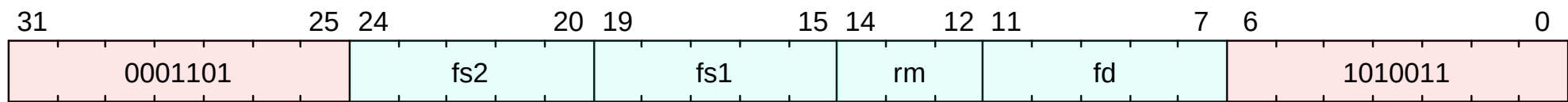
B.103. fdiv.d

Floating-Point Divide Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.103.1. Encoding



B.103.2. Description

The `fdiv.d` instruction performs the double-precision floating-point division of `fs1` by `fs2`. It is defined analogously to its single-precision counterpart, but operates on double-precision operands and produces double-precision results.

B.103.3. Access

M	S	U
Always	Always	Always

B.103.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3>  rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.103.5. IDL Operation

B.103.6. Exceptions

This instruction does not generate synchronous exceptions.

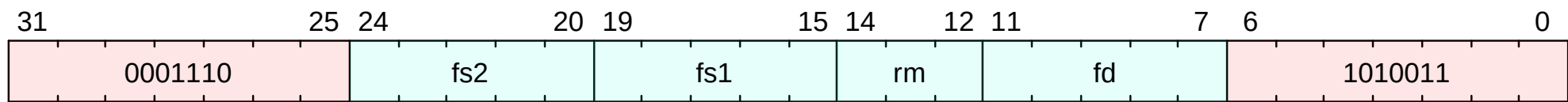
B.104. fdiv.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.104.1. Encoding



B.104.2. Description

No description available.

B.104.3. Access

M	S	U
Always	Always	Always

B.104.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.104.5. IDL Operation

B.104.6. Exceptions

This instruction does not generate synchronous exceptions.

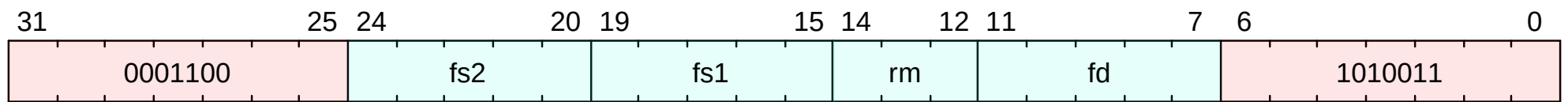
B.105. fdiv.s

Floating-Point Divide Single-Precision

This instruction is defined by:

F

B.105.1. Encoding



B.105.2. Description

The [fdiv.s](#) instruction performs the single-precision floating-point division of **fs1** by **fs2**, and writes the final result to **fd**.

B.105.3. Access

M	S	U
Always	Always	Always

B.105.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.105.5. IDL Operation

B.105.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) = match op {
        FADD_S => riscv_f32Add (rm_3b, rs1_val_32b, rs2_val_32b),
        FSUB_S => riscv_f32Sub (rm_3b, rs1_val_32b, rs2_val_32b),
        FMUL_S => riscv_f32Mul (rm_3b, rs1_val_32b, rs2_val_32b),
        FDIV_S => riscv_f32Div (rm_3b, rs1_val_32b, rs2_val_32b)
      };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.105.7. Exceptions

This instruction does not generate synchronous exceptions.

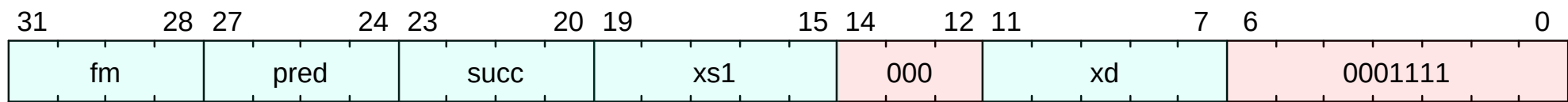
B.106. fence

Memory ordering fence

This instruction is defined by:

I

B.106.1. Encoding



B.106.2. Description

Orders memory operations.

The [fence](#) instruction is used to order device I/O and memory accesses as viewed by other RISC-V harts and external devices or coprocessors. Any combination of device input (I), device output (O), memory reads (R), and memory writes (W) may be ordered with respect to any combination of the same. Informally, no other RISC-V hart or external device can observe any operation in the *successor* set following a [fence](#) before any operation in the *predecessor* set preceding the [fence](#).

The predecessor and successor fields have the same format to specify operation types:

pred				succ			
27	26	25	24	23	22	21	20
PI	PO	PR	PW	SI	SO	SR	SW

Table 15. Fence mode encoding

fm field	Mnemonic	Meaning
0000	<i>none</i>	Normal Fence
1000	TSO	With FENCE <i>RW, RW</i> : exclude write-to-read ordering; otherwise: <i>Reserved for future use.</i>
<i>other</i>		<i>Reserved for future use.</i>

When the mode field *fm* is **0001** and both the predecessor and successor sets are 'RW', then the instruction acts as a special-case [fence.tso](#). [fence.tso](#) orders all load operations in its predecessor set before all memory operations in its successor set, and all store operations in its predecessor set before all store operations in its successor set. This leaves non-AMO store operations in the 'fence.tso's predecessor set unordered with non-AMO loads in its successor set.

When mode field *fm* is not **0001**, or when mode field *fm* is **0001** but the *pred* and *succ* fields are not both 'RW' (0x3), then the fence acts as a baseline fence (*e.g.*, *fm* is effectively **0000**). This is unaffected by the FIOM bits, described below (implicit promotion does not change how [fence.tso](#) is decoded).

The **xs1** and **xd** fields are unused and ignored.

In modes other than M-mode, [fence](#) is further affected by [menvcfg.FIOM](#), [senvcfg.FIOM](#)<% if ext?(:H) %>, and/or [henvcfg.FIOM](#)<% end %> as follows:

Table 16. Effective PR/PW/SR/SW in (H)S-mode

menvcfg.FIOM	pred.PI pred.PO succ.SI succ.SO	→	effective PR effective PW effective SR effective SW
0	-		from encoding
1	0		from encoding
1	1		1

Table 17. Effective PR/PW/SR/SW in U-mode

menvcfg.FIOM	senvcfg.FIOM	pred.PI pred.PO succ.SI succ.SO	→	effective PR effective PW effective SR effective SW
0	0	-		from encoding
0	1	0		from encoding
0	1	1		1
1	-	0		from encoding

menvcfg.FIOM	senvcfg.FIOM	pred.PI pred.PO succ.SI succ.SO	→ → → →	effective PR effective PW effective SR effective SW
1	-	1		1

<%- if ext?:(H) -%> .Effective PR/PW/SR/SW in VS-mode and VU-mode

menvcfg.FIOM	henvcfg.FIOM	pred.PI pred.PO succ.SI succ.SO	→ → → →	effective PR effective PW effective SR effective SW
0	0	-		from encoding
0	1	0		from encoding
0	1	1		1
1	-	0		from encoding
1	-	1		1

<%- end -%>

B.106.3. Access

M	S	U
Always	Always	Always

B.106.4. Decode Variables

```
Bits<4> fm = $encoding[31:28];
Bits<4> pred = $encoding[27:24];
Bits<4> succ = $encoding[23:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.106.5. IDL Operation

```
Boolean pred_i = pred[3] == 1;
Boolean pred_o = pred[2] == 1;
Boolean pred_r = pred[1] == 1;
Boolean pred_w = pred[0] == 1;
Boolean succ_i = succ[3] == 1;
Boolean succ_o = succ[2] == 1;
Boolean succ_r = succ[1] == 1;
Boolean succ_w = succ[0] == 1;
if (mode() == PrivilegeMode::S) {
  if (CSR[menvcfg].FIOM == 1) {
    if (pred_i) {
      pred_r = true;
    }
    if (pred_o) {
      pred_w = true;
    }
    if (succ_i) {
      succ_r = true;
    }
    if (succ_o) {
      succ_w = true;
    }
  }
} else if (mode() == PrivilegeMode::U) {
  if ((CSR[menvcfg].FIOM | CSR[senvcfg].FIOM) == 1) {
    if (pred_i) {
      pred_r = true;
    }
    if (pred_o) {
      pred_w = true;
    }
    if (succ_i) {
```

```

        succ_r = true;
    }
    if (succ_o) {
        succ_w = true;
    }
}
} else if (mode() == PrivilegeMode::VS || mode() == PrivilegeMode::VU) {
    if ((CSR[menvcfg].FIOM | CSR[henvcfg].FIOM) == 1) {
        if (pred_i) {
            pred_r = true;
        }
        if (pred_o) {
            pred_w = true;
        }
        if (succ_i) {
            succ_r = true;
        }
        if (succ_o) {
            succ_w = true;
        }
    }
}
}
fence(pred_i, pred_o, pred_r, pred_w, succ_i, succ_o, succ_r, succ_w);

```

B.106.6. Sail Operation

```

{
    // If the FIOM bit in menvcfg/senvcfg is set then the I/O bits can imply R/W.
    let fiom = is_fiom_active();
    let pred = effective_fence_set(pred, fiom);
    let succ = effective_fence_set(succ, fiom);

    match (pred, succ) {
        (_ : bits(2) @ 0b11, _ : bits(2) @ 0b11) => __barrier(Barrier_RISCV_rw_rw()),
        (_ : bits(2) @ 0b10, _ : bits(2) @ 0b11) => __barrier(Barrier_RISCV_r_rw()),
        (_ : bits(2) @ 0b10, _ : bits(2) @ 0b10) => __barrier(Barrier_RISCV_r_r()),
        (_ : bits(2) @ 0b11, _ : bits(2) @ 0b01) => __barrier(Barrier_RISCV_rw_w()),
        (_ : bits(2) @ 0b01, _ : bits(2) @ 0b01) => __barrier(Barrier_RISCV_w_w()),
        (_ : bits(2) @ 0b01, _ : bits(2) @ 0b11) => __barrier(Barrier_RISCV_w_rw()),
        (_ : bits(2) @ 0b11, _ : bits(2) @ 0b10) => __barrier(Barrier_RISCV_rw_r()),
        (_ : bits(2) @ 0b10, _ : bits(2) @ 0b01) => __barrier(Barrier_RISCV_r_w()),
        (_ : bits(2) @ 0b01, _ : bits(2) @ 0b10) => __barrier(Barrier_RISCV_w_r()),

        (_ : bits(4) , _ : bits(2) @ 0b00) => (),
        (_ : bits(2) @ 0b00, _ : bits(4) ) => (),

        _ => { print("FIXME: unsupported fence");
              () }
    };
    RETIRE_SUCCESS
}

```

B.106.7. Exceptions

This instruction does not generate synchronous exceptions.

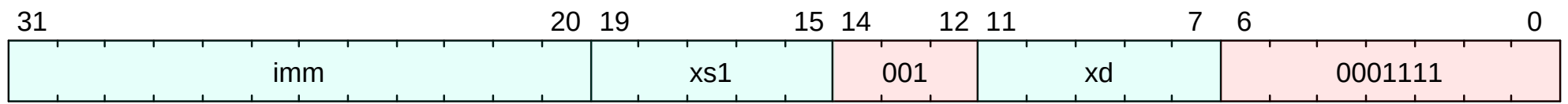
B.107. fence.i

Instruction fence

This instruction is defined by:

[Zifencei](#)

B.107.1. Encoding



B.107.2. Description

The FENCE.I instruction is used to synchronize the instruction and data streams. RISC-V does not guarantee that stores to instruction memory will be made visible to instruction fetches on a RISC-V hart until that hart executes a FENCE.I instruction. A FENCE.I instruction ensures that a subsequent instruction fetch on a RISC-V hart will see any previous data stores already visible to the same RISC-V hart. FENCE.I does *not* ensure that other RISC-V harts' instruction fetches will observe the local hart's stores in a multiprocessor system. To make a store to instruction memory visible to all RISC-V harts, the writing hart also has to execute a data FENCE before requesting that all remote RISC-V harts execute a FENCE.I.

The unused fields in the FENCE.I instruction, *imm*[11:0], *xs1*, and *xd*, are reserved for finer-grain fences in future extensions. For forward compatibility, base implementations shall ignore these fields, and standard software shall zero these fields.



Because FENCE.I only orders stores with a hart's own instruction fetches, application code should only rely upon FENCE.I if the application thread will not be migrated to a different hart. The EEI can provide mechanisms for efficient multiprocessor instruction-stream synchronization.

B.107.3. Access

M	S	U
Always	Always	Always

B.107.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.107.5. IDL Operation

```
ifence();
```

B.107.6. Sail Operation

```
{ /* __barrier(Barrier_RISCV_i); */ RETIRE_SUCCESS }
```

B.107.7. Exceptions

This instruction does not generate synchronous exceptions.

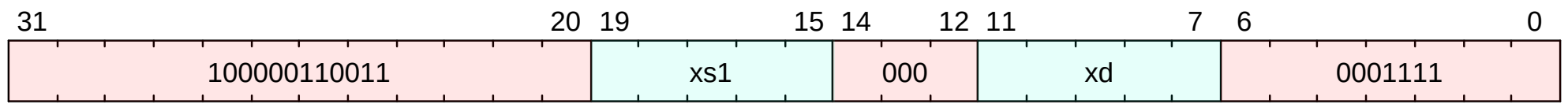
B.108. fence.tso

Memory ordering fence, total store ordering

This instruction is defined by:

I

B.108.1. Encoding



B.108.2. Description

Orders memory operations.

[fence.tso](#) orders all load operations in its predecessor set before all memory operations in its successor set, and all store operations in its predecessor set before all store operations in its successor set. This leaves non-AMO store operations in the 'fence.tso's predecessor set unordered with non-AMO loads in its successor set.

The [xs1](#) and [xd](#) fields are unused and ignored.

In modes other than M-mode, [fence.tso](#) is further affected by [menvcfg.FIOM](#), [senvcfg.FIOM](#)<% if ext?(:H) %>, and/or [henvcfg.FIOM](#)<% end %>.

B.108.3. Access

M	S	U
Always	Always	Always

B.108.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.108.5. IDL Operation

```
fence_tso();
```

B.108.6. Sail Operation

```
{
  match (pred, succ) {
    (_ : bits(2) @ 0b11, _ : bits(2) @ 0b11) => sail_barrier(Barrier_RISCV_tso),
    (_ : bits(2) @ 0b00, _ : bits(2) @ 0b00) => (),

    _ => { print("FIXME: unsupported fence");
          () }
  };
  RETIRE_SUCCESS
}
```

B.108.7. Exceptions

This instruction does not generate synchronous exceptions.

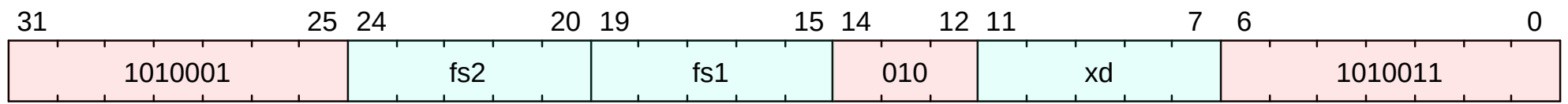
B.109. feq.d

Floating-Point Equal Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.109.1. Encoding



B.109.2. Description

The [feq.d](#) instruction writes 1 to [xd](#) if [fs1](#) and [fs2](#) are equal, and 0 otherwise. It is defined analogously to its single-precision counterpart, but operates on double-precision operands.

B.109.3. Access

M	S	U
Always	Always	Always

B.109.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.109.5. IDL Operation

B.109.6. Exceptions

This instruction does not generate synchronous exceptions.

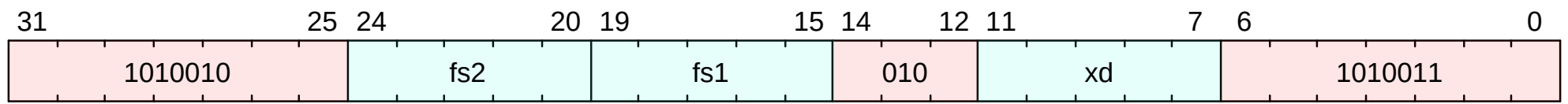
B.110. feq.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.110.1. Encoding



B.110.2. Description

No description available.

B.110.3. Access

M	S	U
Always	Always	Always

B.110.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.110.5. IDL Operation

B.110.6. Exceptions

This instruction does not generate synchronous exceptions.

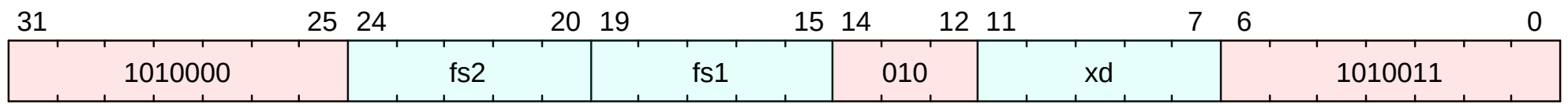
B.111. feq.s

Floating-Point Equal Single-Precision

This instruction is defined by:

F

B.111.1. Encoding



B.111.2. Description

The `feq.s` instruction writes 1 to `xd` if `fs1` and `fs2` are equal, and 0 otherwise. If either operand is NaN, the result is 0 (not equal). If either operand is a signaling NaN, the invalid flag is set. Positive zero is considered equal to negative zero.

B.111.3. Access

M	S	U
Always	Always	Always

B.111.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.111.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value_a = f[fs1][31:0];
Bits<32> sp_value_b = f[fs1][31:0];
if (is_sp_nan?(sp_value_a) || is_sp_nan?(sp_value_b)) {
  if (is_sp_signaling_nan?(sp_value_a) || is_sp_signaling_nan?(sp_value_b)) {
    set_fp_flag(FpFlag::NV);
  }
  X[xd] = 0;
} else {
  X[xd] = sp_value_a == sp_value_b || ((sp_value_a | sp_value_b)[30:0] == 0 ? 1 : 0);
}
```

B.111.6. Sail Operation

```
{
  let rs1_val_S = F_or_X_S(rs1);
  let rs2_val_S = F_or_X_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32Le (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.111.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

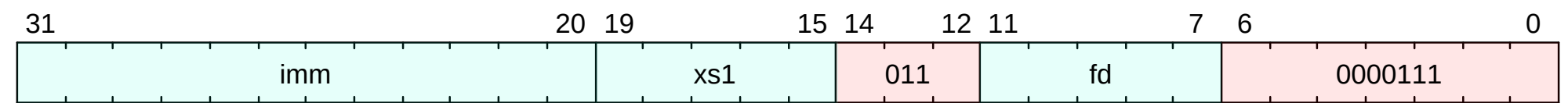
B.112. fld

Floating-Point Load Double-Precision

This instruction is defined by:

D

B.112.1. Encoding



B.112.2. Description

The `fld` instruction loads a double-precision floating-point value from memory into floating-point register `fd`. It is guaranteed to execute atomically if the effective address is naturally aligned and $XLEN \geq 64$. It doesn't modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

B.112.3. Access

M	S	U
Always	Always	Always

B.112.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.112.5. IDL Operation

B.112.6. Exceptions

This instruction does not generate synchronous exceptions.

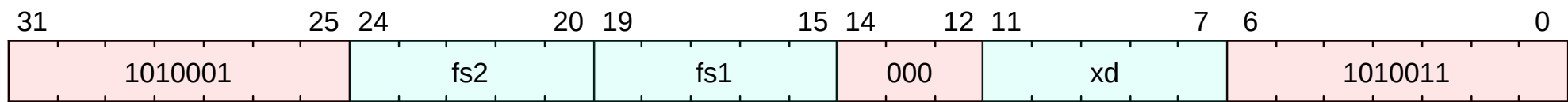
B.113. fle.d

Floating-Point Less Than or Equal Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.113.1. Encoding



B.113.2. Description

The fle.d instruction writes 1 to xd if fs1 is less than or equal to fs2, and 0 otherwise. It is defined analogously to its single-precision counterpart, but operates on double-precision operands.

B.113.3. Access

M	S	U
Always	Always	Always

B.113.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.113.5. IDL Operation

B.113.6. Exceptions

This instruction does not generate synchronous exceptions.

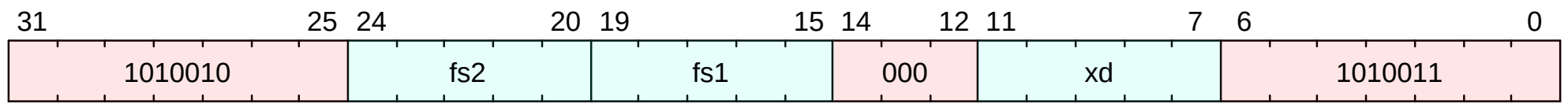
B.114. fle.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.114.1. Encoding



B.114.2. Description

No description available.

B.114.3. Access

M	S	U
Always	Always	Always

B.114.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.114.5. IDL Operation

B.114.6. Exceptions

This instruction does not generate synchronous exceptions.

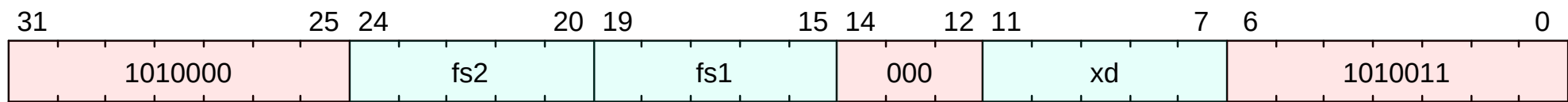
B.115. fle.s

Floating-Point Less Than or Equal Single-Precision

This instruction is defined by:

F

B.115.1. Encoding



B.115.2. Description

The [fle.s](#) instruction writes 1 to `xd` if `fs1` is less than or equal to `fs2`, and 0 otherwise. If either operand is NaN, the result is 0 (not equal). If either operand is a NaN (signaling or quiet), the invalid flag is set. Positive zero and negative zero are considered equal.

B.115.3. Access

M	S	U
Always	Always	Always

B.115.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.115.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value_a = f[fs1][31:0];
Bits<32> sp_value_b = f[fs2][31:0];
if (is_sp_nan?(sp_value_a) || is_sp_nan?(sp_value_b)) {
  if (is_sp_signaling_nan?(sp_value_a) || is_sp_signaling_nan?(sp_value_b)) {
    set_fp_flag(FpFlag::NV);
  }
  X[xd] = 0;
} else {
  X[xd] = sp_value_a == sp_value_b || ((sp_value_a | sp_value_b)[30:0] == 0 ? 1 : 0);
}
```

B.115.6. Sail Operation

```
{
  let rs1_val_S = F_or_X_S(rs1);
  let rs2_val_S = F_or_X_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32Le (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.115.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

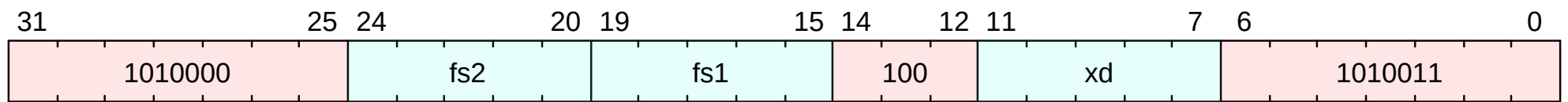
B.116. fleq.s

Floating-Point Less Than or Equal Quiet Single-Precision

This instruction is defined by:

Zfa

B.116.1. Encoding



B.116.2. Description

The [fleq.s](#) instruction is defined like the [fle.s](#) instruction, except that quiet NaN inputs do not cause the invalid operation exception flag to be set.

B.116.3. Access

M	S	U
Always	Always	Always

B.116.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.116.5. IDL Operation

B.116.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);
  let rs2_val_S = F_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32le_quiet  (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.116.7. Exceptions

This instruction does not generate synchronous exceptions.

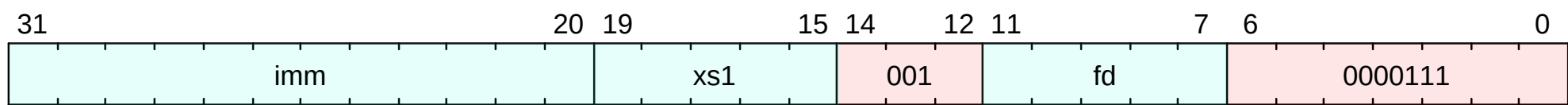
B.117. flh

Half-precision floating-point load

This instruction is defined by:

Zfhmin

B.117.1. Encoding



B.117.2. Description

The [flh](#) instruction loads a single-precision floating-point value from memory at address *xs1* + *imm* into floating-point register *xd*.

[flh](#) does not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

[flh](#) is only guaranteed to execute atomically if the effective address is naturally aligned.

B.117.3. Access

M	S	U
Always	Always	Always

B.117.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.117.5. IDL Operation

```
check_f_ok($encoding);
XReg virtual_address = X[xs1] + $signed(imm);
Bits<16> hp_value = read_memory<16>(virtual_address, $encoding);
f[fd] = nan_box<16, FLEN>(hp_value);
mark_f_state_dirty();
```

B.117.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(rs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(addr, _) => {
          let (aq, rl, res) = (false, false, false);
          match (width) {
            BYTE => { handle_illegal(); RETIRE_FAIL },
            HALF =>
              process_fload16(rd, vaddr, mem_read(Read(Data), addr, 2, aq, rl, res)),
            WORD =>
              process_fload32(rd, vaddr, mem_read(Read(Data), addr, 4, aq, rl, res)),
            DOUBLE if sizeof(flen) >= 64 =>
              process_fload64(rd, vaddr, mem_read(Read(Data), addr, 8, aq, rl, res)),
            _ => report_invalid_width(__FILE__, __LINE__, width, "floating point load"),
          }
        }
      }
  }
}
```



```
}
```

B.117.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

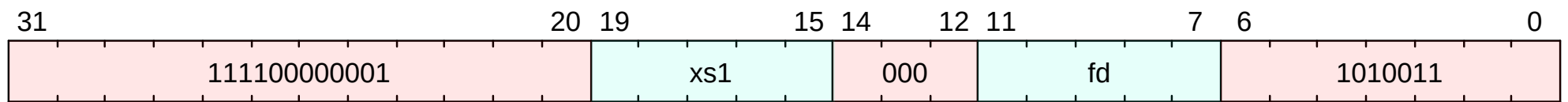
B.118. fli.s

No synopsis available

This instruction is defined by:

Zfa

B.118.1. Encoding



B.118.2. Description

No description available.

B.118.3. Access

M	S	U
Always	Always	Always

B.118.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.118.5. IDL Operation

B.118.6. Sail Operation

```
{
  let bits : bits(32) = match constantidx {
    0b000000 => { 0xbf800000 }, /* -1.0 */
    0b000001 => { 0x00800000 }, /* minimum positive normal */
    0b000010 => { 0x37800000 }, /* 1.0 * 2^-16 */
    0b000011 => { 0x38000000 }, /* 1.0 * 2^-15 */
    0b000100 => { 0x3b800000 }, /* 1.0 * 2^-8 */
    0b000101 => { 0x3c000000 }, /* 1.0 * 2^-7 */
    0b000110 => { 0x3d800000 }, /* 1.0 * 2^-4 */
    0b000111 => { 0x3e000000 }, /* 1.0 * 2^-3 */
    0b010000 => { 0x3e800000 }, /* 0.25 */
    0b010001 => { 0x3ea00000 }, /* 0.3125 */
    0b010010 => { 0x3ec00000 }, /* 0.375 */
    0b010011 => { 0x3ee00000 }, /* 0.4375 */
    0b010100 => { 0x3f000000 }, /* 0.5 */
    0b010101 => { 0x3f200000 }, /* 0.625 */
    0b010110 => { 0x3f400000 }, /* 0.75 */
    0b010111 => { 0x3f600000 }, /* 0.875 */
    0b100000 => { 0x3f800000 }, /* 1.0 */
    0b100001 => { 0x3fa00000 }, /* 1.25 */
    0b100010 => { 0x3fc00000 }, /* 1.5 */
    0b100011 => { 0x3fe00000 }, /* 1.75 */
    0b101000 => { 0x40000000 }, /* 2.0 */
    0b101001 => { 0x40200000 }, /* 2.5 */
    0b101010 => { 0x40400000 }, /* 3 */
    0b101011 => { 0x40800000 }, /* 4 */
    0b110000 => { 0x41000000 }, /* 8 */
    0b110001 => { 0x41800000 }, /* 16 */
    0b110010 => { 0x43000000 }, /* 2^7 */
    0b110011 => { 0x43800000 }, /* 2^8 */
    0b111000 => { 0x47000000 }, /* 2^15 */
    0b111001 => { 0x47800000 }, /* 2^16 */
    0b111010 => { 0x7f800000 }, /* +inf */
    0b111011 => { canonical_NaN_S() },
  };
};
```



```
F_S(rd) = bits;  
RETIRE_SUCCESS  
}
```

B.118.7. Exceptions

This instruction does not generate synchronous exceptions.

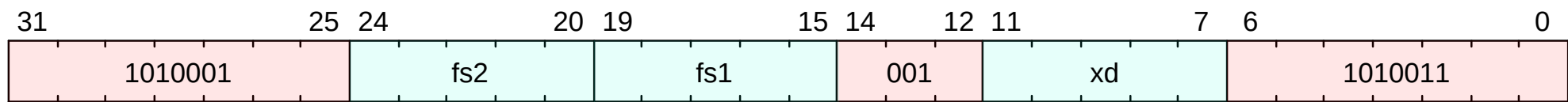
B.119. flt.d

Floating-Point Less Than Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.119.1. Encoding



B.119.2. Description

The `flt.d` instruction writes 1 to `xd` if `fs1` is less than `fs2`, and 0 otherwise. It is defined analogously to its single-precision counterpart, but operates on double-precision operands.

B.119.3. Access

M	S	U
Always	Always	Always

B.119.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.119.5. IDL Operation

B.119.6. Exceptions

This instruction does not generate synchronous exceptions.

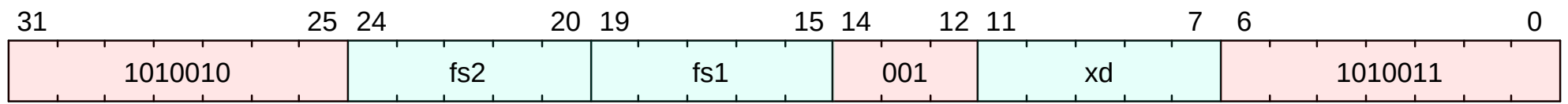
B.120. flt.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.120.1. Encoding



B.120.2. Description

No description available.

B.120.3. Access

M	S	U
Always	Always	Always

B.120.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.120.5. IDL Operation

B.120.6. Exceptions

This instruction does not generate synchronous exceptions.

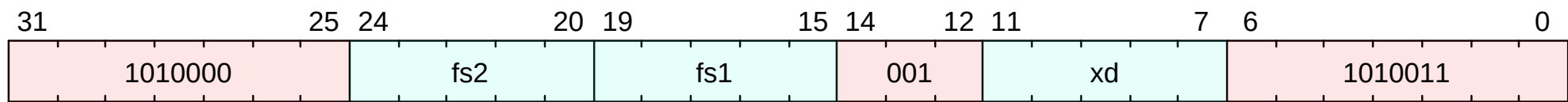
B.121. flt.s

Floating-Point Less Than Single-Precision

This instruction is defined by:

F

B.121.1. Encoding



B.121.2. Description

The [flt.s](#) instruction writes 1 to [xd](#) if [fs1](#) is less than [fs2](#), and 0 otherwise. If either operand is NaN, the result is 0 (not equal). If either operand is a NaN (signaling or quiet), the invalid flag is set.

B.121.3. Access

M	S	U
Always	Always	Always

B.121.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.121.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value_a = f[fs1][31:0];
Bits<32> sp_value_b = f[fs2][31:0];
if (is_sp_nan?(sp_value_a) || is_sp_nan?(sp_value_b)) {
    set_fp_flag(FpFlag::NV);
    X[xd] = 0;
} else {
    Boolean sign_a = sp_value_a[31] == 1;
    Boolean sign_b = sp_value_b[31] == 1;
    Boolean a_lt_b = (sign_a != sign_b) ? (sign_a && sp_value_a[30:0] | sp_value_b[30:0]) != 0 : sp_value_a != sp_value_b && (sign_a
!= (sp_value_a < sp_value_b));
    X[xd] = a_lt_b ? 1 : 0;
}
```

B.121.6. Sail Operation

```
{
    let rs1_val_S = F_or_X_S(rs1);
    let rs2_val_S = F_or_X_S(rs2);

    let (fflags, rd_val) : (bits_fflags, bool) =
        riscv_f32le (rs1_val_S, rs2_val_S);

    accrue_fflags(fflags);
    X(rd) = zero_extend(bool_to_bits(rd_val));
    RETIRE_SUCCESS
}
```

B.121.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

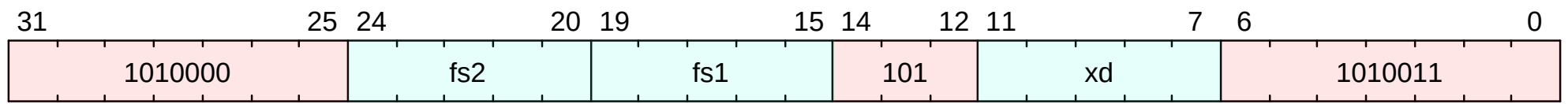
B.122. fltq.s

Floating-Point Less Than Quiet Single-Precision

This instruction is defined by:

[Zfa](#)

B.122.1. Encoding



B.122.2. Description

The [fltq.s](#) is defined like the [flt.s](#) instruction, except that quiet NaN inputs do not cause the invalid operation exception flag to be set.

B.122.3. Access

M	S	U
Always	Always	Always

B.122.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.122.5. IDL Operation

B.122.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);
  let rs2_val_S = F_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32Lt_quiet  (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.122.7. Exceptions

This instruction does not generate synchronous exceptions.

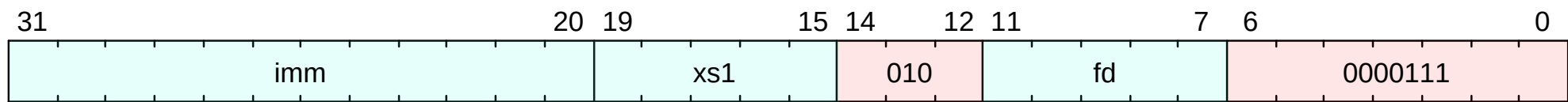
B.123. flw

Floating-Point Load Single-Precision

This instruction is defined by:

F

B.123.1. Encoding



B.123.2. Description

The [flw](#) instruction loads a single-precision floating-point value from memory at address [xs1](#) + [imm](#) into floating-point register [fd](#). It does not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

B.123.3. Access

M	S	U
Always	Always	Always

B.123.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.123.5. IDL Operation

```
check_f_ok($encoding);
XReg virtual_address = X[xs1] + $signed(imm);
Bits<32> sp_value = read_memory<32>(virtual_address, $encoding);
if (implemented?(ExtensionName::D)) {
    f[fd] = nan_box<32, 64>(sp_value);
} else {
    f[fd] = sp_value;
}
mark_f_state_dirty();
```

B.123.6. Sail Operation

```
{
    let offset : xlenbits = sign_extend(imm);
    /* Get the address, X(rs1) + offset.
       Some extensions perform additional checks on address validity. */
    match ext_data_get_addr(rs1, offset, Read(Data), width) {
        Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
        Ext_DataAddr_OK(vaddr) =>
            if check_misaligned(vaddr, width)
            then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
            else match translateAddr(vaddr, Read(Data)) {
                TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
                TR_Address(addr, _) => {
                    let (aq, rl, res) = (false, false, false);
                    match (width) {
                        BYTE => { handle_illegal(); RETIRE_FAIL },
                        HALF =>
                            process_fload16(rd, vaddr, mem_read(Read(Data), addr, 2, aq, rl, res)),
                        WORD =>
                            process_fload32(rd, vaddr, mem_read(Read(Data), addr, 4, aq, rl, res)),
                        DOUBLE if sizeof(flen) >= 64 =>
                            process_fload64(rd, vaddr, mem_read(Read(Data), addr, 8, aq, rl, res)),
                        _ => report_invalid_width(__FILE__, __LINE__, width, "floating point load"),
                    }
                }
            }
    }
}
```



```
}  
}
```

B.123.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

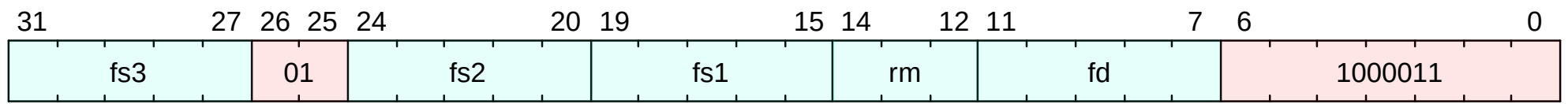
B.124. fmadd.d

Floating-Point Multiply-Add Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.124.1. Encoding



B.124.2. Description

The `fmadd.d` instruction multiplies the values in `fs1` and `fs2`, adds the value in `fs3`, and writes the final result to `fd`.

B.124.3. Access

M	S	U
Always	Always	Always

B.124.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.124.5. IDL Operation

B.124.6. Exceptions

This instruction does not generate synchronous exceptions.

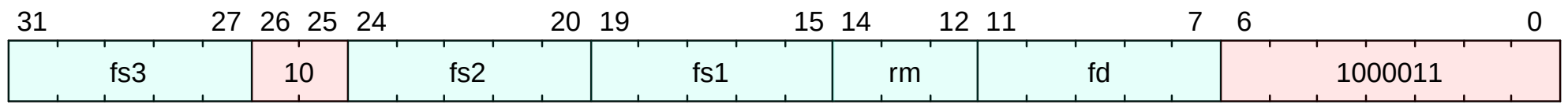
B.125. fmadd.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.125.1. Encoding



B.125.2. Description

No description available.

B.125.3. Access

M	S	U
Always	Always	Always

B.125.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.125.5. IDL Operation

B.125.6. Exceptions

This instruction does not generate synchronous exceptions.

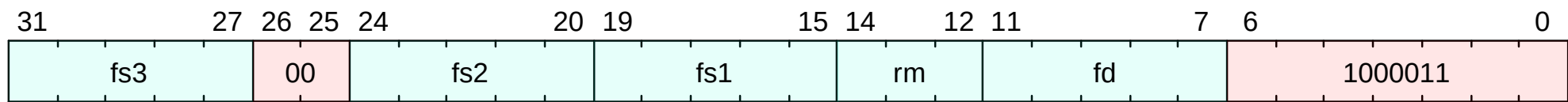
B.126. fmadd.s

Floating-Point Multiply-Add Single-Precision

This instruction is defined by:

F

B.126.1. Encoding



B.126.2. Description

The [fmadd.s](#) multiplies the values in [fs1](#) and [fs2](#), adds the value in [fs3](#), and writes the final result to [fd](#).

B.126.3. Access

M	S	U
Always	Always	Always

B.126.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.126.5. IDL Operation

B.126.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  let rs3_val_32b = F_or_X_S(rs3);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) =
        match op {
          FMADD_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, rs3_val_32b),
          FMSUB_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, negate_S (rs3_val_32b)),
          FNMSUB_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, rs3_val_32b),
          FNMADD_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, negate_S (rs3_val_32b))
        };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.126.7. Exceptions

This instruction does not generate synchronous exceptions.

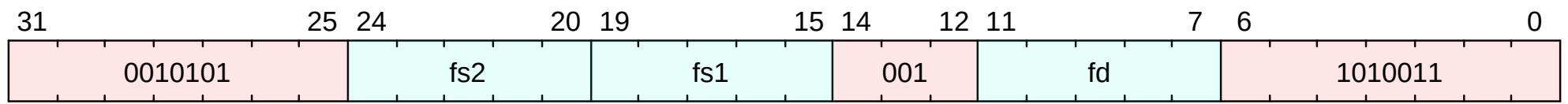
B.127. fmax.d

Floating-Point Maximum-Number Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.127.1. Encoding



B.127.2. Description

The `fmax.d` instruction writes larger of `fs1` and `fs2` to `fd`. For the purposes of this instruction, the value `-0.0` is considered to be less than the value `+0.0`. If both inputs are NaNs, the result is the canonical NaN. If only one operand is a NaN, the result is the non-NaN operand. Signaling NaN inputs set the invalid operation exception flag, even when the result is not NaN.

B.127.3. Access

M	S	U
Always	Always	Always

B.127.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.127.5. IDL Operation

B.127.6. Exceptions

This instruction does not generate synchronous exceptions.

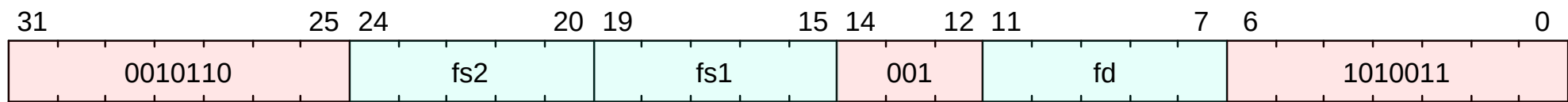
B.128. fmax.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.128.1. Encoding



B.128.2. Description

No description available.

B.128.3. Access

M	S	U
Always	Always	Always

B.128.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.128.5. IDL Operation

B.128.6. Exceptions

This instruction does not generate synchronous exceptions.

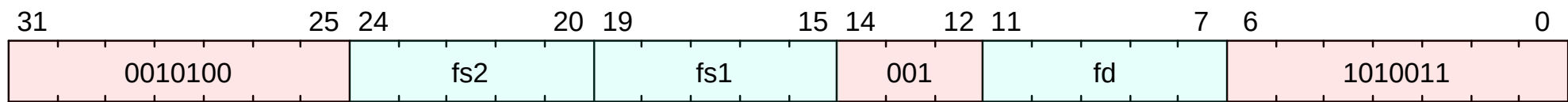
B.129. fmax.s

Floating-Point Maximum-Number Single-Precision

This instruction is defined by:

F

B.129.1. Encoding



B.129.2. Description

The `fmax.s` instruction writes larger of `fs1` and `fs2` to `fd`. For the purposes of this instruction, the value `-0.0` is considered to be less than the value `+0.0`. If both inputs are NaNs, the result is the canonical NaN. If only one operand is a NaN, the result is the non-NaN operand. Signaling NaN inputs set the invalid operation exception flag, even when the result is not NaN.



Note that in version 2.2 of the F extension, the `fmin.s` and `fmax.s` instructions were amended to implement the proposed *IEEE 754-201x minimumNumber* and *maximumNumber* operations, rather than the *IEEE 754-2008 minNum* and *maxNum* operations. These operations differ in their handling of signaling NaNs.

B.129.3. Access

M	S	U
Always	Always	Always

B.129.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.129.5. IDL Operation

B.129.6. Sail Operation

```
{
  let rs1_val_S = F_or_X_S(rs1);
  let rs2_val_S = F_or_X_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32Le (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.129.7. Exceptions

This instruction does not generate synchronous exceptions.

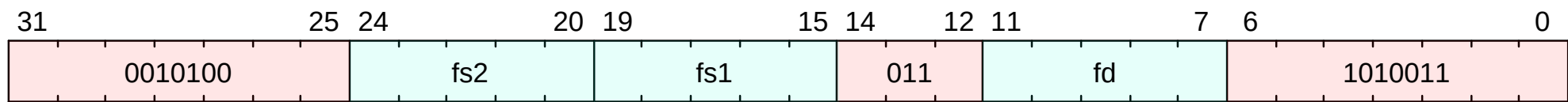
B.130. fmaxm.s

No synopsis available

This instruction is defined by:

Zfa

B.130.1. Encoding



B.130.2. Description

No description available.

B.130.3. Access

M	S	U
Always	Always	Always

B.130.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.130.5. IDL Operation

B.130.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);
  let rs2_val_S = F_S(rs2);

  let is_quiet = true;
  let (rs2_lt_rs1, fflags) = fle_S (rs2_val_S, rs1_val_S, is_quiet);

  let rd_val_S = if      (f_is_NaN_S(rs1_val_S) | f_is_NaN_S(rs2_val_S))      then canonical_NaN_S()
                  else if (f_is_neg_zero_S(rs1_val_S) & f_is_pos_zero_S(rs2_val_S)) then rs2_val_S
                  else if (f_is_neg_zero_S(rs2_val_S) & f_is_pos_zero_S(rs1_val_S)) then rs1_val_S
                  else if rs2_lt_rs1                                     then rs1_val_S
                  else /* (not rs2_lt_rs1) */                             rs2_val_S;

  accrue_fflags(fflags);
  F_S(rd) = rd_val_S;
  RETIRE_SUCCESS
}
```

B.130.7. Exceptions

This instruction does not generate synchronous exceptions.

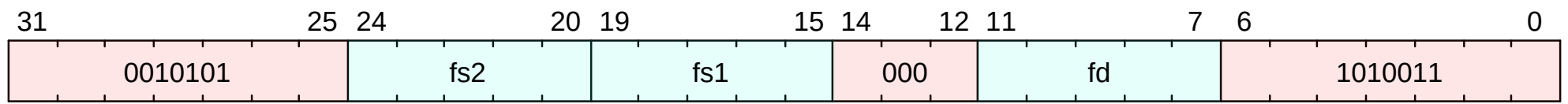
B.131. fmin.d

Floating-Point Minimum-Number Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.131.1. Encoding



B.131.2. Description

The `fmin.d` instruction writes smaller of `fs1` and `fs2` to `fd`. For the purposes of this instruction, the value `-0.0` is considered to be less than the value `+0.0`. If both inputs are NaNs, the result is the canonical NaN. If only one operand is a NaN, the result is the non-NaN operand. Signaling NaN inputs set the invalid operation exception flag, even when the result is not NaN.

B.131.3. Access

M	S	U
Always	Always	Always

B.131.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.131.5. IDL Operation

B.131.6. Exceptions

This instruction does not generate synchronous exceptions.

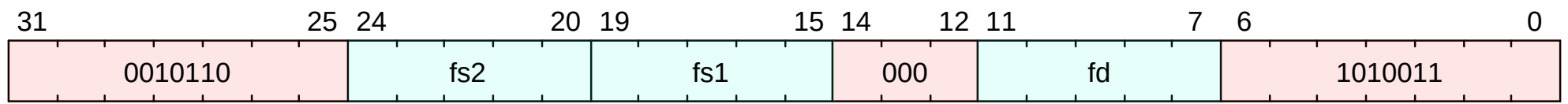
B.132. fmin.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.132.1. Encoding



B.132.2. Description

No description available.

B.132.3. Access

M	S	U
Always	Always	Always

B.132.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.132.5. IDL Operation

B.132.6. Exceptions

This instruction does not generate synchronous exceptions.

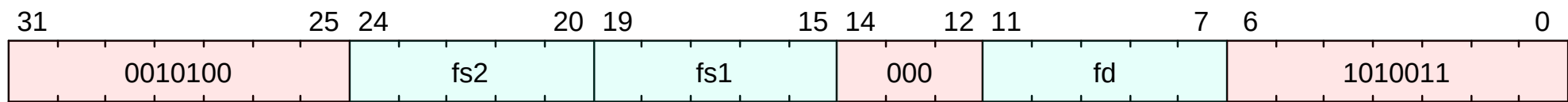
B.133. fmin.s

Floating-Point Minimum-Number Single-Precision

This instruction is defined by:

F

B.133.1. Encoding



B.133.2. Description

The [fmin.s](#) instruction writes smaller of [fs1](#) and [fs2](#) to [fd](#). For the purposes of this instruction, the value [-0.0](#) is considered to be less than the value [+0.0](#). If both inputs are NaNs, the result is the canonical NaN. If only one operand is a NaN, the result is the non-NaN operand. Signaling NaN inputs set the invalid operation exception flag, even when the result is not NaN.



Note that in version 2.2 of the F extension, the [fmin.s](#) and [fmax.s](#) instructions were amended to implement the proposed *IEEE 754-201x minimumNumber* and *maximumNumber* operations, rather than the *IEEE 754-2008 minNum* and *maxNum* operations. These operations differ in their handling of signaling NaNs.

B.133.3. Access

M	S	U
Always	Always	Always

B.133.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.133.5. IDL Operation

B.133.6. Sail Operation

```
{
  let rs1_val_S = F_or_X_S(rs1);
  let rs2_val_S = F_or_X_S(rs2);

  let (fflags, rd_val) : (bits_fflags, bool) =
    riscv_f32Le (rs1_val_S, rs2_val_S);

  accrue_fflags(fflags);
  X(rd) = zero_extend(bool_to_bits(rd_val));
  RETIRE_SUCCESS
}
```

B.133.7. Exceptions

This instruction does not generate synchronous exceptions.

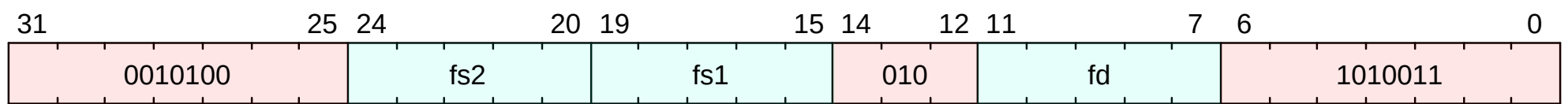
B.134. fminm.s

No synopsis available

This instruction is defined by:

[Zfa](#)

B.134.1. Encoding



B.134.2. Description

No description available.

B.134.3. Access

M	S	U
Always	Always	Always

B.134.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.134.5. IDL Operation

B.134.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);
  let rs2_val_S = F_S(rs2);

  let is_quiet = true;
  let (rs1_lt_rs2, fflags) = fle_S (rs1_val_S, rs2_val_S, is_quiet);

  let rd_val_S = if      (f_is_NaN_S(rs1_val_S) | f_is_NaN_S(rs2_val_S))      then canonical_NaN_S()
                  else if (f_is_neg_zero_S(rs1_val_S) & f_is_pos_zero_S(rs2_val_S)) then rs1_val_S
                  else if (f_is_neg_zero_S(rs2_val_S) & f_is_pos_zero_S(rs1_val_S)) then rs2_val_S
                  else if rs1_lt_rs2                                     then rs1_val_S
                  else /* (not rs1_lt_rs2) */                             rs2_val_S;

  accrue_fflags(fflags);
  F_S(rd) = rd_val_S;
  RETIRE_SUCCESS
}
```

B.134.7. Exceptions

This instruction does not generate synchronous exceptions.

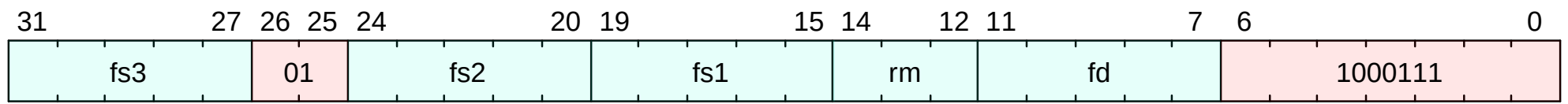
B.135. fmsub.d

Floating-Point Multiply-Subtract Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.135.1. Encoding



B.135.2. Description

The `fmsub.d` instruction multiplies the values in `fs1` and `fs2`, subtracts the value in `fs3`, and writes the final result to `fd`.

B.135.3. Access

M	S	U
Always	Always	Always

B.135.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.135.5. IDL Operation

B.135.6. Exceptions

This instruction does not generate synchronous exceptions.

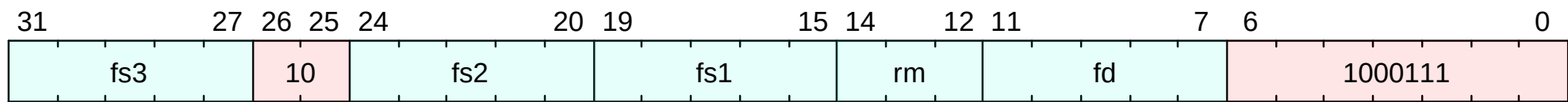
B.136. fmsub.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.136.1. Encoding



B.136.2. Description

No description available.

B.136.3. Access

M	S	U
Always	Always	Always

B.136.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.136.5. IDL Operation

B.136.6. Exceptions

This instruction does not generate synchronous exceptions.

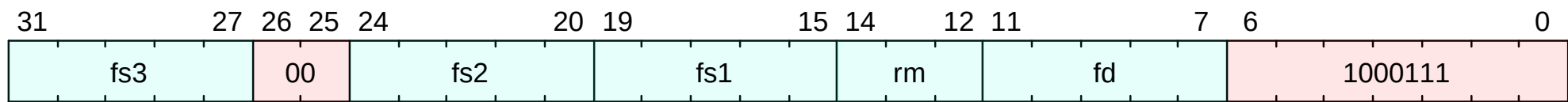
B.137. fmsub.s

Floating-Point Multiply-Subtract Single-Precision

This instruction is defined by:

F

B.137.1. Encoding



B.137.2. Description

The `fmsub.s` multiplies the values in `fs1` and `fs2`, subtracts the value in `fs3`, and writes the final result to `fd`.

B.137.3. Access

M	S	U
Always	Always	Always

B.137.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.137.5. IDL Operation

B.137.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  let rs3_val_32b = F_or_X_S(rs3);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) =
        match op {
          FMADD_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, rs3_val_32b),
          FMSUB_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, negate_S (rs3_val_32b)),
          FNMSUB_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, rs3_val_32b),
          FNMADD_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, negate_S (rs3_val_32b))
        };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.137.7. Exceptions

This instruction does not generate synchronous exceptions.

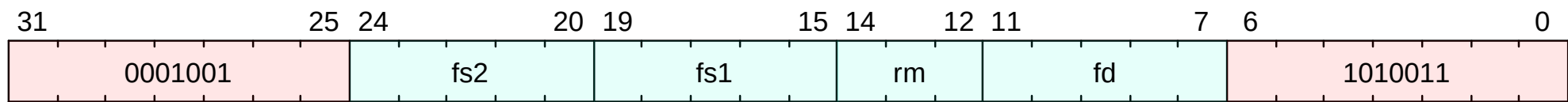
B.138. fmul.d

Floating-Point Multiply Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.138.1. Encoding



B.138.2. Description

The `fmul.d` instruction performs the double-precision floating-point multiplication between `fs1` and `fs2`. It is defined analogously to its single-precision counterpart, but operates on double-precision operands and produces double-precision results.

B.138.3. Access

M	S	U
Always	Always	Always

B.138.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3>  rm = $encoding[14:12];
Bits<5>  fd = $encoding[11:7];
```

B.138.5. IDL Operation

B.138.6. Exceptions

This instruction does not generate synchronous exceptions.

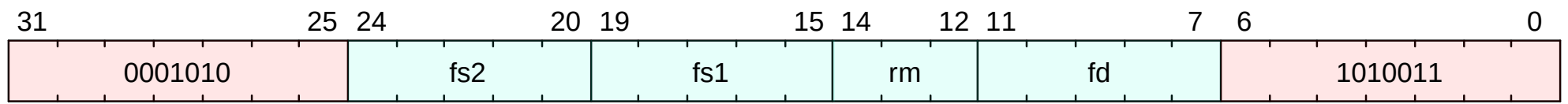
B.139. fmul.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.139.1. Encoding



B.139.2. Description

No description available.

B.139.3. Access

M	S	U
Always	Always	Always

B.139.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.139.5. IDL Operation

B.139.6. Exceptions

This instruction does not generate synchronous exceptions.

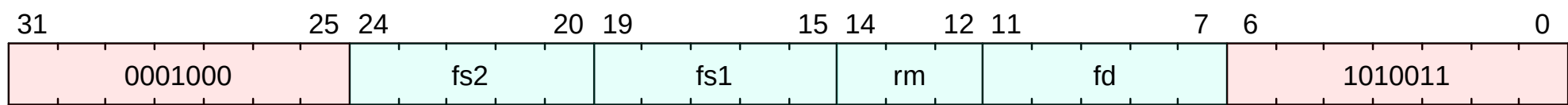
B.140. fmul.s

Floating-Point Multiply Single-Precision

This instruction is defined by:

F

B.140.1. Encoding



B.140.2. Description

The [fmul.s](#) instruction performs the single-precision floating-point multiplication between **fs1** and **fs2**, and writes the result in **fd**.

B.140.3. Access

M	S	U
Always	Always	Always

B.140.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.140.5. IDL Operation

B.140.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) = match op {
        FADD_S => riscv_f32Add (rm_3b, rs1_val_32b, rs2_val_32b),
        FSUB_S => riscv_f32Sub (rm_3b, rs1_val_32b, rs2_val_32b),
        FMUL_S => riscv_f32Mul (rm_3b, rs1_val_32b, rs2_val_32b),
        FDIV_S => riscv_f32Div (rm_3b, rs1_val_32b, rs2_val_32b)
      };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.140.7. Exceptions

This instruction does not generate synchronous exceptions.

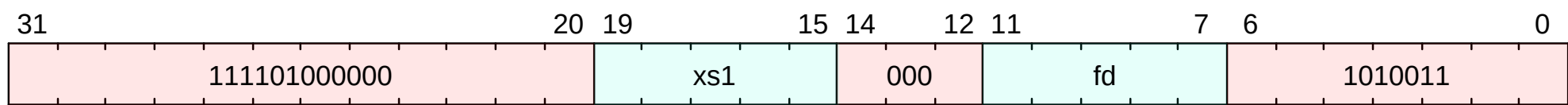
B.141. fmv.h.x

Half-precision floating-point move from integer

This instruction is defined by:

Zfhmin

B.141.1. Encoding



B.141.2. Description

Moves the half-precision value encoded in IEEE 754-2008 standard encoding from the lower 16 bits of integer register **xs1** to the floating-point register **fd**. The bits are not modified in the transfer, and in particular, the payloads of non-canonical NaNs are preserved.

B.141.3. Access

M	S	U
Always	Always	Always

B.141.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.141.5. IDL Operation

```
check_f_ok($encoding);
Bits<16> hp_value = X[xs1][15:0];
f[fd] = nan_box<16, FLEN>(hp_value);
mark_f_state_dirty();
```

B.141.6. Sail Operation

```
{
  let rs1_val_X      = X(rs1);
  let rd_val_H       = rs1_val_X [15..0];
  F(rd) = nan_box (rd_val_H);
  RETIRE_SUCCESS
}
```

B.141.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

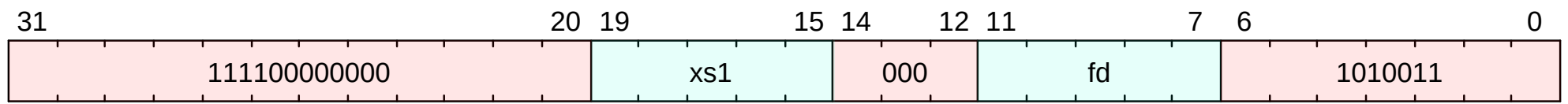
B.142. fmv.w.x

Floating-Point Move Single-Precision Word from Integer Register

This instruction is defined by:

F

B.142.1. Encoding



B.142.2. Description

The [fmv.w.x](#) instruction moves the single-precision value encoded in [IEEE 754-2008](#) standard encoding from the lower 32 bits of integer register [xs1](#) to the floating-point register [fd](#). The bits are not modified in the transfer, and in particular, the payloads of non-canonical NaNs are preserved.

B.142.3. Access

M	S	U
Always	Always	Always

B.142.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.142.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = X[xs1][31:0];
if (implemented?(ExtensionName::D)) {
  f[fd] = nan_box<32, 64>(sp_value);
} else {
  f[fd] = sp_value;
}
mark_f_state_dirty();
```

B.142.6. Sail Operation

```
{
  let rs1_val_X      = X(rs1);
  let rd_val_S      = rs1_val_X [31..0];
  F(rd) = nan_box (rd_val_S);
  RETIRE_SUCCESS
}
```

B.142.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

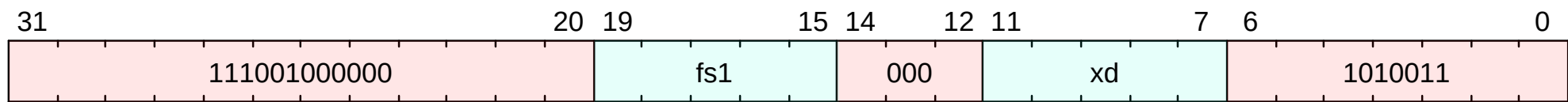
B.143. fmv.x.h

Move half-precision value from floating-point to integer register

This instruction is defined by:

Zfhmin

B.143.1. Encoding



B.143.2. Description

Moves the half-precision value in floating-point register fs1 represented in IEEE 754-2008 encoding to the lower 16 bits of integer register xd.

The bits are not modified in the transfer, and in particular, the payloads of non-canonical NaNs are preserved.

The highest XLEN-16 bits of the destination register are filled with copies of the floating-point number’s sign bit.

B.143.3. Access

M	S	U
Always	Always	Always

B.143.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.143.5. IDL Operation

```
check_f_ok($encoding);
X[xd] = sext(f[fs1][15:0], 16);
```

B.143.6. Sail Operation

```
{
  let rs1_val_X      = X(rs1);
  let rd_val_H      = rs1_val_X [15..0];
  F(rd) = nan_box (rd_val_H);
  RETIRE_SUCCESS
}
```

B.143.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

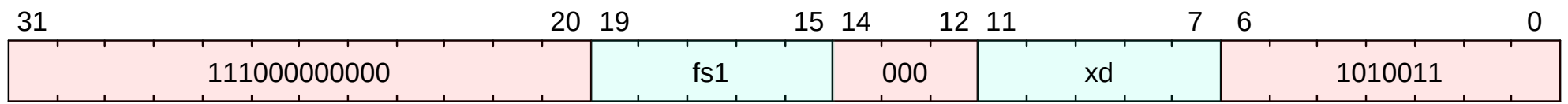
B.144. fmv.x.w

Floating-Point Move Single-Precision Word to Integer Register

This instruction is defined by:

F

B.144.1. Encoding



B.144.2. Description

The `fmv.x.w` instruction moves the single-precision value in floating-point register `fs1` represented in [IEEE 754-2008](#) encoding to the lower 32 bits of integer register `xd`. The bits are not modified in the transfer, and in particular, the payloads of non-canonical NaNs are preserved. For RV64, the higher 32 bits of the destination register are filled with copies of the floating-point number’s sign bit.

B.144.3. Access

M	S	U
Always	Always	Always

B.144.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.144.5. IDL Operation

```
check_f_ok($encoding);
X[xd] = sext(f[fs1][31:0], 32);
```

B.144.6. Sail Operation

```
{
  let rs1_val_X      = X(rs1);
  let rd_val_S       = rs1_val_X [31..0];
  F(rd) = nan_box (rd_val_S);
  RETIRE_SUCCESS
}
```

B.144.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

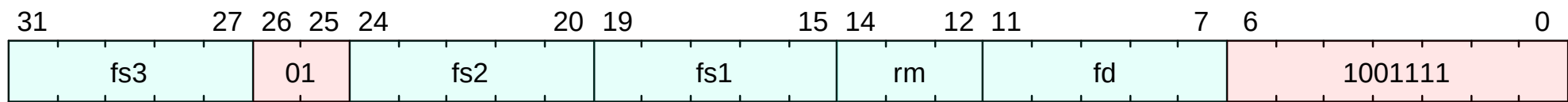
B.145. fnmadd.d

Floating-Point Negate-Multiply-Add Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.145.1. Encoding



B.145.2. Description

The `fnmadd.d` instruction multiplies the values in `fs1` and `fs2`, negates the product, subtracts the value in `fs3`, and writes the final result to `fd`.

B.145.3. Access

M	S	U
Always	Always	Always

B.145.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.145.5. IDL Operation

B.145.6. Exceptions

This instruction does not generate synchronous exceptions.

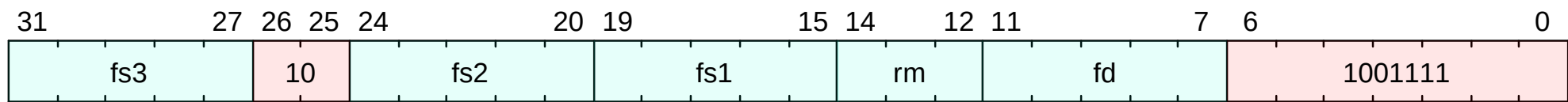
B.146. fnmadd.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.146.1. Encoding



B.146.2. Description

No description available.

B.146.3. Access

M	S	U
Always	Always	Always

B.146.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.146.5. IDL Operation

B.146.6. Exceptions

This instruction does not generate synchronous exceptions.

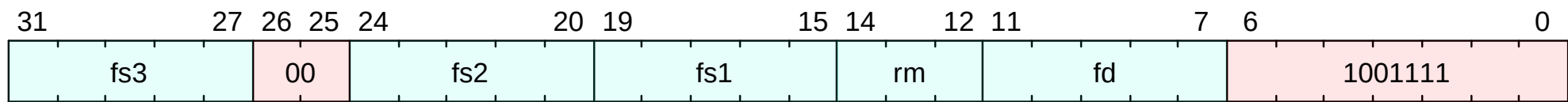
B.147. fnmadd.s

Floating-Point Negate-Multiply-Add Single-Precision

This instruction is defined by:

F

B.147.1. Encoding



B.147.2. Description

The `fnmadd.s` multiplies the values in `fs1` and `fs2`, negates the product, subtracts the value in `fs3`, and writes the final result to `fd`.

B.147.3. Access

M	S	U
Always	Always	Always

B.147.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.147.5. IDL Operation

B.147.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  let rs3_val_32b = F_or_X_S(rs3);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) =
        match op {
          FMADD_S => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, rs3_val_32b),
          FMSUB_S => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, negate_S (rs3_val_32b)),
          FNMSUB_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, rs3_val_32b),
          FNMADD_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, negate_S (rs3_val_32b))
        };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.147.7. Exceptions

This instruction does not generate synchronous exceptions.

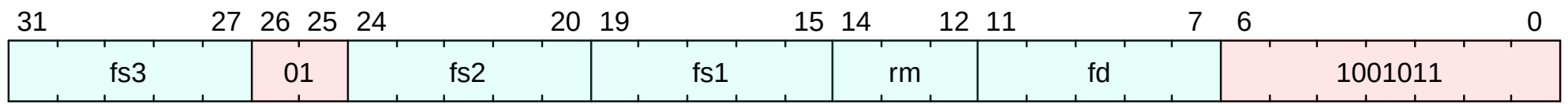
B.148. fnmsub.d

Floating-Point Negate-Multiply-Subtract Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.148.1. Encoding



B.148.2. Description

The `fnmsub.d` instruction multiplies the values in `fs1` and `fs2`, negates the product, adds the value in `fs3`, and writes the final result to `fd`.

B.148.3. Access

M	S	U
Always	Always	Always

B.148.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.148.5. IDL Operation

B.148.6. Exceptions

This instruction does not generate synchronous exceptions.

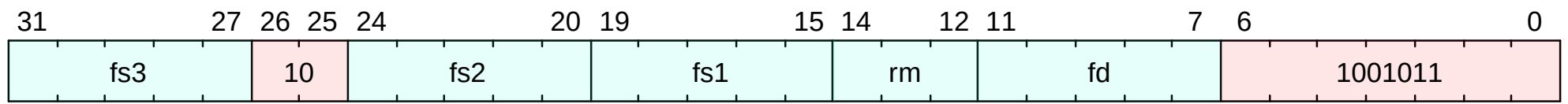
B.149. fnmsub.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.149.1. Encoding



B.149.2. Description

No description available.

B.149.3. Access

M	S	U
Always	Always	Always

B.149.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.149.5. IDL Operation

B.149.6. Exceptions

This instruction does not generate synchronous exceptions.

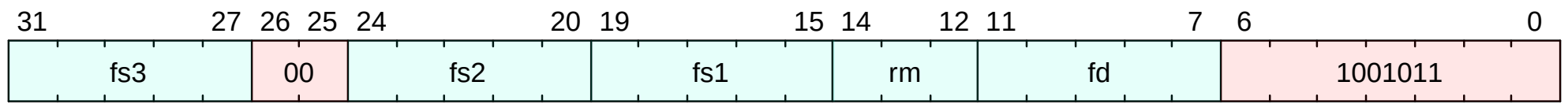
B.150. fnmsub.s

Floating-Point Negate-Multiply-Subtract Single-Precision

This instruction is defined by:

F

B.150.1. Encoding



B.150.2. Description

The [fnmsub.s](#) instruction multiplies the values in **fs1** and **fs2**, negates the product, adds the value in **fs3**, and writes the final result to **fd**.

B.150.3. Access

M	S	U
Always	Always	Always

B.150.4. Decode Variables

```
Bits<5> fs3 = $encoding[31:27];
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.150.5. IDL Operation

B.150.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  let rs3_val_32b = F_or_X_S(rs3);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) =
        match op {
          FMADD_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, rs3_val_32b),
          FMSUB_S  => riscv_f32MulAdd (rm_3b, rs1_val_32b, rs2_val_32b, negate_S (rs3_val_32b)),
          FNMSUB_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, rs3_val_32b),
          FNMADD_S => riscv_f32MulAdd (rm_3b, negate_S (rs1_val_32b), rs2_val_32b, negate_S (rs3_val_32b))
        };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.150.7. Exceptions

This instruction does not generate synchronous exceptions.

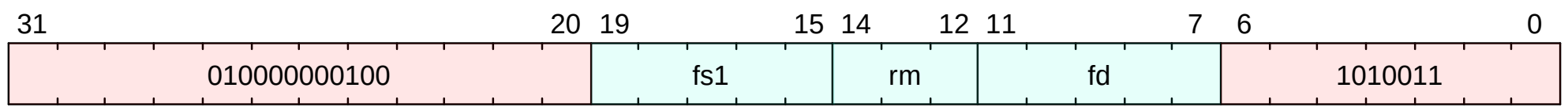
B.151. fround.s

Floating-point round single-precision float to integer

This instruction is defined by:

Zfa

B.151.1. Encoding



B.151.2. Description

Rounds the single-precision floating-point number in floating-point register *fs1* to an integer, according to the rounding mode specified in the instruction’s *rm* field.

It then writes that integer, represented as a single-precision floating-point number, to floating-point register *fd*.

Zero and infinite inputs are copied to *fd* unmodified.

Signaling NaN inputs cause the invalid operation exception flag to be set; no other exception flags are set. FROUND.S is encoded like FCVT.S.D, but with rs2=4.

B.151.3. Access

M	S	U
Always	Always	Always

B.151.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.151.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode rounding_mode = rm_to_mode(rm, $encoding);
f[fd] = round_f32_to_integral(f[fs1], rounding_mode);
mark_f_state_dirty();
```

B.151.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);

  match (select_instr_or_fcsr_rm(rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_f32roundToInt(rm_3b, rs1_val_S, false);

      accrue_fflags(fflags);
      F_S(rd) = rd_val_S;
      RETIRE_SUCCESS
    }
  }
}
```

B.151.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

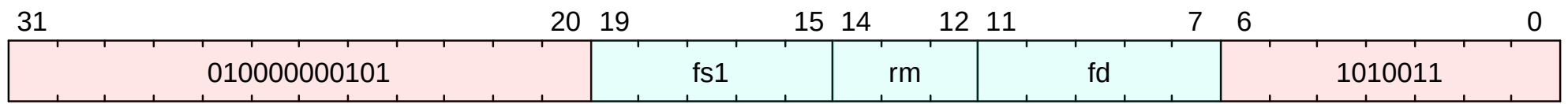
B.152. froundnx.s

Floating-point Round Single-precision to Integer with Inexact

This instruction is defined by:

Zfa

B.152.1. Encoding



B.152.2. Description

No description available.

B.152.3. Access

M	S	U
Always	Always	Always

B.152.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.152.5. IDL Operation

B.152.6. Sail Operation

```
{
  let rs1_val_S = F_S(rs1);

  match (select_instr_or_fcsr_rm(rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_f32roundToInt(rm_3b, rs1_val_S, true);

      accrue_fflags(fflags);
      F_S(rd) = rd_val_S;
      RETIRE_SUCCESS
    }
  }
}
```

B.152.7. Exceptions

This instruction does not generate synchronous exceptions.

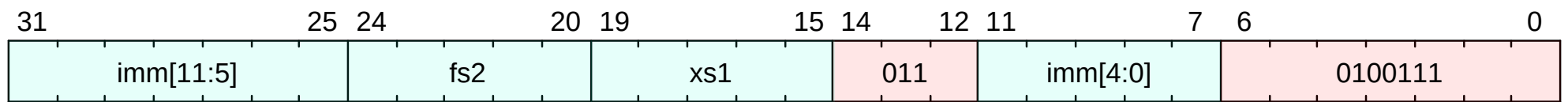
B.153. fsd

Floating-Point Store Double-Precision

This instruction is defined by:

D

B.153.1. Encoding



B.153.2. Description

The [fsd](#) instruction stores a double-precision value from the floating-point registers to memory. It is guaranteed to execute atomically if the effective address is naturally aligned and XLEN≥64. It doesn't modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

B.153.3. Access

M	S	U
Always	Always	Always

B.153.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> fs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.153.5. IDL Operation

B.153.6. Exceptions

This instruction does not generate synchronous exceptions.

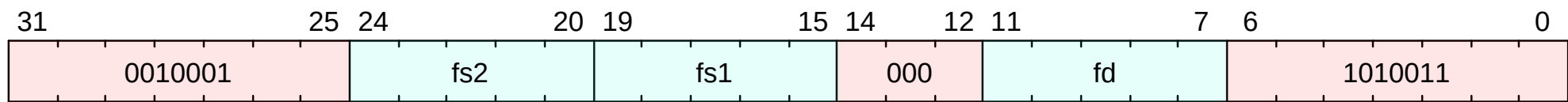
B.154. fsgnj.d

Floating-Point Sign-Inject Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.154.1. Encoding



B.154.2. Description

The `fsgnj.d` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is taken from `fs2`’s sign bit, and the result is written to the destination register ``fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.154.3. Access

M	S	U
Always	Always	Always

B.154.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.154.5. IDL Operation

B.154.6. Exceptions

This instruction does not generate synchronous exceptions.

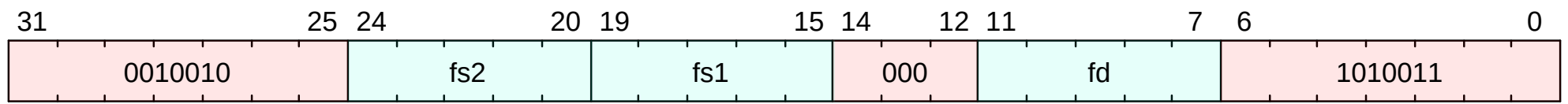
B.155. fsgnj.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.155.1. Encoding



B.155.2. Description

No description available.

B.155.3. Access

M	S	U
Always	Always	Always

B.155.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.155.5. IDL Operation

B.155.6. Exceptions

This instruction does not generate synchronous exceptions.

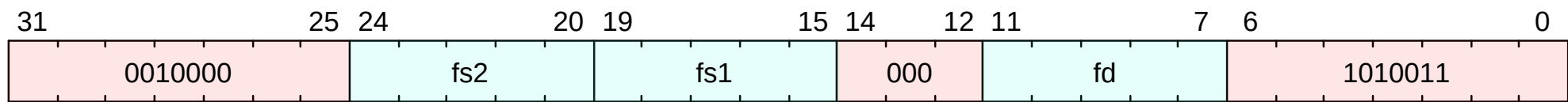
B.156. fsgnj.s

Floating-Point Sign-Inject Single-Precision

This instruction is defined by:

F

B.156.1. Encoding



B.156.2. Description

The `fsgnj.s` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is taken from `fs2`’s sign bit, and the result is written to the destination register `fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.156.3. Access

M	S	U
Always	Always	Always

B.156.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.156.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = {f[fs2][31], f[fs1][30:0]};
if (implemented?(ExtensionName::D)) {
    f[fd] = nan_box<32, 64>(sp_value);
} else {
    f[fd] = sp_value;
}
mark_f_state_dirty();
```

B.156.6. Sail Operation

```
{
    let rs1_val_S = F_or_X_S(rs1);
    let rs2_val_S = F_or_X_S(rs2);

    let (fflags, rd_val) : (bits_fflags, bool) =
        riscv_f32Le (rs1_val_S, rs2_val_S);

    accrue_fflags(fflags);
    X(rd) = zero_extend(bool_to_bits(rd_val));
    RETIRE_SUCCESS
}
```

B.156.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

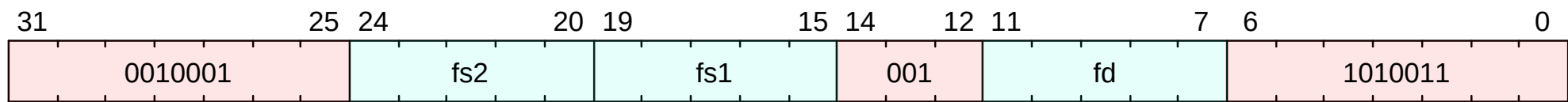
B.157. fsgnjn.d

Floating-Point Sign-Inject Negate Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.157.1. Encoding



B.157.2. Description

The `fsgnjn.d` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is opposite of `fs2`’s sign bit, and the result is written to the destination register ``fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.157.3. Access

M	S	U
Always	Always	Always

B.157.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.157.5. IDL Operation

B.157.6. Exceptions

This instruction does not generate synchronous exceptions.

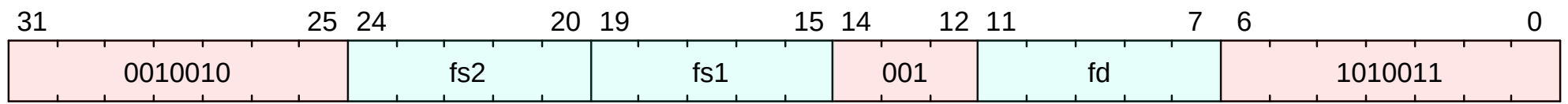
B.158. fsgnjn.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.158.1. Encoding



B.158.2. Description

No description available.

B.158.3. Access

M	S	U
Always	Always	Always

B.158.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.158.5. IDL Operation

B.158.6. Exceptions

This instruction does not generate synchronous exceptions.

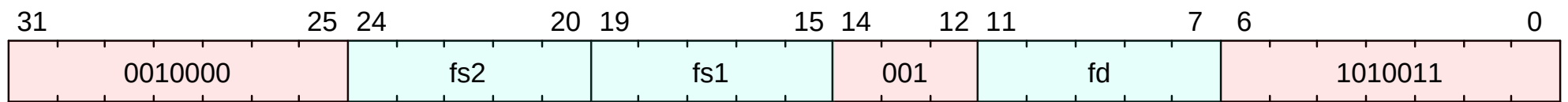
B.159. fsgnjn.s

Floating-Point Sign-Inject Negate Single-Precision

This instruction is defined by:

F

B.159.1. Encoding



B.159.2. Description

The `fsgnjn.s` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is opposite of `fs2`’s sign bit, and the result is written to the destination register `fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.159.3. Access

M	S	U
Always	Always	Always

B.159.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.159.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = {~f[fs2][31], f[fs1][30:0]};
if (implemented?(ExtensionName::D)) {
    f[fd] = nan_box<32, 64>(sp_value);
} else {
    f[fd] = sp_value;
}
mark_f_state_dirty();
```

B.159.6. Sail Operation

```
{
    let rs1_val_S = F_or_X_S(rs1);
    let rs2_val_S = F_or_X_S(rs2);

    let (fflags, rd_val) : (bits_fflags, bool) =
        riscv_f32Le (rs1_val_S, rs2_val_S);

    accrue_fflags(fflags);
    X(rd) = zero_extend(bool_to_bits(rd_val));
    RETIRE_SUCCESS
}
```

B.159.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

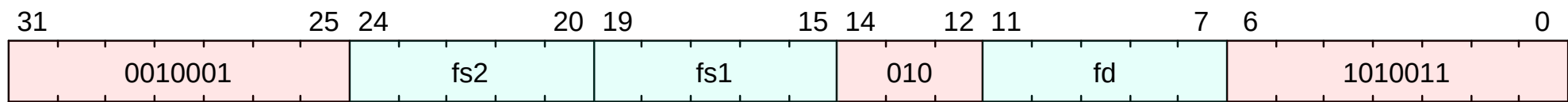
B.160. fsgnjx.d

Floating-Point Sign-Inject XOR Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.160.1. Encoding



B.160.2. Description

The `fsgnjx.d` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is the XOR of sign bits of `fs1` and `fs2`, and the result is written to the destination register `fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.160.3. Access

M	S	U
Always	Always	Always

B.160.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.160.5. IDL Operation

B.160.6. Exceptions

This instruction does not generate synchronous exceptions.

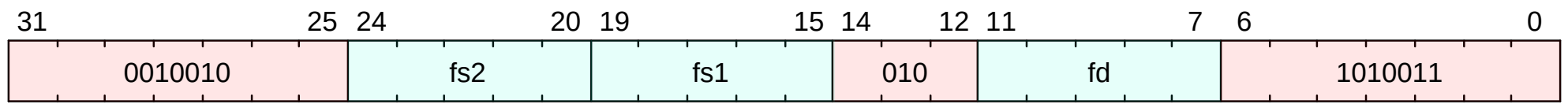
B.161. fsgnjx.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.161.1. Encoding



B.161.2. Description

No description available.

B.161.3. Access

M	S	U
Always	Always	Always

B.161.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.161.5. IDL Operation

B.161.6. Exceptions

This instruction does not generate synchronous exceptions.

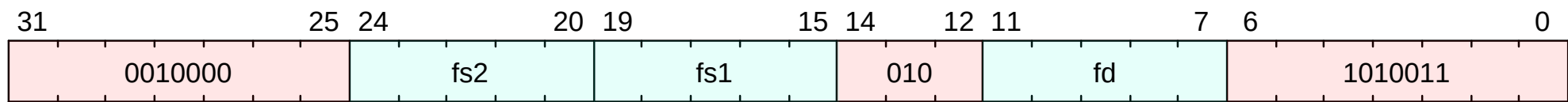
B.162. fsgnjx.s

Floating-Point Sign-Inject XOR Single-Precision

This instruction is defined by:

F

B.162.1. Encoding



B.162.2. Description

The `fsgnjx.s` instruction produces a result that takes all bits except the sign bit from `fs1`. The result’s sign bit is the XOR of sign bits of `fs1` and `fs2`, and the result is written to the destination register `fd`. Sign-injection instructions do not set floating-point exception flags, nor do they canonicalize NaNs.

B.162.3. Access

M	S	U
Always	Always	Always

B.162.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<5> fd = $encoding[11:7];
```

B.162.5. IDL Operation

```
check_f_ok($encoding);
Bits<32> sp_value = {f[fs1][31] ^ f[fs2][31], f[fs1][30:0]};
if (implemented?(ExtensionName::D)) {
    f[fd] = nan_box<32, 64>(sp_value);
} else {
    f[fd] = sp_value;
}
mark_f_state_dirty();
```

B.162.6. Sail Operation

```
{
    let rs1_val_S = F_or_X_S(rs1);
    let rs2_val_S = F_or_X_S(rs2);

    let (fflags, rd_val) : (bits_fflags, bool) =
        riscv_f32Le (rs1_val_S, rs2_val_S);

    accrue_fflags(fflags);
    X(rd) = zero_extend(bool_to_bits(rd_val));
    RETIRE_SUCCESS
}
```

B.162.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

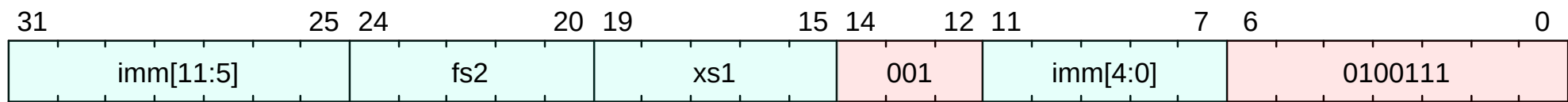
B.163. fsh

Half-precision floating-point store

This instruction is defined by:

Zfhmin

B.163.1. Encoding



B.163.2. Description

The [fsh](#) instruction stores a half-precision floating-point value from register *xd* to memory at address *xs1* + *imm*.

[fsh](#) does not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

[fsh](#) ignores all but the lower 16 bits in *fs2*.

[fsh](#) is only guaranteed to execute atomically if the effective address is naturally aligned.

B.163.3. Access

M	S	U
Always	Always	Always

B.163.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> xs1 = $encoding[19:15];
Bits<5> fs2 = $encoding[24:20];
```

B.163.5. IDL Operation

```
check_f_ok($encoding);
XReg virtual_address = X[xs1] + $signed(imm);
Bits<16> hp_value = f[fs2][15:0];
write_memory<16>(virtual_address, hp_value, $encoding);
```

B.163.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  let (aq, rl, con) = (false, false, false);
  /* Get the address, X(rs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1, offset, Write(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Write(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(addr, _) => {
          let eares : MemoryOpResult(unit) = match width {
            BYTE => MemValue () /* bogus placeholder for illegal size */,
            HALF => mem_write_ea(addr, 2, aq, rl, false),
            WORD => mem_write_ea(addr, 4, aq, rl, false),
            DOUBLE => mem_write_ea(addr, 8, aq, rl, false)
          };
          match (eares) {
            MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
            MemValue(_) => {
              let rs2_val = F(rs2);
              match (width) {
                BYTE => { handle_illegal(); RETIRE_FAIL },
```

```

        HALF => process_fstore (vaddr, mem_write_value(addr, 2, rs2_val[15..0], aq, rl, con)),
        WORD => process_fstore (vaddr, mem_write_value(addr, 4, rs2_val[31..0], aq, rl, con)),
        DOUBLE if sizeof(flen) >= 64 =>
            process_fstore (vaddr, mem_write_value(addr, 8, rs2_val, aq, rl, con)),
        _ => report_invalid_width(__FILE__, __LINE__, width, "floating point store"),
    };
}
}
}
}
}
}
}
}
}
}

```

B.163.7. Exceptions

This instruction may result in the following synchronous exceptions:

- `IllegalInstruction`
- `LoadAccessFault`
- `StoreAmoAccessFault`
- `StoreAmoAddressMisaligned`
- `StoreAmoPageFault`

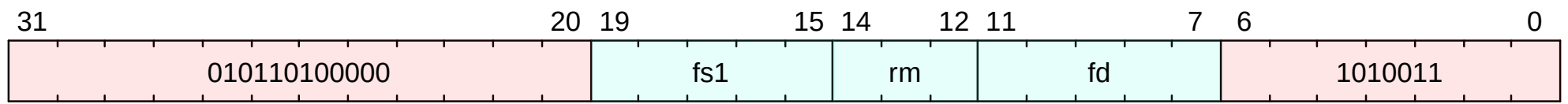
B.164. fsqrt.d

Floating-Point Square Root Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.164.1. Encoding



B.164.2. Description

The `fsqrt.d` instruction computes the square root of `fs1` and result is written in `fd`. It is defined analogously to its single-precision counterpart, but operates on double-precision operands and produces double-precision results.

B.164.3. Access

M	S	U
Always	Always	Always

B.164.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.164.5. IDL Operation

B.164.6. Exceptions

This instruction does not generate synchronous exceptions.

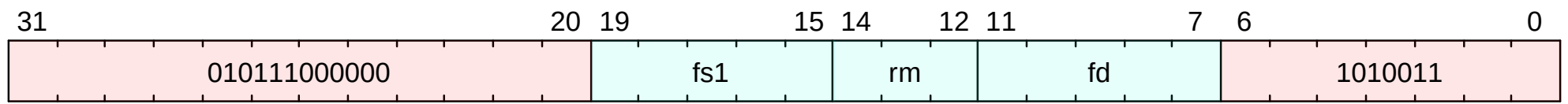
B.165. fsqrt.h

No synopsis available

This instruction is defined by:

(Zfh □ Zhinx)

B.165.1. Encoding



B.165.2. Description

No description available.

B.165.3. Access

M	S	U
Always	Always	Always

B.165.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.165.5. IDL Operation

B.165.6. Exceptions

This instruction does not generate synchronous exceptions.

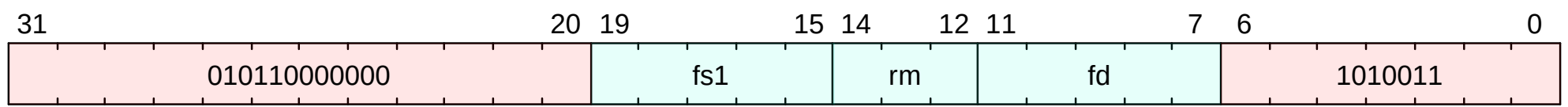
B.166. fsqrt.s

Floating-Point Square Root Single-Precision

This instruction is defined by:

F

B.166.1. Encoding



B.166.2. Description

The `fsqrt.s` instruction computes the square root of `fs1` and writes the result is written to `fd`.

B.166.3. Access

M	S	U
Always	Always	Always

B.166.4. Decode Variables

```
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.166.5. IDL Operation

B.166.6. Sail Operation

```
{
  assert(sizeof(xlen) >= 64);
  let rs1_val_LU = X(rs1)[63..0];
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_S) = riscv_ui64ToF32 (rm_3b, rs1_val_LU);

      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_S;
      RETIRE_SUCCESS
    }
  }
}
```

B.166.7. Exceptions

This instruction does not generate synchronous exceptions.

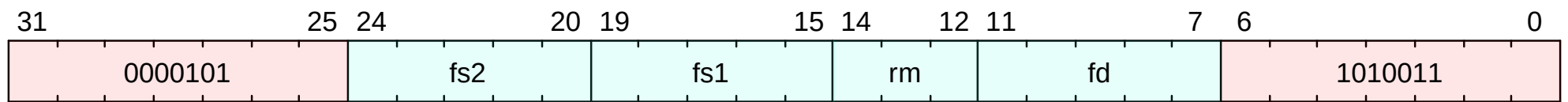
B.167. fsub.d

Floating-Point Subtract Double-Precision

This instruction is defined by:

(D $\square$ Zdinx)

B.167.1. Encoding



B.167.2. Description

The `fsub.d` instruction is analogous to `fsub.s` and performs double-precision floating-point subtraction between `fs1` and `fs2` and writes the final result to `fd`.

B.167.3. Access

M	S	U
Always	Always	Always

B.167.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.167.5. IDL Operation

B.167.6. Exceptions

This instruction does not generate synchronous exceptions.

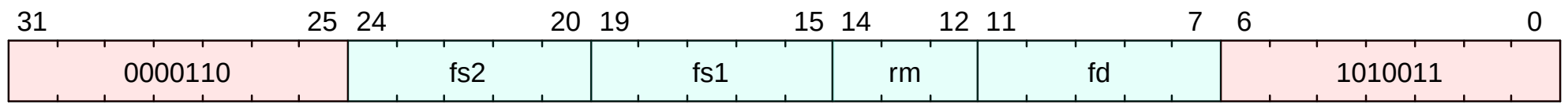
B.168. fsub.h

No synopsis available

This instruction is defined by:

(Zfh ☐ Zhinx)

B.168.1. Encoding



B.168.2. Description

No description available.

B.168.3. Access

M	S	U
Always	Always	Always

B.168.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.168.5. IDL Operation

B.168.6. Exceptions

This instruction does not generate synchronous exceptions.

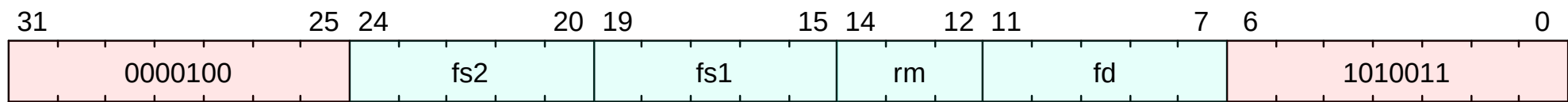
B.169. fsub.s

Floating-Point Subtract Single-Precision

This instruction is defined by:

F

B.169.1. Encoding



B.169.2. Description

The `fsub.s` instruction performs the single-precision floating-point subtraction of `fs2` from `fs1` and writes the result in `fd`.

B.169.3. Access

M	S	U
Always	Always	Always

B.169.4. Decode Variables

```
Bits<5> fs2 = $encoding[24:20];
Bits<5> fs1 = $encoding[19:15];
Bits<3> rm = $encoding[14:12];
Bits<5> fd = $encoding[11:7];
```

B.169.5. IDL Operation

```
check_f_ok($encoding);
RoundingMode mode = rm_to_mode(rm, $encoding);
f[fd] = f32_sub(f[fs1], f[fs2], mode);
```

B.169.6. Sail Operation

```
{
  let rs1_val_32b = F_or_X_S(rs1);
  let rs2_val_32b = F_or_X_S(rs2);
  match (select_instr_or_fcsr_rm (rm)) {
    None() => { handle_illegal(); RETIRE_FAIL },
    Some(rm') => {
      let rm_3b = encdec_rounding_mode(rm');
      let (fflags, rd_val_32b) : (bits(5), bits(32)) = match op {
        FADD_S  => riscv_f32Add (rm_3b, rs1_val_32b, rs2_val_32b),
        FSUB_S  => riscv_f32Sub (rm_3b, rs1_val_32b, rs2_val_32b),
        FMUL_S  => riscv_f32Mul (rm_3b, rs1_val_32b, rs2_val_32b),
        FDIV_S  => riscv_f32Div (rm_3b, rs1_val_32b, rs2_val_32b)
      };
      accrue_fflags(fflags);
      F_or_X_S(rd) = rd_val_32b;
      RETIRE_SUCCESS
    }
  }
}
```

B.169.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

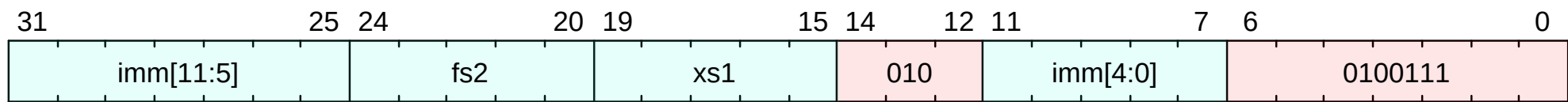
B.170. fsw

Floating-Point Store Single-Precision

This instruction is defined by:

F

B.170.1. Encoding



B.170.2. Description

The `fsw` instruction stores a single-precision floating-point value in `fs2` to memory at address `xs1 + imm`. It does not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

B.170.3. Access

M	S	U
Always	Always	Always

B.170.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> fs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.170.5. IDL Operation

```
check_f_ok($encoding);
XReg virtual_address = X[xs1] + $signed(imm);
write_memory<32>(virtual_address, f[fs2][31:0], $encoding);
```

B.170.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  let (aq, rl, con) = (false, false, false);
  /* Get the address, X(rs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(rs1, offset, Write(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Write(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(addr, _) => {
          let eares : MemoryOpResult(unit) = match width {
            BYTE => MemValue () /* bogus placeholder for illegal size */,
            HALF => mem_write_ea(addr, 2, aq, rl, false),
            WORD => mem_write_ea(addr, 4, aq, rl, false),
            DOUBLE => mem_write_ea(addr, 8, aq, rl, false)
          };
          match (eares) {
            MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
            MemValue(_) => {
              let rs2_val = F(rs2);
              match (width) {
                BYTE => { handle_illegal(); RETIRE_FAIL },
                HALF => process_fstore (vaddr, mem_write_value(addr, 2, rs2_val[15..0], aq, rl, con)),
                WORD => process_fstore (vaddr, mem_write_value(addr, 4, rs2_val[31..0], aq, rl, con)),
                DOUBLE if sizeof(flen) >= 64 =>
                  process_fstore (vaddr, mem_write_value(addr, 8, rs2_val, aq, rl, con)),
                _ => report_invalid_width(__FILE__, __LINE__, width, "floating point store"),
              };
            }
          }
        }
      }
  }
};
```

```
    }  
  }  
}
```

B.170.7. Exceptions

This instruction may result in the following synchronous exceptions:

- `IllegalInstruction`
- `LoadAccessFault`
- `StoreAmoAccessFault`
- `StoreAmoAddressMisaligned`
- `StoreAmoPageFault`

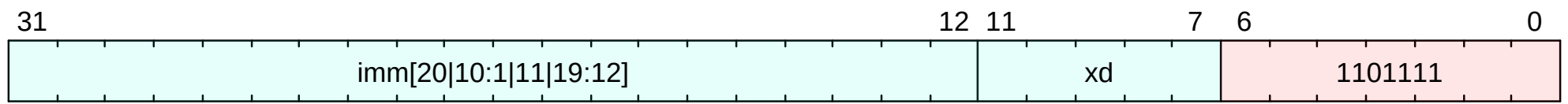
B.171. jal

Jump and link

This instruction is defined by:

I

B.171.1. Encoding



B.171.2. Description

Jump to a PC-relative offset and store the return address in xd.

B.171.3. Access

M	S	U
Always	Always	Always

B.171.4. Decode Variables

```
signed Bits<21> imm = sext({$encoding[31], $encoding[19:12], $encoding[20], $encoding[30:21], 1'd0});
Bits<5> xd = $encoding[11:7];
```

B.171.5. IDL Operation

```
XReg return_addr = $pc + 4;
X[xd] = return_addr;
jump_halfword($pc + $signed(imm));
```

B.171.6. Sail Operation

```
{
  let t : xlenbits = PC + sign_extend(imm);
  /* Extensions get the first checks on the prospective target address. */
  match ext_control_check_pc(t) {
    Ext_ControlAddr_Error(e) => {
      ext_handle_control_check_error(e);
      RETIRE_FAIL
    },
    Ext_ControlAddr_OK(target) => {
      /* Perform standaxd alignment check */
      if bit_to_bool(target[1]) & not(extension("C"))
      then {
        handle_mem_exception(target, E_Fetch_Addr_Align());
        RETIRE_FAIL
      } else {
        X(xd) = get_next_pc();
        set_next_pc(target);
        RETIRE_SUCCESS
      }
    }
  }
}
```

B.171.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

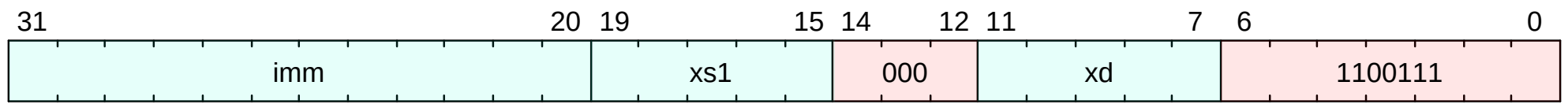
B.172. jalr

Jump and link register

This instruction is defined by:

I

B.172.1. Encoding



B.172.2. Description

Jump to an address formed by adding xs1 to a signed offset then clearing the least significant bit, and store the return address in xd.

B.172.3. Access

M	S	U
Always	Always	Always

B.172.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.172.5. IDL Operation

```
XReg addr = (X[xs1] + $signed(imm)) & ~MXLEN'1;
XReg returnaddr;
returnaddr = $pc + 4;
X[xd] = returnaddr;
jump(addr);
```

B.172.6. Sail Operation

```
{
/* For the sequential model, the memory-model definition doesn't work directly
 * if xs1 = xd. We would effectively have to keep a regfile for reads and another for
 * writes, and swap on instruction completion. This could perhaps be optimized in
 * some manner, but for now, we just keep a reoxdered definition to improve simulator
 * performance.
 */
let t : xlenbits = X(xs1) + sign_extend(imm);
/* Extensions get the first checks on the prospective target address. */
match ext_control_check_addr(t) {
  Ext_ControlAddr_Error(e) => {
    ext_handle_control_check_error(e);
    RETIRE_FAIL
  },
  Ext_ControlAddr_OK(addr) => {
    let target = [addr with 0 = bitzero]; /* clear addr[0] */
    if bit_to_bool(target[1]) & not(extension("C")) then {
      handle_mem_exception(target, E_Fetch_Addr_Align());
      RETIRE_FAIL
    } else {
      X(xd) = get_next_pc();
      set_next_pc(target);
      RETIRE_SUCCESS
    }
  }
}
}
```

B.172.7. Exceptions

This instruction may result in the following synchronous exceptions:

- InstructionAddressMisaligned

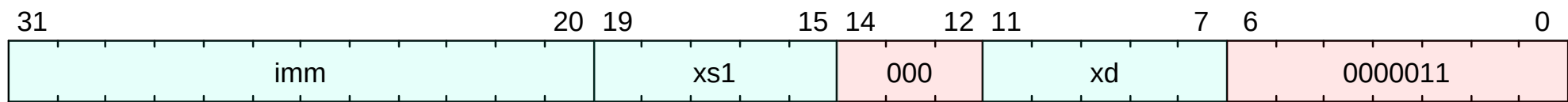
B.173. lb

Load byte

This instruction is defined by:

I

B.173.1. Encoding



B.173.2. Description

Load 8 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset. Sign extend the result.

B.173.3. Access

M	S	U
Always	Always	Always

B.173.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.173.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
X[xd] = sext(read_memory<8>(virtual_address, $encoding), 8);
```

B.173.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.173.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault

- LoadAddressMisaligned
- LoadPageFault

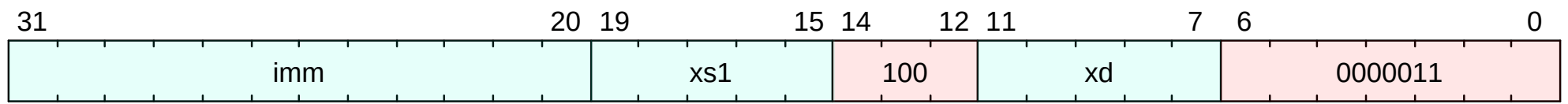
B.174. lbu

Load byte unsigned

This instruction is defined by:

I

B.174.1. Encoding



B.174.2. Description

Load 8 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset. Zero extend the result.

B.174.3. Access

M	S	U
Always	Always	Always

B.174.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.174.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
X[xd] = read_memory<8>(virtual_address, $encoding);
```

B.174.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.174.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault

- LoadAddressMisaligned
- LoadPageFault

B.175. ld

Load doubleword

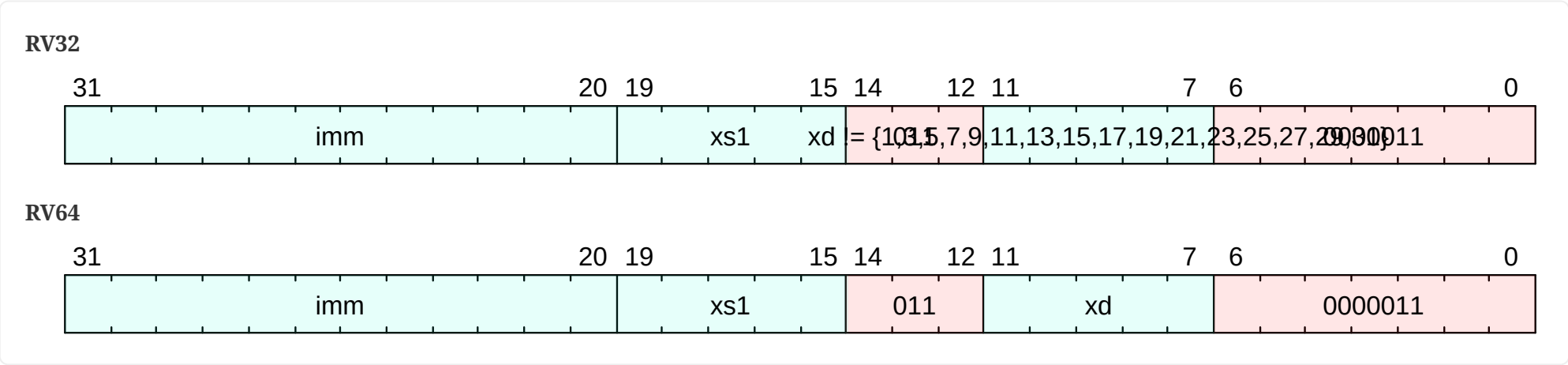
This instruction is defined by:

(I || Zilsd)

B.175.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.175.2. Description

For RV64, load 64 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset.

<% if ext?(:Zilsd) %> For RV32, Loads a 64-bit value into registers xd and xd+1. The effective address is obtained by adding register xs1 to the sign-extended 12-bit offset. <% end %>

B.175.3. Access

M	S	U
Always	Always	Always

B.175.4. Decode Variables

RV32

Bits<12> imm = \$encoding[31:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

RV64

Bits<12> imm = \$encoding[31:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

B.175.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
if (xlen() == 32) {
  if (implemented?(ExtensionName::Zilsd)) {
    Bits<64> data = read_memory<64>(virtual_address, $encoding);
    X[xd] = data[31:0];
    X[xd + 1] = data[63:32];
  } else {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else {
  X[xd] = read_memory<64>(virtual_address, $encoding);
}
```


B.175.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.175.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- LoadAddressMisaligned
- LoadPageFault

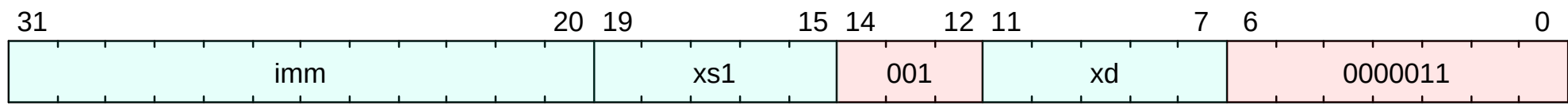
B.176. lh

Load halfword

This instruction is defined by:

I

B.176.1. Encoding



B.176.2. Description

Load 16 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset. Sign extend the result.

B.176.3. Access

M	S	U
Always	Always	Always

B.176.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.176.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
X[xd] = sext(read_memory<16>(virtual_address, $encoding), 16);
```

B.176.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.176.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault

- LoadAddressMisaligned
- LoadPageFault

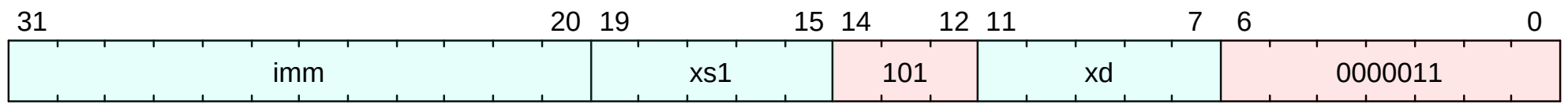
B.177. lhu

Load halfword unsigned

This instruction is defined by:

I

B.177.1. Encoding



B.177.2. Description

Load 16 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset. Zero extend the result.

B.177.3. Access

M	S	U
Always	Always	Always

B.177.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.177.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
X[xd] = read_memory<16>(virtual_address, $encoding);
```

B.177.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.177.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault

- LoadAddressMisaligned
- LoadPageFault

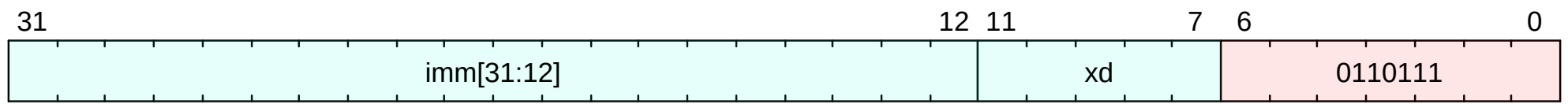
B.178. lui

Load upper immediate

This instruction is defined by:

I

B.178.1. Encoding



B.178.2. Description

Load the zero-extended imm into xd.

B.178.3. Access

M	S	U
Always	Always	Always

B.178.4. Decode Variables

```
Bits<32> imm = {$encoding[31:12], 12'd0};
Bits<5> xd = $encoding[11:7];
```

B.178.5. IDL Operation

```
X[xd] = $signed(imm);
```

B.178.6. Sail Operation

```
{
  let off : xlenbits = sign_extend(imm @ 0x000);
  let ret : xlenbits = match op {
    RISC_V_LUI    => off,
    RISC_V_AUIPC => get_arch_pc() + off
  };
  X(xd) = ret;
  RETIRE_SUCCESS
}
```

B.178.7. Exceptions

This instruction does not generate synchronous exceptions.

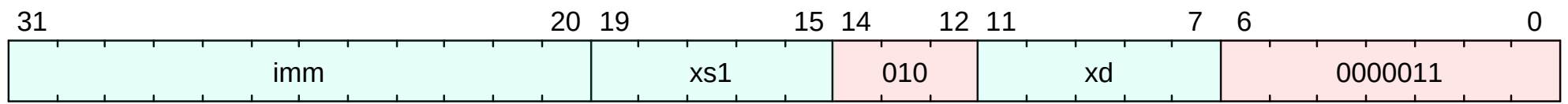
B.179. lw

Load word

This instruction is defined by:

I

B.179.1. Encoding



B.179.2. Description

Load 32 bits of data into register **xd** from an address formed by adding **xs1** to a signed offset. Sign extend the result.

B.179.3. Access

M	S	U
Always	Always	Always

B.179.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.179.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
X[xd] = sext(read_memory<32>(virtual_address, $encoding), 32);
```

B.179.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Read(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_Load_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Read(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) =>
          match (width) {
            BYTE =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 1, aq, rl, false), is_unsigned),
            HALF =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 2, aq, rl, false), is_unsigned),
            WORD =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 4, aq, rl, false), is_unsigned),
            DOUBLE if sizeof(xlen) >= 64 =>
              process_load(xd, vaddr, mem_read(Read(Data), paddr, 8, aq, rl, false), is_unsigned),
            _ => report_invalid_width(__FILE__, __LINE__, width, "load")
          }
      }
  }
}
```

B.179.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault

- LoadAddressMisaligned
- LoadPageFault

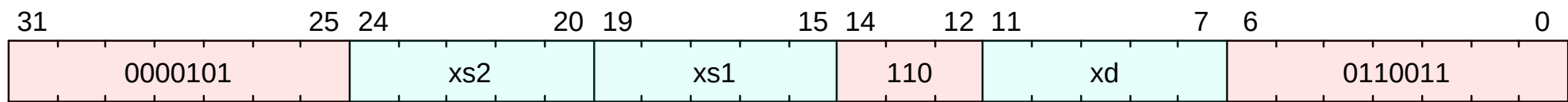
B.180. max

Maximum

This instruction is defined by:

Zbb

B.180.1. Encoding



B.180.2. Description

Returns the larger of two signed integers.



Software Hint

Calculating the absolute value of a signed integer can be performed using the following sequence: `neg rD,rS` followed by ``max rD,rS,rD`. When using this common sequence, it is suggested that they are scheduled with no intervening instructions so that implementations that are so optimized can fuse them together.

B.180.3. Access

M	S	U
Always	Always	Always

B.180.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.180.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = ($signed(X[xs1]) > $signed(X[xs2])) ? X[xs1] : X[xs2];
```

B.180.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
      then rs1_val <<< rs2_val[4..0]
      else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
      then rs1_val >>> rs2_val[4..0]
      else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.180.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

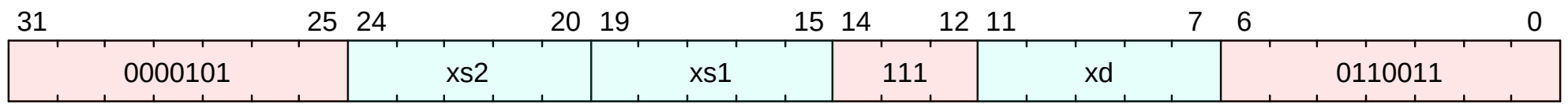
B.181. maxu

Unsigned maximum

This instruction is defined by:

Zbb

B.181.1. Encoding



B.181.2. Description

Returns the larger of two unsigned integers.

B.181.3. Access

M	S	U
Always	Always	Always

B.181.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.181.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = (X[xs1] > X[xs2]) ? X[xs1] : X[xs2];
```

B.181.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.181.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

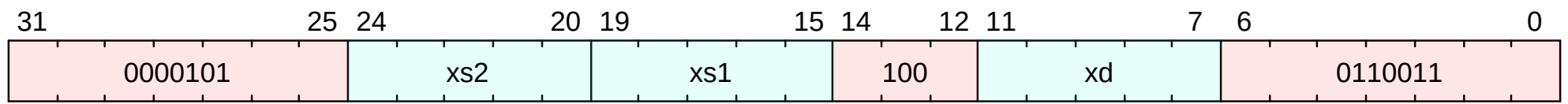
B.182. min

Minimum

This instruction is defined by:

Zbb

B.182.1. Encoding



B.182.2. Description

Returns the smaller of two signed integers.

B.182.3. Access

M	S	U
Always	Always	Always

B.182.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.182.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = ($signed(X[xs1]) < $signed(X[xs2])) ? X[xs1] : X[xs2];
```

B.182.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
      then rs1_val <<< rs2_val[4..0]
      else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
      then rs1_val >>> rs2_val[4..0]
      else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.182.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

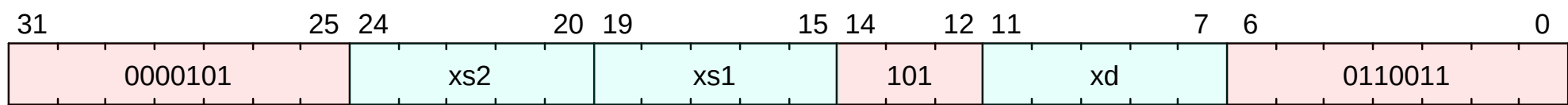
B.183. minu

Unsigned minimum

This instruction is defined by:

Zbb

B.183.1. Encoding



B.183.2. Description

Returns the smaller of two unsigned integers.

B.183.3. Access

M	S	U
Always	Always	Always

B.183.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.183.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = (X[xs1] < X[xs2]) ? X[xs1] : X[xs2];
```

B.183.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.183.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

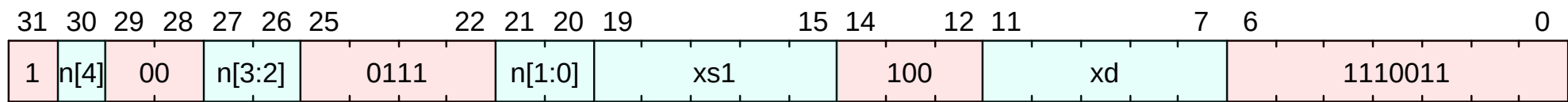
B.184. mop.r.n

May-be-operation (1 source register)

This instruction is defined by:

Zimop

B.184.1. Encoding



B.184.2. Description

Unless redefined by another extension, this instructions simply writes 0 to X[xd]. The encoding allows future extensions to define them to read X[xs1], as well as write X[xd].

B.184.3. Access

M	S	U
Always	Always	Always

B.184.4. Decode Variables

```
Bits<5> n = {$encoding[30], $encoding[27:26], $encoding[21:20]};
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.184.5. IDL Operation

```
X[xd] = 0;
```

B.184.6. Exceptions

This instruction does not generate synchronous exceptions.

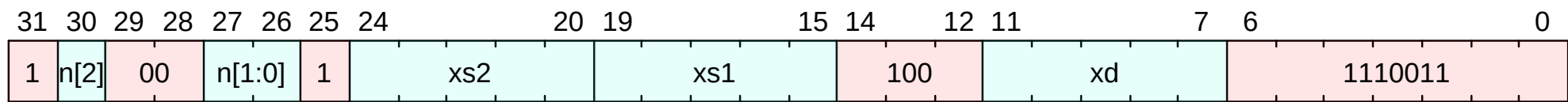
B.185. mop.rr.n

May-be-operation (2 source registers)

This instruction is defined by:

Zimop

B.185.1. Encoding



B.185.2. Description

The Zimop extension defines 8 MOP instructions named MOP.RR.n, where n is an integer between 0 and 7, inclusive. Unless redefined by another extension, these instructions simply write 0 to X[xd]. Their encoding allows future extensions to define them to read X[xs1] and X[xs2], as well as write X[xd].

B.185.3. Access

M	S	U
Always	Always	Always

B.185.4. Decode Variables

```
Bits<3> n = {$encoding[30], $encoding[27:26]};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.185.5. IDL Operation

```
X[xd] = 0;
```

B.185.6. Exceptions

This instruction does not generate synchronous exceptions.

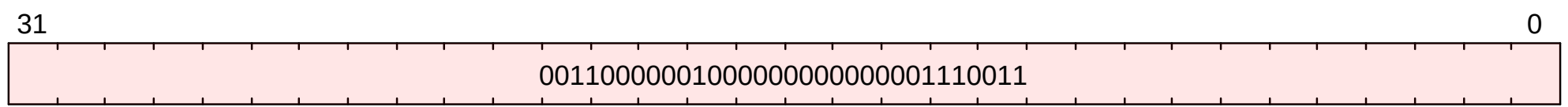
B.186. mret

Machine-mode Return from Trap

This instruction is defined by:

Sm

B.186.1. Encoding



B.186.2. Description

Return from machine mode after handling a trap.

B.186.3. Access

M	S	U
Always	Never	Never

B.186.4. Decode Variables

B.186.5. IDL Operation

```
if (CSR[mstatus].MPP != 2'b11) {
    if (implemented?(ExtensionName::U)) {
        CSR[mstatus].MPRV = 0;
    }
}
if (implemented?(ExtensionName::Smdbltrp)) {
    if (xlen() == 64) {
        CSR[mstatus].MDT = 1'b0;
    } else {
        CSR[mstatush].MDT = 1'b0;
    }
}
CSR[mstatus].MIE = CSR[mstatus].MPIE;
CSR[mstatus].MPIE = 1;
if (CSR[mstatus].MPP == 2'b00) {
    set_mode(PrivilegeMode::U);
} else if (CSR[mstatus].MPP == 2'b01) {
    set_mode(PrivilegeMode::S);
} else if (CSR[mstatus].MPP == 2'b11) {
    set_mode(PrivilegeMode::M);
}
CSR[mstatus].MPP = implemented?(ExtensionName::U) ? 2'b00 : 2'b11;
$pc = $bits(CSR[CSR[mepc]]);
```

B.186.6. Sail Operation

```
{
    if cur_privilege != Machine
    then { handle_illegal(); RETIRE_FAIL }
    else if not(ext_check_xret_priv (Machine))
    then { ext_fail_xret_priv(); RETIRE_FAIL }
    else {
        set_next_pc(exception_handler(cur_privilege, CTL_MRET(), PC));
        RETIRE_SUCCESS
    }
}
```


B.186.7. Exceptions

This instruction does not generate synchronous exceptions.

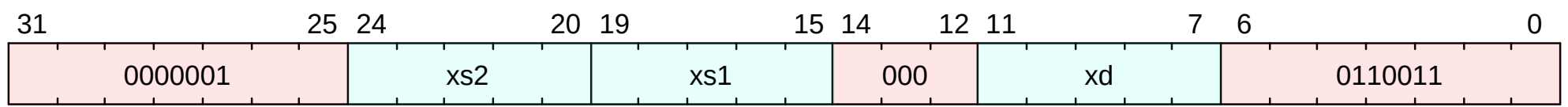
B.187. mul

Signed multiply

This instruction is defined by:

([M](#) || [Zmmul](#))

B.187.1. Encoding



B.187.2. Description

MUL performs an XLEN-bitxXLEN-bit multiplication of **xs1** by **xs2** and places the lower XLEN bits in the destination register. Any overflow is thrown away.



If both the high and low bits of the same product are required, then the recommended code sequence is: MULH[[S]U] xdh, xs1, xs2; MUL xdl, xs1, xs2 (source register specifiers must be in same order and xdh cannot be the same as xs1 or xs2). Microarchitectures can then fuse these into a single multiply operation instead of performing two separate multiplies.

B.187.3. Access

M	S	U
Always	Always	Always

B.187.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.187.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg src1 = X[xs1];
XReg src2 = X[xs2];
X[xd] = (src1 * src2)[MXLEN - 1:0];
```

B.187.6. Sail Operation

```
{
  if extension("M") | haveZmmul() then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if signed1 then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if signed2 then signed(rs2_val) else unsigned(rs2_val);
    let result_wide = to_bits(2 * sizeof(xlen), rs1_int * rs2_int);
    let result = if    high
                  then result_wide[(2 * sizeof(xlen) - 1) .. sizeof(xlen)]
                  else result_wide[(sizeof(xlen) - 1) .. 0];
    X(rd) = result;
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```

B.187.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

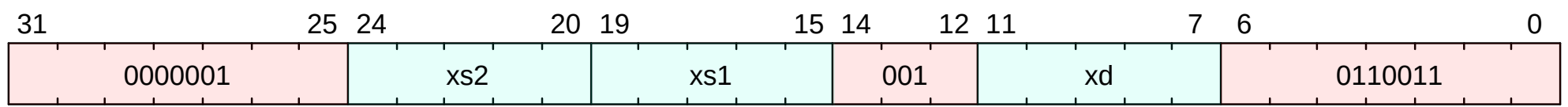
B.188. mulh

Signed multiply high

This instruction is defined by:

(M || Zmmul)

B.188.1. Encoding



B.188.2. Description

Multiply the signed values in xs1 to xs2, and store the upper half of the result in xd. The lower half is thrown away.

If both the upper and lower halves are needed, it suggested to use the sequence:

```
mulh xdh, xs1, xs2
mul  xdl, xs1, xs2
---
```

Microarchitectures may look for that sequence and fuse the operations.

B.188.3. Access

M	S	U
Always	Always	Always

B.188.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.188.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
Bits<1> xs1_sign_bit = X[xs1][xlen() - 1];
Bits<MXLEN `* 2> src1 = {{xlen(){xs1_sign_bit}}, X[xs1]};
Bits<1> xs2_sign_bit = X[xs2][xlen() - 1];
Bits<MXLEN `* 2> src2 = {{xlen(){xs2_sign_bit}}, X[xs2]};
X[xd] = (src1 * src2)[(xlen() * 8'd2) - 1:xlen()];
```

B.188.6. Sail Operation

```
{
  if extension("M") | haveZmmul() then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if signed1 then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if signed2 then signed(rs2_val) else unsigned(rs2_val);
    let result_wide = to_bits(2 * sizeof(xlen), rs1_int * rs2_int);
    let result = if  high
                  then result_wide[(2 * sizeof(xlen) - 1) .. sizeof(xlen)]
                  else result_wide[sizeof(xlen) - 1) .. 0];
    X(rd) = result;
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```

}

B.188.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

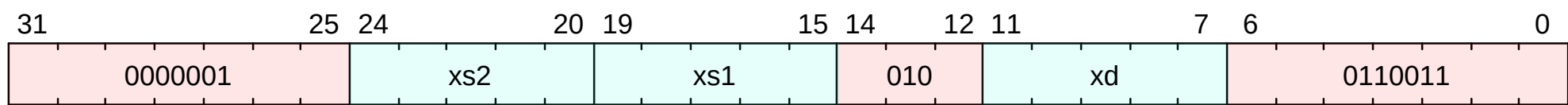
B.189. mulhsu

Signed/unsigned multiply high

This instruction is defined by:

([M](#) || [Zmmul](#))

B.189.1. Encoding



B.189.2. Description

Multiply the signed value in xs1 by the unsigned value in xs2, and store the upper half of the result in xd. The lower half is thrown away.

If both the upper and lower halves are needed, it suggested to use the sequence:

```
mulhsu xdh, xs1, xs2
mul    xdl, xs1, xs2
---
```

Microarchitectures may look for that sequence and fuse the operations.

B.189.3. Access

M	S	U
Always	Always	Always

B.189.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd  = $encoding[11:7];
```

B.189.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
Bits<1> xs1_sign_bit = X[xs1][MXLEN - 1];
Bits<MXLEN * 8'd2> src1 = {{MXLEN{xs1_sign_bit}}, X[xs1]};
Bits<MXLEN * 8'd2> src2 = {{MXLEN{1'b0}}, X[xs2]};
X[xd] = (src1 * src2)[(MXLEN * 8'd2) - 1:MXLEN];
```

B.189.6. Sail Operation

```
{
  if extension("M") | haveZmmul() then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if signed1 then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if signed2 then signed(rs2_val) else unsigned(rs2_val);
    let result_wide = to_bits(2 * sizeof(xlen), rs1_int * rs2_int);
    let result = if    high
                  then result_wide[(2 * sizeof(xlen) - 1) .. sizeof(xlen)]
                  else result_wide[(sizeof(xlen) - 1) .. 0];
    X(rd) = result;
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```



```
}
```

B.189.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

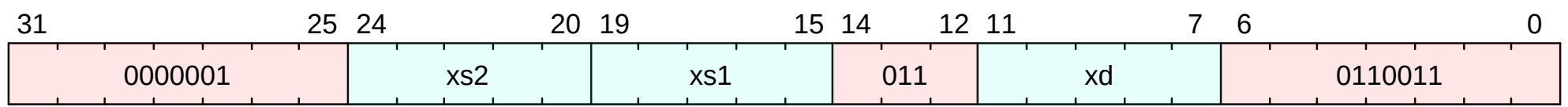
B.190. mulhu

Unsigned multiply high

This instruction is defined by:

([M](#) || [Zmmul](#))

B.190.1. Encoding



B.190.2. Description

Multiply the unsigned values in xs1 to xs2, and store the upper half of the result in xd. The lower half is thrown away.

If both the upper and lower halves are needed, it suggested to use the sequence:

```
mulhu xdh, xs1, xs2
mul    xdl, xs1, xs2
---
```

Microarchitectures may look for that sequence and fuse the operations.

B.190.3. Access

M	S	U
Always	Always	Always

B.190.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.190.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
Bits<MXLEN * 8'd2> src1 = {{MXLEN{1'b0}}, X[xs1]};
Bits<MXLEN * 8'd2> src2 = {{MXLEN{1'b0}}, X[xs2]};
X[xd] = (src1 * src2)[(MXLEN * 8'd2) - 1:MXLEN];
```

B.190.6. Sail Operation

```
{
  if extension("M") | haveZmmul() then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if signed1 then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if signed2 then signed(rs2_val) else unsigned(rs2_val);
    let result_wide = to_bits(2 * sizeof(xlen), rs1_int * rs2_int);
    let result = if    high
                  then result_wide[(2 * sizeof(xlen) - 1) .. sizeof(xlen)]
                  else result_wide[sizeof(xlen) - 1) .. 0];
    X(rd) = result;
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```


B.190.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

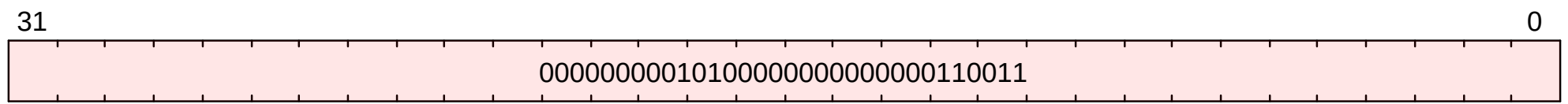
B.191. ntl.all

Non-temporal locality hint, all

This instruction is defined by:

[Zihintntl](#)

B.191.1. Encoding



B.191.2. Description

The NTL.ALL instruction indicates that the immediately subsequent instruction does not exhibit temporal locality within the capacity of any level of cache in the memory hierarchy. NTL.ALL is encoded as ADD x0, x0, x5.

B.191.3. Access

M	S	U
Always	Always	Always

B.191.4. Decode Variables

B.191.5. Exceptions

This instruction does not generate synchronous exceptions.

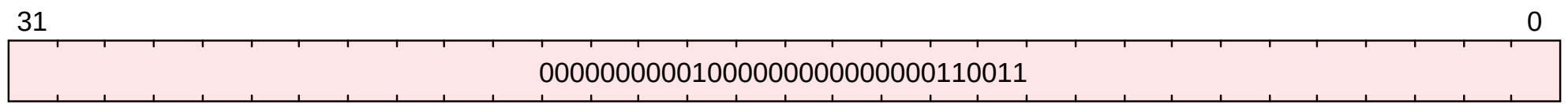
B.192. ntl.p1

Non-temporal locality hint, innermost private

This instruction is defined by:

[Zihintntl](#)

B.192.1. Encoding



B.192.2. Description

The NTL.P1 instruction indicates that the immediately subsequent instruction does not exhibit temporal locality within the capacity of the innermost level of private cache in the memory hierarchy. NTL.P1 is encoded as ADD x0, x0, x2.

B.192.3. Access

M	S	U
Always	Always	Always

B.192.4. Decode Variables

B.192.5. Exceptions

This instruction does not generate synchronous exceptions.

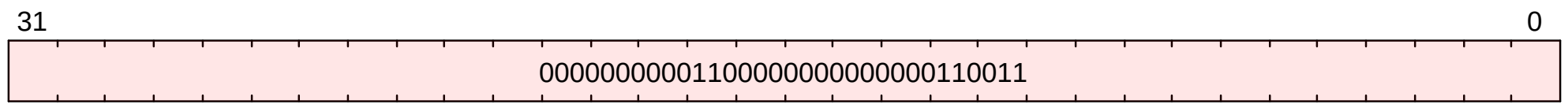
B.193. ntl.pall

Non-temporal locality hint, all private

This instruction is defined by:

[Zihintntl](#)

B.193.1. Encoding



B.193.2. Description

The NTL.PALL instruction indicates that the immediately subsequent instruction does not exhibit temporal locality within the capacity of any level of private cache in the memory hierarchy. NTL.PALL is encoded as ADD x0, x0, x3.

B.193.3. Access

M	S	U
Always	Always	Always

B.193.4. Decode Variables

B.193.5. Exceptions

This instruction does not generate synchronous exceptions.

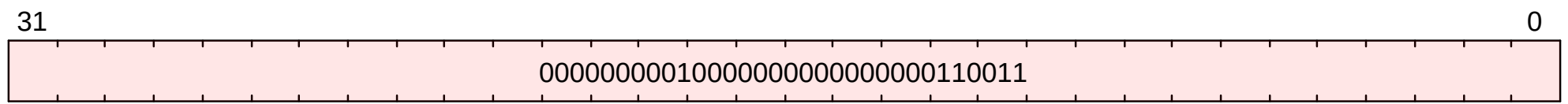
B.194. ntl.s1

Non-temporal locality hint, innermost shared

This instruction is defined by:

[Zihintntl](#)

B.194.1. Encoding



B.194.2. Description

The NTL.S1 instruction indicates that the immediately subsequent instruction does not exhibit temporal locality within the capacity of the innermost level of shared cache in the memory hierarchy. NTL.S1 is encoded as ADD x0, x0, x4.

B.194.3. Access

M	S	U
Always	Always	Always

B.194.4. Decode Variables

B.194.5. Exceptions

This instruction does not generate synchronous exceptions.

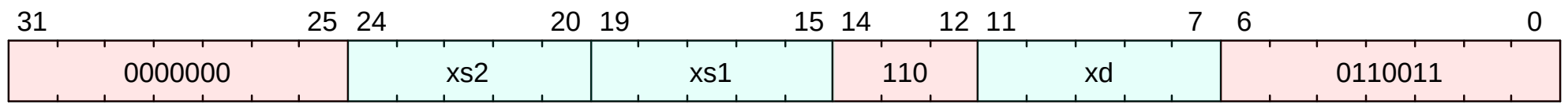
B.195. or

Or

This instruction is defined by:

I

B.195.1. Encoding



B.195.2. Description

Or xs1 with xs2, and store the result in xd

B.195.3. Access

M	S	U
Always	Always	Always

B.195.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.195.5. IDL Operation

```
X[xd] = X[xs1] | X[xs2];
```

B.195.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD => xs1_val + xs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND => xs1_val & xs2_val,
    RISCV_OR  => xs1_val | xs2_val,
    RISCV_XOR => xs1_val ^ xs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB => xs1_val - xs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.195.7. Exceptions

This instruction does not generate synchronous exceptions.

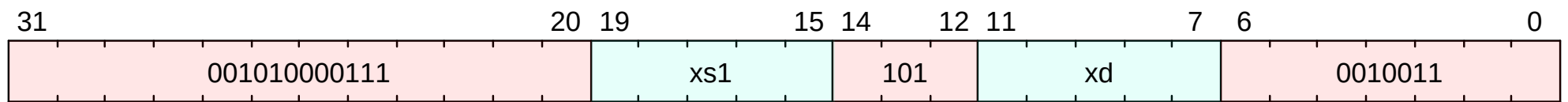
B.196. orc.b

Bitware OR-combine, byte granule

This instruction is defined by:

Zbb

B.196.1. Encoding



B.196.2. Description

Combines the bits within each byte using bitwise logical OR. This sets the bits of each byte in the result xd to all zeros if no bit within the respective byte of xs1 is set, or to all ones if any bit within the respective byte of xs1 is set.

B.196.3. Access

M	S	U
Always	Always	Always

B.196.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.196.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg input = X[xs1];
XReg output = 0;
for (U32 i = 0; i < (xlen() - 8); i = i + 8) {
    output[(i + 7):i] = (input[(i + 7):i] == 0) ? 8'd0 : ~8'd0;
}
X[xd] = output;
```

B.196.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    result : xlenbits = zeros();
    foreach (i from 0 to (sizeof(xlen) - 8) by 8)
        result[(i + 7) .. i] = if rs1_val[(i + 7) .. i] == zeros()
                                then 0x00
                                else 0xFF;

    X(rd) = result;
    RETIRE_SUCCESS
}
```

B.196.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

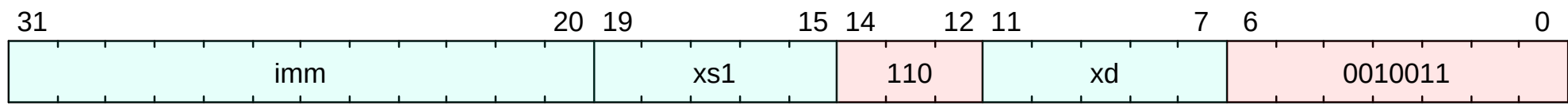
B.197. ori

Or immediate

This instruction is defined by:

I

B.197.1. Encoding



B.197.2. Description

Or an immediate to the value in xs1, and store the result in xd

B.197.3. Access

M	S	U
Always	Always	Always

B.197.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.197.5. IDL Operation

```
X[xd] = X[xs1] | $signed(imm);
```

B.197.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.197.7. Exceptions

This instruction does not generate synchronous exceptions.

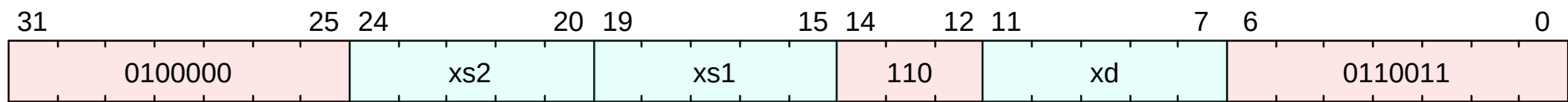
B.198. orn

OR with inverted operand

This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.198.1. Encoding



B.198.2. Description

Performs the bitwise logical OR operation between xs1 and the bitwise inversion of xs2.

B.198.3. Access

M	S	U
Always	Always	Always

B.198.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.198.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs1] | ~X[xs2];
```

B.198.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.198.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

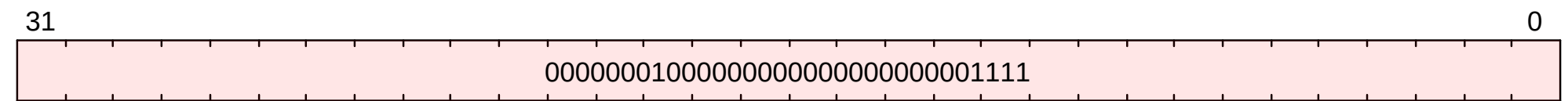
B.199. pause

Pause hint

This instruction is defined by:

Zihintpause

B.199.1. Encoding



B.199.2. Description

The PAUSE instruction is a HINT that indicates the current hart's rate of instruction retirement should be temporarily reduced or paused. The duration of its effect must be bounded and may be zero.



Software can use the PAUSE instruction to reduce energy consumption while executing spin-wait code sequences. Multithreaded cores might temporarily relinquish execution resources to other harts when PAUSE is executed. It is recommended that a PAUSE instruction generally be included in the code sequence for a spin-wait loop.

A future extension might add primitives similar to the x86 `MONITOR/MWAIT` instructions, which provide a more efficient mechanism to wait on writes to a specific memory location. However, these instructions would not supplant `PAUSE`. `PAUSE` is more appropriate when polling for non-memory events, when polling for multiple events, or when software does not know precisely what events it is polling for.

The duration of a PAUSE instruction's effect may vary significantly within and among implementations. In typical implementations this duration should be much less than the time to perform a context switch, probably more on the rough order of an on-chip cache miss latency or a cacheless access to main memory.

A series of PAUSE instructions can be used to create a cumulative delay loosely proportional to the number of PAUSE instructions. In spin-wait loops in portable code, however, only one PAUSE instruction should be used before re-evaluating loop conditions, else the hart might stall longer than optimal on some implementations, degrading system performance.

PAUSE is encoded as a FENCE instruction with *pred*=W, *succ*=0, *fm*=0, *xd*=x0, and *xs1*=x0.



PAUSE is encoded as a hint within the FENCE opcode because some implementations are expected to deliberately stall the PAUSE instruction until outstanding memory transactions have completed. Because the successor set is null, however, PAUSE does not *mandate* any particular memory ordering—hence, it truly is a HINT.

Like other FENCE instructions, PAUSE cannot be used within LR/SC sequences without voiding the forward-progress guarantee.

The choice of a predecessor set of W is arbitrary, since the successor set is null. Other HINTs similar to PAUSE might be encoded with other predecessor sets.

B.199.3. Access

M	S	U
Always	Always	Always

B.199.4. Decode Variables

B.199.5. IDL Operation

B.199.6. Exceptions

This instruction does not generate synchronous exceptions.

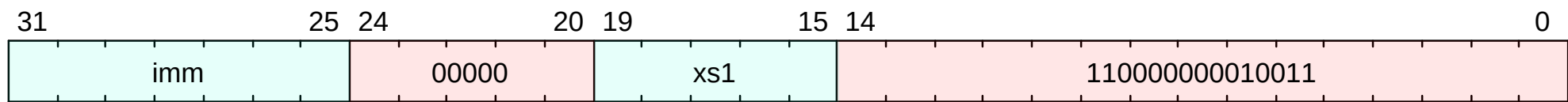
B.200. prefetch.i

Cache block prefetch for instruction fetch

This instruction is defined by:

Zicbop

B.200.1. Encoding



B.200.2. Description

A prefetch.i instruction indicates to hardware that the cache block whose effective address is the sum of the base address specified in xs1 and the sign-extended offset encoded in imm[11:0], where imm[4:0] equals 0b00000, is likely to be accessed by an instruction fetch in the near future.

B.200.3. Access

M	S	U
Always	Always	Always

B.200.4. Decode Variables

```
Bits<7> imm = $encoding[31:25];
Bits<5> xs1 = $encoding[19:15];
```

B.200.5. IDL Operation

```
XReg address = X[xs1] + $signed(imm << 5);
prefetch_instruction(address);
```

B.200.6. Exceptions

This instruction does not generate synchronous exceptions.

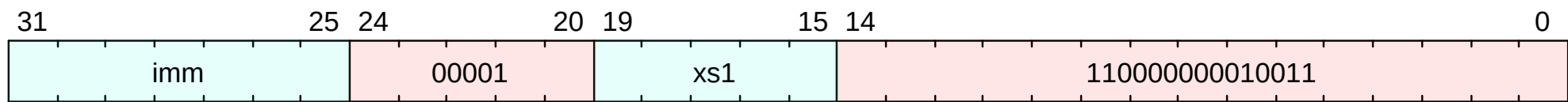
B.201. prefetch.r

Cache block prefetch for data read

This instruction is defined by:

Zicbop

B.201.1. Encoding



B.201.2. Description

A prefetch.r instruction indicates to hardware that the cache block whose effective address is the sum of the base address specified in xs1 and the sign-extended offset encoded in imm[11:0], where imm[4:0] equals 0b00000, is likely to be accessed by a data read (i.e. load) in the near future.

B.201.3. Access

M	S	U
Always	Always	Always

B.201.4. Decode Variables

```
Bits<7> imm = $encoding[31:25];
Bits<5> xs1 = $encoding[19:15];
```

B.201.5. IDL Operation

```
XReg address = X[xs1] + $signed(imm << 5);
prefetch_read(address);
```

B.201.6. Exceptions

This instruction does not generate synchronous exceptions.

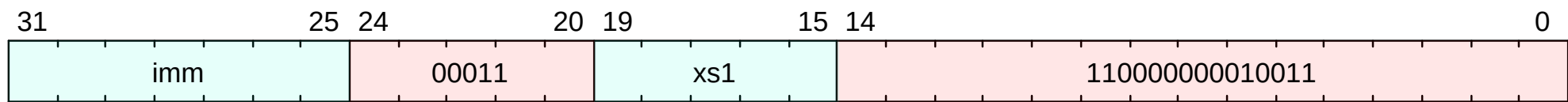
B.202. prefetch.w

Cache block prefetch for data write

This instruction is defined by:

Zicbop

B.202.1. Encoding



B.202.2. Description

A prefetch.w instruction indicates to hardware that the cache block whose effective address is the sum of the base address specified in xs1 and the sign-extended offset encoded in imm[11:0], where imm[4:0] equals 0b00000, is likely to be accessed by a data write (i.e. store) in the near future.

B.202.3. Access

M	S	U
Always	Always	Always

B.202.4. Decode Variables

```
Bits<7> imm = $encoding[31:25];
Bits<5> xs1 = $encoding[19:15];
```

B.202.5. IDL Operation

```
XReg address = X[xs1] + $signed(imm << 5);
prefetch_write(address);
```

B.202.6. Exceptions

This instruction does not generate synchronous exceptions.

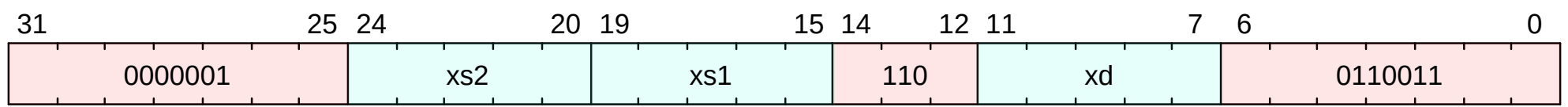
B.203. rem

Signed remainder

This instruction is defined by:

M

B.203.1. Encoding



B.203.2. Description

Calculate the remainder of signed division of xs1 by xs2, and store the result in xd.

If the value in register xs2 is zero, write the value in xs1 into xd;

If the result of the division overflows, write zero into xd;

B.203.3. Access

M	S	U
Always	Always	Always

B.203.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.203.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg src1 = X[xs1];
XReg src2 = X[xs2];
if (src2 == 0) {
    X[xd] = src1;
} else if ((src1 == {1'b1, {MXLEN - 1{1'b0}}}) && (src2 == {MXLEN{1'b1}})) {
    X[xd] = 0;
} else {
    X[xd] = $signed(src1) % $signed(src2);
}
```

B.203.6. Sail Operation

```
{
  if extension("M") then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if s then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if s then signed(rs2_val) else unsigned(rs2_val);
    let r : int = if rs2_int == 0 then rs1_int else rem_round_zero(rs1_int, rs2_int);
    /* signed overflow case returns zero naturally as required due to -1 divisor */
    X(rd) = to_bits(sizeof(xlen), r);
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```


B.203.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

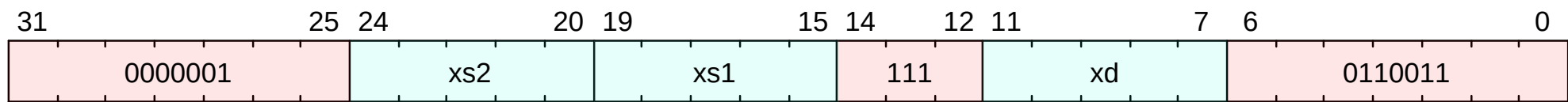
B.204. remu

Unsigned remainder

This instruction is defined by:

M

B.204.1. Encoding



B.204.2. Description

Calculate the remainder of unsigned division of xs1 by xs2, and store the result in xd.

B.204.3. Access

M	S	U
Always	Always	Always

B.204.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.204.5. IDL Operation

```
if (implemented?(ExtensionName::M) && (CSR[misa].M == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg src1 = X[xs1];
XReg src2 = X[xs2];
if (src2 == 0) {
    X[xd] = src1;
} else {
    X[xd] = src1 % src2;
}
```

B.204.6. Sail Operation

```
{
  if extension("M") then {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let rs1_int : int = if s then signed(rs1_val) else unsigned(rs1_val);
    let rs2_int : int = if s then signed(rs2_val) else unsigned(rs2_val);
    let r : int = if rs2_int == 0 then rs1_int else rem_round_zero(rs1_int, rs2_int);
    /* signed overflow case returns zero naturally as required due to -1 divisor */
    X(rd) = to_bits(sizeof(xlen), r);
    RETIRE_SUCCESS
  } else {
    handle_illegal();
    RETIRE_FAIL
  }
}
```

B.204.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.205. rev8

Byte-reverse register (RV64 encoding)

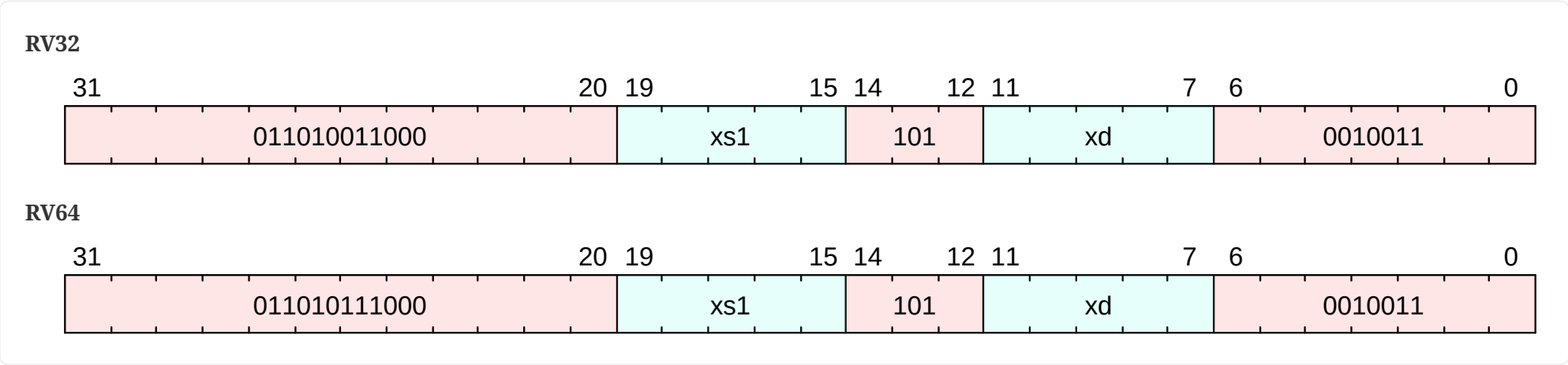
This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.205.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.205.2. Description

Reverses the order of the bytes in rs1.



The rev8 mnemonic corresponds to different instruction encodings in RV32 and RV64.



The byte-reverse operation is only available for the full register width. To emulate word-sized and halfword-sized byte-reversal, perform a `rev8 xd, xs1` followed by a `srai xd, xd, K`, where K is XLEN-32 and XLEN-16, respectively.

B.205.3. Access

M	S	U
Always	Always	Always

B.205.4. Decode Variables

RV32

Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

RV64

Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

B.205.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {  
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
}  
XReg input = X[xs1];  
XReg output = 0;  
XReg j = xlen() - 1;  
for (U32 i = 0; i < (xlen() - 8); i = i + 8) {  
  output[(i + 7):i] = input[j:(j - 7)];  
  j = j - 8;  
}  
X[xd] = output;
```

B.205.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  result : xlenbits = zeros();
  foreach (i from 0 to (sizeof(xlen) - 8) by 8)
    result[(i + 7) .. i] = rs1_val[(sizeof(xlen) - i - 1) .. (sizeof(xlen) - i - 8)];
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.205.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

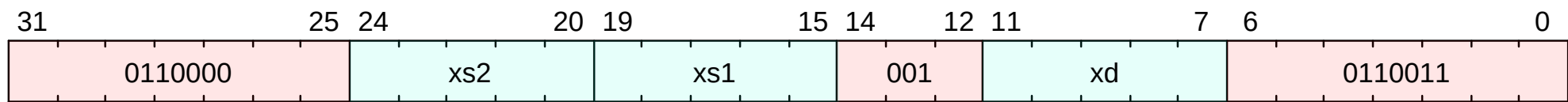
B.206. rol

Rotate left (Register)

This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.206.1. Encoding



B.206.2. Description

Performs a rotate left of xs1 by the amount in least-significant **log2(XLEN)** bits of xs2.

B.206.3. Access

M	S	U
Always	Always	Always

B.206.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.206.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg shamt = (xlen() == 32) ? X[xs2][4:0] : X[xs2][5:0];
X[xd] = (X[xs1] << shamt) | (X[xs1] >> (xlen() - shamt));
```

B.206.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.206.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

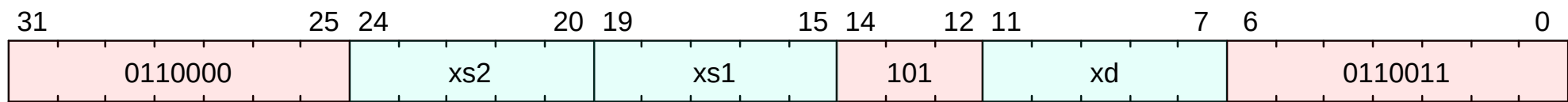
B.207. ror

Rotate right (Register)

This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.207.1. Encoding



B.207.2. Description

Performs a rotate right of xs1 by the amount in least-significant $\log_2(XLEN)$ bits of xs2.

B.207.3. Access

M	S	U
Always	Always	Always

B.207.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.207.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
XReg shamt = (xlen() == 32) ? X[xs2][4:0] : X[xs2][5:0];
X[xd] = (X[xs1] >> shamt) | (X[xs1] << (xlen() - shamt));
```

B.207.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let result : xlenbits = match op {
        RISCV_ANDN => rs1_val & ~(rs2_val),
        RISCV_ORN  => rs1_val | ~(rs2_val),
        RISCV_XNOR => ~(rs1_val ^ rs2_val),
        RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
        RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
        RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
        RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
        RISCV_ROL  => if sizeof(xlen) == 32
                        then rs1_val <<< rs2_val[4..0]
                        else rs1_val <<< rs2_val[5..0],
        RISCV_ROR  => if sizeof(xlen) == 32
                        then rs1_val >>> rs2_val[4..0]
                        else rs1_val >>> rs2_val[5..0]
    };
    X(rd) = result;
    RETIRE_SUCCESS
}
```

B.207.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

B.208. rori

Rotate right (Immediate)

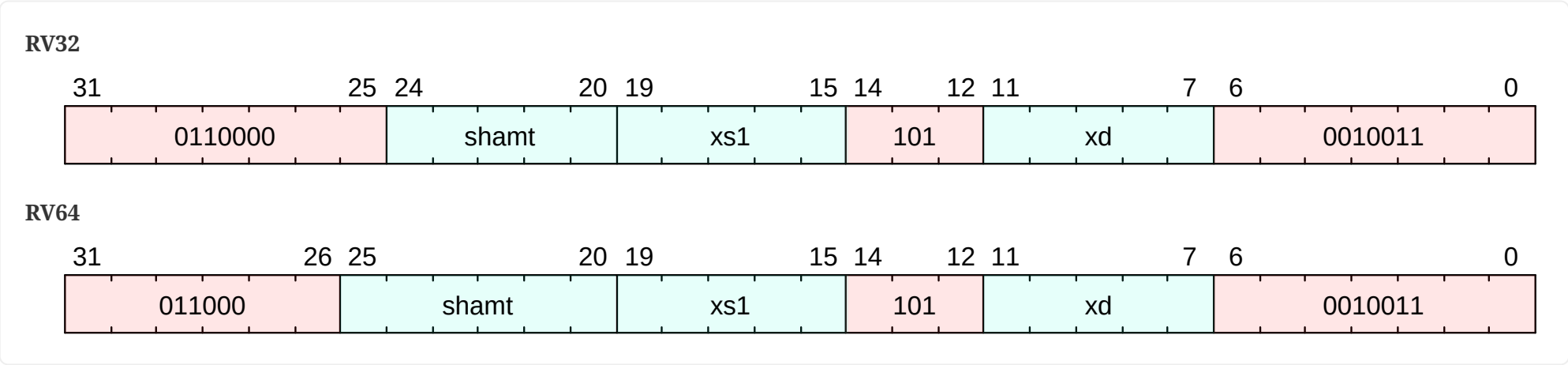
This instruction is defined by:

(Zbb || Zbkb)

B.208.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.208.2. Description

Performs a rotate right of xs1 by the amount in the least-significant log2(XLEN) bits of shamt. For RV32, the encodings corresponding to shamt[5]=1 are reserved.

B.208.3. Access

M	S	U
Always	Always	Always

B.208.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];
Bits<5> xs1 = \$encoding[19:15];
Bits<5> xd = \$encoding[11:7];

B.208.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {  
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
}  
XReg shamt = (xlen() == 32) ? shamt[4:0] : shamt[5:0];  
X[xd] = (X[xs1] >> shamt) | (X[xs1] << (xlen() - shamt));
```

B.208.6. Sail Operation

```
{  
  let rs1_val = X(rs1);  
  let result : xlenbits = if sizeof(xlen) == 32  
                           then rs1_val >>> shamt[4..0]  
                           else rs1_val >>> shamt;  
  
  X(rd) = result;  
  RETIRE_SUCCESS  
}
```

B.208.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

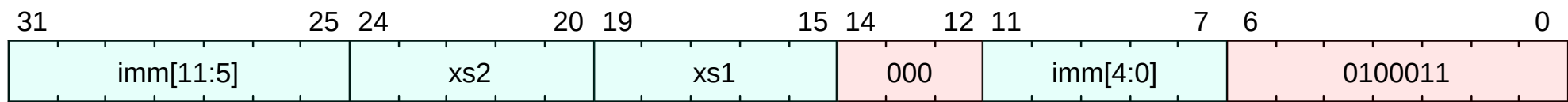
B.209. sb

Store byte

This instruction is defined by:

I

B.209.1. Encoding



B.209.2. Description

Store 8 bits of data from register **xs2** to an address formed by adding **xs1** to a signed offset.

B.209.3. Access

M	S	U
Always	Always	Always

B.209.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.209.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
write_memory<8>(virtual_address, X[xs2][7:0], $encoding);
```

B.209.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Write(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Write(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) => {
          let eares : MemoryOpResult(unit) = match width {
            BYTE => mem_write_ea(paddr, 1, aq, rl, false),
            HALF => mem_write_ea(paddr, 2, aq, rl, false),
            WORD => mem_write_ea(paddr, 4, aq, rl, false),
            DOUBLE => mem_write_ea(paddr, 8, aq, rl, false)
          };
          match (eares) {
            MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
            MemValue(_) => {
              let xs2_val = X(xs2);
              let res : MemoryOpResult(bool) = match (width) {
                BYTE => mem_write_value(paddr, 1, xs2_val[7..0], aq, rl, false),
                HALF => mem_write_value(paddr, 2, xs2_val[15..0], aq, rl, false),
                WORD => mem_write_value(paddr, 4, xs2_val[31..0], aq, rl, false),
                DOUBLE if sizeof(xlen) >= 64
                  => mem_write_value(paddr, 8, xs2_val, aq, rl, false),
                _ => report_invalid_width(__FILE__, __LINE__, width, "store"),
              };
              match (res) {
                MemValue(true) => RETIRE_SUCCESS,
                MemValue(false) => internal_error(__FILE__, __LINE__, "store got false from mem_write_value"),
              }
            }
          }
        }
      }
  }
}
```

```
MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL }  
    }  
    }  
    }  
    }  
    }  
    }
```

B.209.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

B.210. sd

Store doubleword

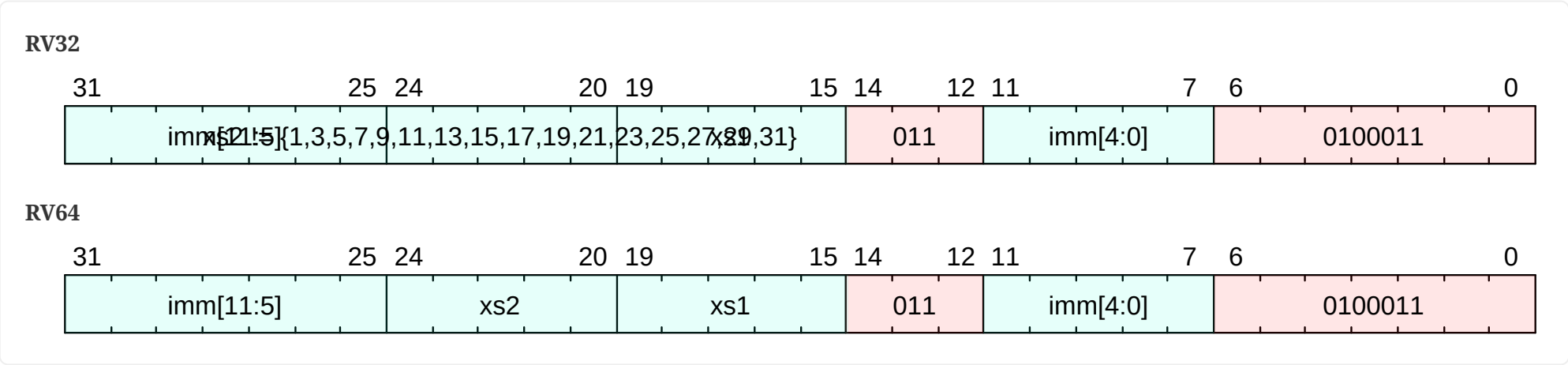
This instruction is defined by:

([I](#) || [Zil](#)[sd](#))

B.210.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.210.2. Description

For RV64, store 64 bits of data from register **xs2** to an address formed by adding **xs1** to a signed offset. <% if ext?:(Zilsd) %> For RV32, store doubleword from even/odd register pair. <% end %>

B.210.3. Access

M	S	U
Always	Always	Always

B.210.4. Decode Variables

RV32

Bits<12> imm = { \$encoding[31:25], \$encoding[11:7] };
Bits<5> xs2 = \$encoding[24:20];
Bits<5> xs1 = \$encoding[19:15];

RV64

signed Bits<12> imm = sext({ \$encoding[31:25], \$encoding[11:7] });
Bits<5> xs2 = \$encoding[24:20];
Bits<5> xs1 = \$encoding[19:15];

B.210.5. IDL Operation

```
Bits<64> data;  
XReg virtual_address = X[xs1] + $signed(imm);  
if (xlen() == 32) {  
  if (implemented?(ExtensionName::Zc1sd)) {  
    data = {X[xs2 + 1], X[xs2]};  
  } else {  
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);  
  }  
} else {  
  data = X[xs2];  
}  
write_memory<64>(virtual_address, data, $encoding);
```

B.210.6. Sail Operation

```
{  
  let offset : xlenbits = sign_extend(imm);
```

```

/* Get the address, X(xs1) + offset.
   Some extensions perform additional checks on address validity. */
match ext_data_get_addr(xs1, offset, Write(Data), width) {
  Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
  Ext_DataAddr_OK(vaddr) =>
    if check_misaligned(vaddr, width)
    then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
    else match translateAddr(vaddr, Write(Data)) {
      TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
      TR_Address(paddr, _) => {
        let eares : MemoryOpResult(unit) = match width {
          BYTE => mem_write_ea(paddr, 1, aq, rl, false),
          HALF => mem_write_ea(paddr, 2, aq, rl, false),
          WORD => mem_write_ea(paddr, 4, aq, rl, false),
          DOUBLE => mem_write_ea(paddr, 8, aq, rl, false)
        };
        match (eares) {
          MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
          MemValue(_) => {
            let xs2_val = X(xs2);
            let res : MemoryOpResult(bool) = match (width) {
              BYTE => mem_write_value(paddr, 1, xs2_val[7..0], aq, rl, false),
              HALF => mem_write_value(paddr, 2, xs2_val[15..0], aq, rl, false),
              WORD => mem_write_value(paddr, 4, xs2_val[31..0], aq, rl, false),
              DOUBLE if sizeof(xlen) >= 64
                => mem_write_value(paddr, 8, xs2_val, aq, rl, false),
              _ => report_invalid_width(__FILE__, __LINE__, width, "store"),
            };
            match (res) {
              MemValue(true) => RETIRE_SUCCESS,
              MemValue(false) => internal_error(__FILE__, __LINE__, "store got false from mem_write_value"),
              MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL }
            }
          }
        }
      }
    }
}

```

B.210.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

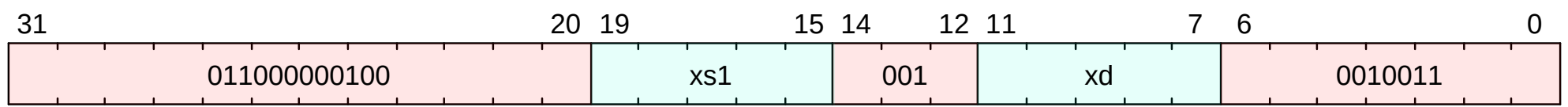
B.211. sext.b

Sign-extend byte

This instruction is defined by:

Zbb

B.211.1. Encoding



B.211.2. Description

Sign-extends the least-significant byte in the source to XLEN by copying the most-significant bit in the byte (i.e., bit 7) to all of the more-significant bits.

B.211.3. Access

M	S	U
Always	Always	Always

B.211.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.211.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (xlen() == 32) {
  X[xd] = {{24{X[xs1][7]}}, X[xs1][7:0]};
} else if (xlen() == 64) {
  X[xd] = {{56{X[xs1][7]}}, X[xs1][7:0]};
}
```

B.211.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let result : xlenbits = match op {
    RISCV_SEXTB => sign_extend(rs1_val[7..0]),
    RISCV_SEXTH => sign_extend(rs1_val[15..0]),
    RISCV_ZEXTH => zero_extend(rs1_val[15..0])
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.211.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

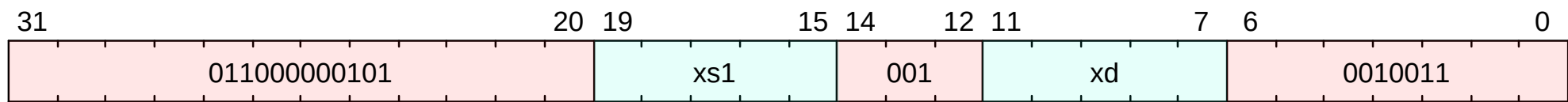
B.212. sext.h

Sign-extend halfword

This instruction is defined by:

Zbb

B.212.1. Encoding



B.212.2. Description

Sign-extends the least-significant halfword in the source to XLEN by copying the most-significant bit in the halfword (i.e., bit 15) to all of the more-significant bits.

B.212.3. Access

M	S	U
Always	Always	Always

B.212.4. Decode Variables

```
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.212.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (xlen() == 32) {
  X[xd] = {{16{X[xs1][15]}}, X[xs1][15:0]};
} else if (xlen() == 64) {
  X[xd] = {{48{X[xs1][15]}}, X[xs1][15:0]};
}
```

B.212.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let result : xlenbits = match op {
    RISCV_SEXTB => sign_extend(rs1_val[7..0]),
    RISCV_SEXTH => sign_extend(rs1_val[15..0]),
    RISCV_ZEXTH => zero_extend(rs1_val[15..0])
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.212.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

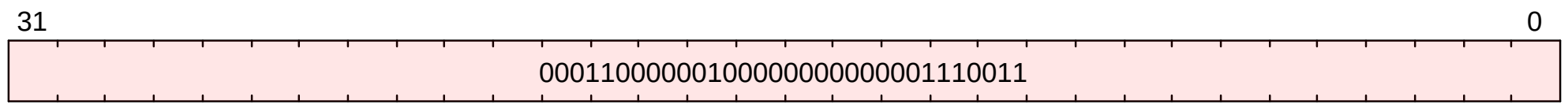
B.213. sfence.inval.ir

Order implicit page table reads after invalidation

This instruction is defined by:

[Svinval](#)

B.213.1. Encoding



B.213.2. Description

The [sfence.inval.ir](#) instruction guarantees that any previous [sINVAL.vma](#) instructions executed by the current hart are ordered before subsequent implicit references by that hart to the memory-management data structures.

B.213.3. Access

M	S	U
Always	Sometimes	Never

B.213.4. Decode Variables

B.213.5. IDL Operation

```
if (mode() == PrivilegeMode::U) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VU) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
}
VmaOrderType vma_type;
vma_type.global = true;
vma_type.smode = true;
if (CSR[misa].H == 1) {
    vma_type.vsmode = true;
    vma_type.gstage = true;
}
order_pgtbl_reads_after_vmafence(vma_type);
```

B.213.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- VirtualInstruction

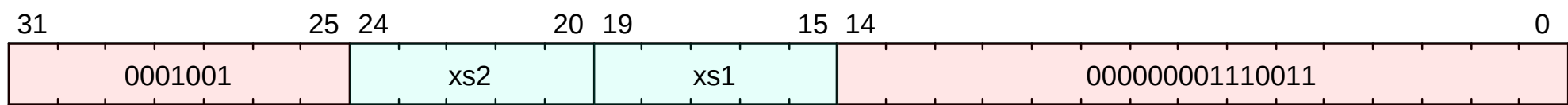
B.214. sfence.vma

Supervisor memory-management fence

This instruction is defined by:

S

B.214.1. Encoding



B.214.2. Description

The supervisor memory-management fence instruction **SFENCE.VMA** is used to synchronize updates to in-memory memory-management data structures with current execution. Instruction execution causes implicit reads and writes to these data structures; however, these implicit references are ordinarily not ordered with respect to explicit loads and stores. Executing an SFENCE.VMA instruction guarantees that any previous stores already visible to the current RISC-V hart are ordered before certain implicit references by subsequent instructions in that hart to the memory-management data structures. The specific set of operations ordered by SFENCE.VMA is determined by *xs1* and *xs2*, as described below. SFENCE.VMA is also used to invalidate entries in the address-translation cache associated with a hart (see [\[sv32algorithm\]](#)). Further details on the behavior of this instruction are described in [\[virt-control\]](#) and [\[pmp-vmem\]](#).



The SFENCE.VMA is used to flush any local hardware caches related to address translation. It is specified as a fence rather than a TLB flush to provide cleaner semantics with respect to which instructions are affected by the flush operation and to support a wider variety of dynamic caching structures and memory-management schemes. SFENCE.VMA is also used by higher privilege levels to synchronize page table writes and the address translation hardware.

SFENCE.VMA orders only the local hart’s implicit references to the memory-management data structures.



Consequently, other harts must be notified separately when the memory-management data structures have been modified. One approach is to use 1) a local data fence to ensure local writes are visible globally, then 2) an interprocessor interrupt to the other thread, then 3) a local SFENCE.VMA in the interrupt handler of the remote thread, and finally 4) signal back to originating thread that operation is complete. This is, of course, the RISC-V analog to a TLB shutdown.

For the common case that the translation data structures have only been modified for a single address mapping (i.e., one page or superpage), *xs1* can specify a virtual address within that mapping to effect a translation fence for that mapping only. Furthermore, for the common case that the translation data structures have only been modified for a single address-space identifier, *xs2* can specify the address space. The behavior of SFENCE.VMA depends on *xs1* and *xs2* as follows:

- If *xs1*=**x0** and *xs2*=**x0**, the fence orders all reads and writes made to any level of the page tables, for all address spaces. The fence also invalidates all address-translation cache entries, for all address spaces.
- If *xs1*=**x0** and *xs2*≠**x0**, the fence orders all reads and writes made to any level of the page tables, but only for the address space identified by integer register *xs2*. Accesses to *global* mappings (see [\[translation\]](#)) are not ordered. The fence also invalidates all address-translation cache entries matching the address space identified by integer register *xs2*, except for entries containing global mappings.
- If *xs1*≠**x0** and *xs2*=**x0**, the fence orders only reads and writes made to leaf page table entries corresponding to the virtual address in *xs1*, for all address spaces. The fence also invalidates all address-translation cache entries that contain leaf page table entries corresponding to the virtual address in *xs1*, for all address spaces.
- If *xs1*≠**x0** and *xs2*≠**x0**, the fence orders only reads and writes made to leaf page table entries corresponding to the virtual address in *xs1*, for the address space identified by integer register *xs2*. Accesses to global mappings are not ordered. The fence also invalidates all address-translation cache entries that contain leaf page table entries corresponding to the virtual address in *xs1* and that match the address space identified by integer register *xs2*, except for entries containing global mappings.

If the value held in *xs1* is not a valid virtual address, then the SFENCE.VMA instruction has no effect. No exception is raised in this case.

When *xs2*≠**x0**, bits SXLEN-1:ASIDMAX of the value held in *xs2* are reserved for future standard use. Until their use is defined by a standard extension, they should be zeroed by software and ignored by current implementations. Furthermore, if ASIDLEN<ASIDMAX, the implementation shall ignore bits ASIDMAX-1:ASIDLEN of the value held in *xs2*.



It is always legal to over-fence, e.g., by fencing only based on a subset of the bits in *xs1* and/or *xs2*, and/or by simply treating all SFENCE.VMA instructions as having *xs1*=**x0** and/or *xs2*=**x0**. For example, simpler implementations can ignore the virtual address in *xs1* and the ASID value in *xs2* and always perform a global fence. The choice not to raise an exception when an invalid virtual address is held in *xs1* facilitates this type of simplification.

An implicit read of the memory-management data structures may return any translation for an address that was valid at any time since the most recent SFENCE.VMA that subsumes that address. The ordering implied by SFENCE.VMA does not place implicit reads and writes to the memory-management data structures into the global memory order in a way that interacts cleanly with the standard RVWMO ordering rules. In particular, even though an SFENCE.VMA orders prior explicit accesses before subsequent implicit accesses, and those implicit accesses are ordered before their

associated explicit accesses, SFENCE.VMA does not necessarily place prior explicit accesses before subsequent explicit accesses in the global memory order. These implicit loads also need not otherwise obey normal program order semantics with respect to prior loads or stores to the same address.



A consequence of this specification is that an implementation may use any translation for an address that was valid at any time since the most recent SFENCE.VMA that subsumes that address. In particular, if a leaf PTE is modified but a subsuming SFENCE.VMA is not executed, either the old translation or the new translation will be used, but the choice is unpredictable. The behavior is otherwise well-defined.

In a conventional TLB design, it is possible for multiple entries to match a single address if, for example, a page is upgraded to a superpage without first clearing the original non-leaf PTE’s valid bit and executing an SFENCE.VMA with $xs1=x0$. In this case, a similar remark applies: it is unpredictable whether the old non-leaf PTE or the new leaf PTE is used, but the behavior is otherwise well defined.

Another consequence of this specification is that it is generally unsafe to update a PTE using a set of stores of a width less than the width of the PTE, as it is legal for the implementation to read the PTE at any time, including when only some of the partial stores have taken effect.

This specification permits the caching of PTEs whose V (Valid) bit is clear. Operating systems must be written to cope with this possibility, but implementers are reminded that eagerly caching invalid PTEs will reduce performance by causing additional page faults.

Implementations must only perform implicit reads of the translation data structures pointed to by the current contents of the [satp](#) register or a subsequent valid (V=1) translation data structure entry, and must only raise exceptions for implicit accesses that are generated as a result of instruction execution, not those that are performed speculatively.

Changes to the [sstatus](#) fields SUM and MXR take effect immediately, without the need to execute an SFENCE.VMA instruction. Changing [satp](#).MODE from Bare to other modes and vice versa also takes effect immediately, without the need to execute an SFENCE.VMA instruction. Likewise, changes to [satp](#).ASID take effect immediately.



The following common situations typically require executing an SFENCE.VMA instruction:

- When software recycles an ASID (i.e., reassociates it with a different page table), it should *first* change [satp](#) to point to the new page table using the recycled ASID, *then* execute SFENCE.VMA with $xs1=x0$ and $xs2$ set to the recycled ASID. Alternatively, software can execute the same SFENCE.VMA instruction while a different ASID is loaded into [satp](#), provided the next time [satp](#) is loaded with the recycled ASID, it is simultaneously loaded with the new page table.
- If the implementation does not provide ASIDs, or software chooses to always use ASID 0, then after every [satp](#) write, software should execute SFENCE.VMA with $xs1=x0$. In the common case that no global translations have been modified, $xs2$ should be set to a register other than $x0$ but which contains the value zero, so that global translations are not flushed.
- If software modifies a non-leaf PTE, it should execute SFENCE.VMA with $xs1=x0$. If any PTE along the traversal path had its G bit set, $xs2$ must be $x0$; otherwise, $xs2$ should be set to the ASID for which the translation is being modified.
- If software modifies a leaf PTE, it should execute SFENCE.VMA with $xs1$ set to a virtual address within the page. If any PTE along the traversal path had its G bit set, $xs2$ must be $x0$; otherwise, $xs2$ should be set to the ASID for which the translation is being modified.
- For the special cases of increasing the permissions on a leaf PTE and changing an invalid PTE to a valid leaf, software may choose to execute the SFENCE.VMA lazily. After modifying the PTE but before executing SFENCE.VMA, either the new or old permissions will be used. In the latter case, a page-fault exception might occur, at which point software should execute SFENCE.VMA in accordance with the previous bullet point.

If a hart employs an address-translation cache, that cache must appear to be private to that hart. In particular, the meaning of an ASID is local to a hart; software may choose to use the same ASID to refer to different address spaces on different harts.



A future extension could redefine ASIDs to be global across the SEE, enabling such options as shared translation caches and hardware support for broadcast TLB shutdown. However, as OSes have evolved to significantly reduce the scope of TLB shutdowns using novel ASID-management techniques, we expect the local-ASID scheme to remain attractive for its simplicity and possibly better scalability.

For implementations that make [satp](#).MODE read-only zero (always Bare), attempts to execute an SFENCE.VMA instruction might raise an illegal-instruction exception.

B.214.3. Access

M	S	U
Always	Always	Never

B.214.4. Decode Variables

Bits<5> $xs2 = \$encoding[24:20];$

```
Bits<5> xs1 = $encoding[19:15];
```

B.214.5. IDL Operation

```
XReg vaddr = X[xs1];
Bits<16> asid = X[xs2][ASID_WIDTH - 1:0];
if (mode() == PrivilegeMode::U) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VU) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[mstatus].TVM == 1 && mode() == PrivilegeMode::S) || (mode() == PrivilegeMode::VS) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && CSR[hstatus].VTVM == 1 && mode() == PrivilegeMode::VS) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
}
if (!implemented?(ExtensionName::Sv32) && !implemented?(ExtensionName::Sv39) && !implemented?(ExtensionName::Sv48) && !
    implemented?(ExtensionName::Sv57)) {
    if (TRAP_ON_SFENCE_VMA_WHEN_SATP_MODE_IS_READ_ONLY) {
        raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
}
VmaOrderType vma_type;
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VS) {
    vma_type.vsmode = true;
    vma_type.single_vmid = true;
    vma_type.vmid = CSR[hgatp].VMID;
} else {
    vma_type.smode = true;
}
if ((xs1 == 0) && (xs2 == 0)) {
    vma_type.global = true;
    order_pgtbl_writes_before_vmafence(vma_type);
    invalidate_translations(vma_type);
    order_pgtbl_reads_after_vmafence(vma_type);
} else if ((xs1 == 0) && (xs2 != 0)) {
    vma_type.single_asid = true;
    vma_type.asid = asid;
    order_pgtbl_writes_before_vmafence(vma_type);
    invalidate_translations(vma_type);
    order_pgtbl_reads_after_vmafence(vma_type);
} else if ((xs1 != 0) && (xs2 == 0)) {
    if (canonical_vaddr?(vaddr)) {
        vma_type.single_vaddr = true;
        vma_type.vaddr = vaddr;
        order_pgtbl_writes_before_vmafence(vma_type);
        invalidate_translations(vma_type);
        order_pgtbl_reads_after_vmafence(vma_type);
    }
} else {
    if (canonical_vaddr?(vaddr)) {
        vma_type.single_asid = true;
        vma_type.asid = asid;
        vma_type.single_vaddr = true;
        vma_type.vaddr = vaddr;
        order_pgtbl_writes_before_vmafence(vma_type);
        invalidate_translations(vma_type);
        order_pgtbl_reads_after_vmafence(vma_type);
    }
}
}
```

B.214.6. Sail Operation

```
{
    let addr : option(xlenbits) = if rs1 == 0b000000 then None() else Some(X(rs1));
    let asid : option(xlenbits) = if rs2 == 0b000000 then None() else Some(X(rs2));
    match cur_privilege {
        User      => { handle_illegal(); RETIRE_FAIL },
        Supervisor => match (architecture(get_mstatus_SXL(mstatus)), mstatus.TVM()) {
            (Some(_), 0b1) => { handle_illegal(); RETIRE_FAIL },

```



```

        (Some(_), 0b0) => { flush_TLB(asid, addr); RETIRE_SUCCESS },
        (_, _)      => internal_error(__FILE__, __LINE__, "unimplemented sfence architecture")
    },
    Machine    => { flush_TLB(asid, addr); RETIRE_SUCCESS }
}
}

```

B.214.7. Exceptions

This instruction may result in the following synchronous exceptions:

- `IllegalInstruction`
- `VirtualInstruction`

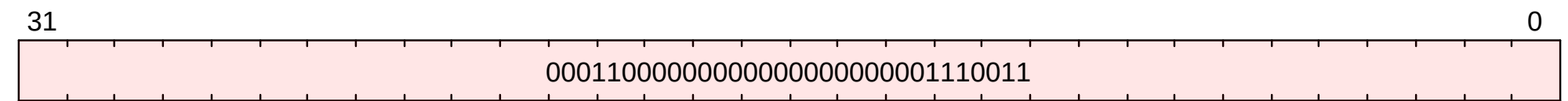
B.215. sfence.w inval

Order writes before sfence

This instruction is defined by:

Svinval

B.215.1. Encoding



B.215.2. Description

The `sfence.w.inval` instruction guarantees that any previous stores already visible to the current RISC-V hart are ordered before subsequent `sinval.vma` instructions executed by the same hart.

B.215.3. Access

M	S	U
Always	Sometimes	Never

B.215.4. Decode Variables

B.215.5. IDL Operation

```
if (mode() == PrivilegeMode::U) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VU) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
}
VmaOrderType vma_type;
vma_type.global = true;
vma_type.smode = true;
if (CSR[misa].H == 1) {
    vma_type.vsmode = true;
    vma_type.gstage = true;
}
order_pgtbl_writes_before_vmafence(vma_type);
```

B.215.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- VirtualInstruction

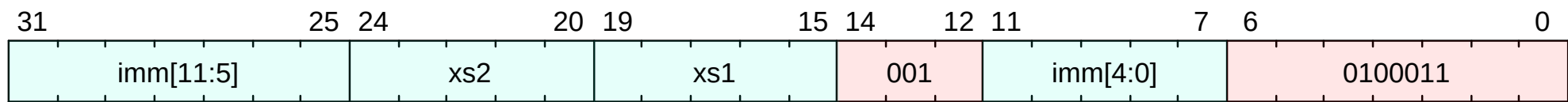
B.216. sh

Store halfword

This instruction is defined by:

I

B.216.1. Encoding



B.216.2. Description

Store 16 bits of data from register **xs2** to an address formed by adding **xs1** to a signed offset.

B.216.3. Access

M	S	U
Always	Always	Always

B.216.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.216.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
write_memory<16>(virtual_address, X[xs2][15:0], $encoding);
```

B.216.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Write(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Write(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) => {
          let eares : MemoryOpResult(unit) = match width {
            BYTE => mem_write_ea(paddr, 1, aq, rl, false),
            HALF => mem_write_ea(paddr, 2, aq, rl, false),
            WORD => mem_write_ea(paddr, 4, aq, rl, false),
            DOUBLE => mem_write_ea(paddr, 8, aq, rl, false)
          };
          match (eares) {
            MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
            MemValue(_) => {
              let xs2_val = X(xs2);
              let res : MemoryOpResult(bool) = match (width) {
                BYTE => mem_write_value(paddr, 1, xs2_val[7..0], aq, rl, false),
                HALF => mem_write_value(paddr, 2, xs2_val[15..0], aq, rl, false),
                WORD => mem_write_value(paddr, 4, xs2_val[31..0], aq, rl, false),
                DOUBLE if sizeof(xlen) >= 64
                  => mem_write_value(paddr, 8, xs2_val, aq, rl, false),
                _ => report_invalid_width(__FILE__, __LINE__, width, "store"),
              };
              match (res) {
                MemValue(true) => RETIRE_SUCCESS,
                MemValue(false) => internal_error(__FILE__, __LINE__, "store got false from mem_write_value"),
              }
            }
          }
        }
      }
  }
}
```

```
MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL }  
    }  
    }  
    }  
    }  
    }  
    }
```

B.216.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

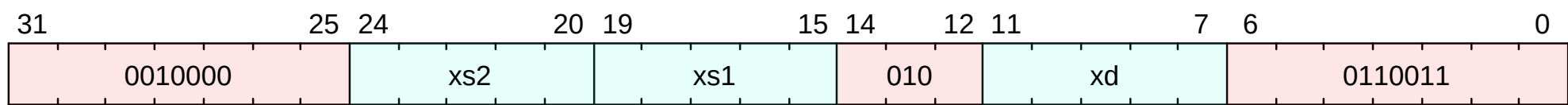
B.217. sh1add

Shift left by 1 and add

This instruction is defined by:

Zba

B.217.1. Encoding



B.217.2. Description

Shifts **xs1** to the left by 1 bit and adds it to **xs2**.

B.217.3. Access

M	S	U
Always	Always	Always

B.217.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.217.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs2] + (X[xs1] << 1);
```

B.217.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let shamt : bits(2) = match op {
        RISCV_SH1ADD => 0b01,
        RISCV_SH2ADD => 0b10,
        RISCV_SH3ADD => 0b11
    };
    let result : xlenbits = (rs1_val << shamt) + rs2_val;
    X(rd) = result;
    RETIRE_SUCCESS
}
```

B.217.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

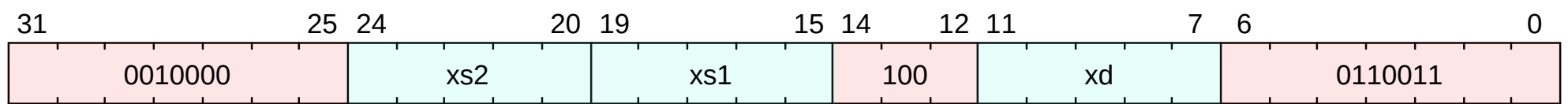
B.218. sh2add

Shift left by 2 and add

This instruction is defined by:

Zba

B.218.1. Encoding



B.218.2. Description

Shifts **xs1** to the left by 2 places and adds it to **xs2**.

B.218.3. Access

M	S	U
Always	Always	Always

B.218.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.218.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs2] + (X[xs1] << 2);
```

B.218.6. Sail Operation

```
{
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    let shamt : bits(2) = match op {
        RISCV_SH1ADD => 0b01,
        RISCV_SH2ADD => 0b10,
        RISCV_SH3ADD => 0b11
    };
    let result : xlenbits = (rs1_val << shamt) + rs2_val;
    X(rd) = result;
    RETIRE_SUCCESS
}
```

B.218.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

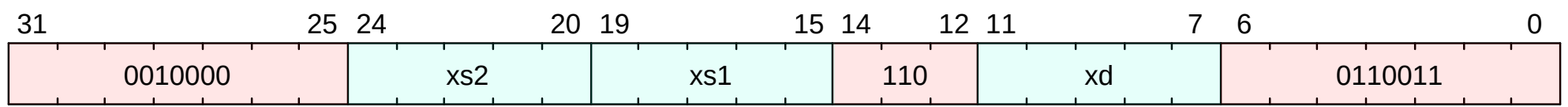
B.219. sh3add

Shift left by 3 and add

This instruction is defined by:

Zba

B.219.1. Encoding



B.219.2. Description

Shifts **xs1** to the left by 3 places and adds it to **xs2**.

B.219.3. Access

M	S	U
Always	Always	Always

B.219.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.219.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = X[xs2] + (X[xs1] << 3);
```

B.219.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let shamt : bits(2) = match op {
    RISCV_SH1ADD => 0b01,
    RISCV_SH2ADD => 0b10,
    RISCV_SH3ADD => 0b11
  };
  let result : xlenbits = (rs1_val << shamt) + rs2_val;
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.219.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

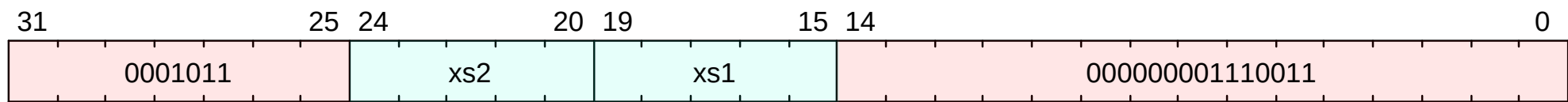
B.220. sinval.vma

Invalidate cached address translations

This instruction is defined by:

[Svinval](#)

B.220.1. Encoding



B.220.2. Description

The [sinval.vma](#) instruction invalidates any address-translation cache entries that an [sfence.vma](#) instruction with the same values of xs1 and xs2 would invalidate. However, unlike [sfence.vma](#), [sinval.vma](#) instructions are only ordered with respect to [sfence.vma](#), [sfence.w.inval](#), and [sfence.inval.ir](#) instructions as defined below.

B.220.3. Access

M	S	U
Always	Sometimes	Never

B.220.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.220.5. IDL Operation

```
XReg vaddr = X[xs1];
Bits<ASID_WIDTH> asid = X[xs2][ASID_WIDTH - 1:0];
if (CSR[mstatus].TVM == 1 && mode() == PrivilegeMode::S) || (mode() == PrivilegeMode::VS) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && CSR[hstatus].VTVM == 1 && mode() == PrivilegeMode::VS) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
}
if (mode() == PrivilegeMode::U) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VU) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
}
VmaOrderType vma_type;
if (CSR[misa].H == 1 && mode() == PrivilegeMode::VS) {
    vma_type.vsmode = true;
    vma_type.single_vmid = true;
    vma_type.vmid = CSR[hgatp].VMID;
} else {
    vma_type.smode = true;
}
if ((xs1 == 0) && (xs2 == 0)) {
    vma_type.global = true;
    invalidate_translations(vma_type);
} else if ((xs1 == 0) && (xs2 != 0)) {
    vma_type.single_asid = true;
    vma_type.asid = asid;
    invalidate_translations(vma_type);
} else if ((xs1 != 0) && (xs2 == 0)) {
    if (canonical_vaddr?(vaddr)) {
        vma_type.single_vaddr = true;
        vma_type.vaddr = vaddr;
        invalidate_translations(vma_type);
    }
} else {
    if (canonical_vaddr?(vaddr)) {
        vma_type.single_asid = true;
```



```
vma_type.asid = asid;
vma_type.single_vaddr = true;
vma_type.vaddr = vaddr;
invalidate_translations(vma_type);
}
}
```

B.220.6. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- VirtualInstruction

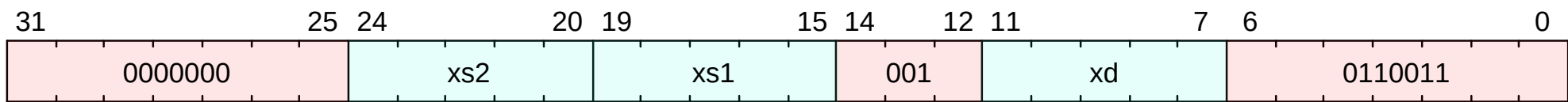
B.221. sll

Shift left logical

This instruction is defined by:

I

B.221.1. Encoding



B.221.2. Description

Shift the value in **xs1** left by the value in the lower 6 bits of **xs2**, and store the result in **xd**.

B.221.3. Access

M	S	U
Always	Always	Always

B.221.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.221.5. IDL Operation

```
if (xlen() == 64) {
  X[xd] = X[xs1] << X[xs2][5:0];
} else {
  X[xd] = X[xs1] << X[xs2][4:0];
}
```

B.221.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCv_ADD => xs1_val + xs2_val,
    RISCv_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCv_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCv_AND => xs1_val & xs2_val,
    RISCv_OR => xs1_val | xs2_val,
    RISCv_XOR => xs1_val ^ xs2_val,
    RISCv_SLL => if sizeof(xlen) == 32
      then xs1_val << (xs2_val[4..0])
      else xs1_val << (xs2_val[5..0]),
    RISCv_SRL => if sizeof(xlen) == 32
      then xs1_val >> (xs2_val[4..0])
      else xs1_val >> (xs2_val[5..0]),
    RISCv_SUB => xs1_val - xs2_val,
    RISCv_SRA => if sizeof(xlen) == 32
      then shift_right_arith32(xs1_val, xs2_val[4..0])
      else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.221.7. Exceptions

This instruction does not generate synchronous exceptions.

B.222. slli

Shift left logical immediate

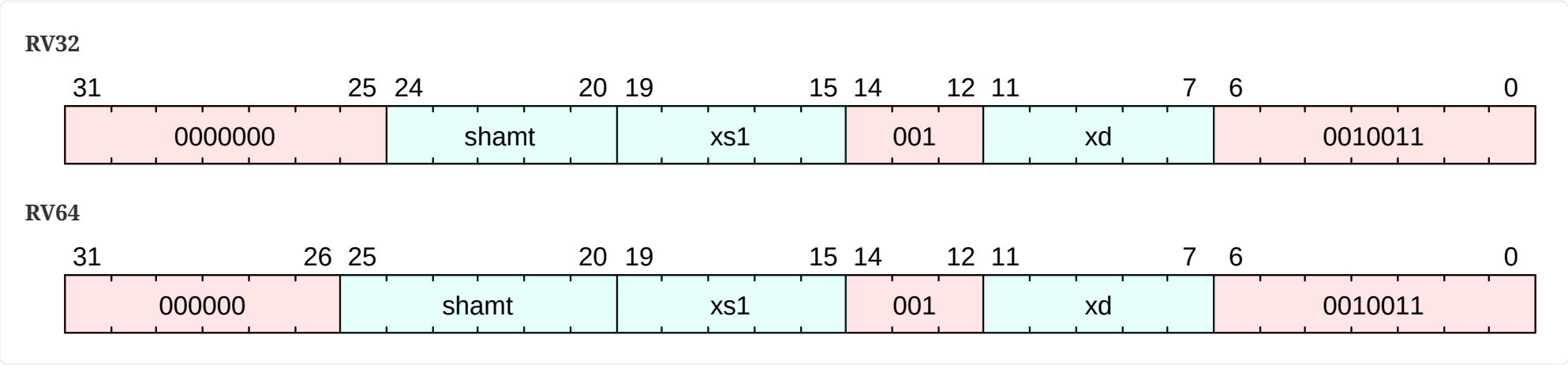
This instruction is defined by:

I

B.222.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.222.2. Description

Shift the value in xs1 left by shamt, and store the result in xd

B.222.3. Access

M	S	U
Always	Always	Always

B.222.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.222.5. IDL Operation

```
X[xd] = X[xs1] << shamt;
```

B.222.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  /* the decoder guaxd should ensure that shamt[5] = 0 for RV32 */
  let result : xlenbits = match op {
    RISCv_SLLI => if sizeof(xlen) == 32
                  then xs1_val << shamt[4..0]
                  else xs1_val << shamt,
    RISCv_SRLI => if sizeof(xlen) == 32
                  then xs1_val >> shamt[4..0]
                  else xs1_val >> shamt,
    RISCv_SRAI => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, shamt[4..0])
                  else shift_right_arith64(xs1_val, shamt)
  };
};
```

```
X(xd) = result;  
RETIRE_SUCCESS  
}
```

B.222.7. Exceptions

This instruction does not generate synchronous exceptions.

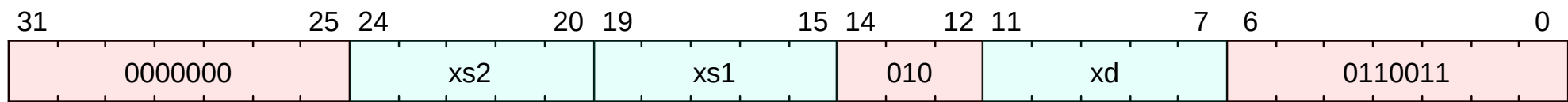
B.223. slt

Set on less than

This instruction is defined by:

I

B.223.1. Encoding



B.223.2. Description

Places the value 1 in register **xd** if register **xs1** is less than the value in register **xs2**, where both sources are treated as signed numbers, else 0 is written to **xd**.

B.223.3. Access

M	S	U
Always	Always	Always

B.223.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.223.5. IDL Operation

```
XReg src1 = X[xs1];
XReg src2 = X[xs2];
X[xd] = ($signed(src1) < $signed(src2)) ? '1' : '0';
```

B.223.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD => xs1_val + xs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND => xs1_val & xs2_val,
    RISCV_OR  => xs1_val | xs2_val,
    RISCV_XOR => xs1_val ^ xs2_val,
    RISCV_SLL => if  sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL => if  sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB => xs1_val - xs2_val,
    RISCV_SRA => if  sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.223.7. Exceptions

This instruction does not generate synchronous exceptions.

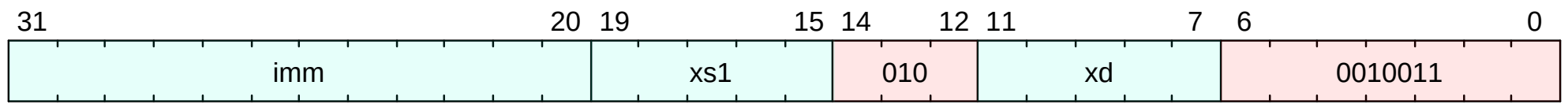
B.224. slti

Set on less than immediate

This instruction is defined by:

I

B.224.1. Encoding



B.224.2. Description

Places the value 1 in register **xd** if register **xs1** is less than the sign-extended immediate when both are treated as signed numbers, else 0 is written to **xd**.

B.224.3. Access

M	S	U
Always	Always	Always

B.224.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.224.5. IDL Operation

```
X[xd] = ($signed(X[xs1]) < $signed(imm)) ? '1' : '0';
```

B.224.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.224.7. Exceptions

This instruction does not generate synchronous exceptions.

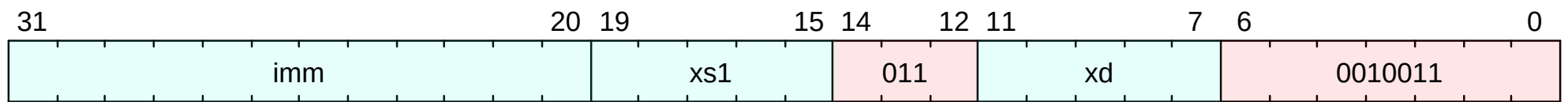
B.225. sltiu

Set on less than immediate unsigned

This instruction is defined by:

I

B.225.1. Encoding



B.225.2. Description

Places the value 1 in register `xd` if register `xs1` is less than the sign-extended immediate when both are treated as unsigned numbers (i.e., the immediate is first sign-extended to XLEN bits then treated as an unsigned number), else 0 is written to `xd`.

`sltiu xd, xs1, 1` sets `xd` to 1 if `xs1` equals zero, otherwise sets `xd` to 0 (assembler pseudoinstruction `SEQZ xd, rs`).

B.225.3. Access

M	S	U
Always	Always	Always

B.225.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.225.5. IDL Operation

```
Bits<MXLEN> sign_extend_imm = $signed(imm);
X[xd] = (X[xs1] < sign_extend_imm) ? 1 : 0;
```

B.225.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.225.7. Exceptions

This instruction does not generate synchronous exceptions.

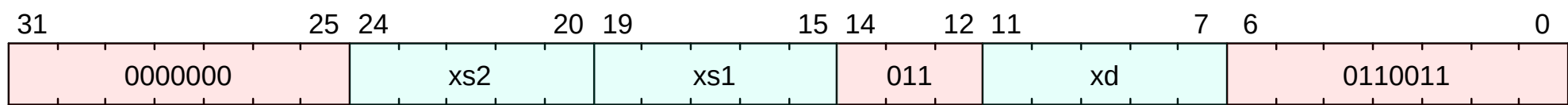
B.226. sltu

Set on less than unsigned

This instruction is defined by:

I

B.226.1. Encoding



B.226.2. Description

Places the value 1 in register **xd** if register **xs1** is less than the value in register **xs2**, where both sources are treated as unsigned numbers, else 0 is written to **xd**.

B.226.3. Access

M	S	U
Always	Always	Always

B.226.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.226.5. IDL Operation

```
X[xd] = (X[xs1] < X[xs2]) ? 1 : 0;
```

B.226.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD => xs1_val + xs2_val,
    RISCV_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND => xs1_val & xs2_val,
    RISCV_OR  => xs1_val | xs2_val,
    RISCV_XOR => xs1_val ^ xs2_val,
    RISCV_SLL => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB => xs1_val - xs2_val,
    RISCV_SRA => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.226.7. Exceptions

This instruction does not generate synchronous exceptions.

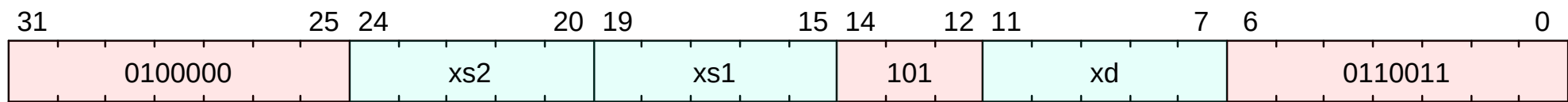
B.227. sra

Shift right arithmetic

This instruction is defined by:

I

B.227.1. Encoding



B.227.2. Description

Arithmetic shift the value in **xs1** right by the value in the lower 5 bits of **xs2**, and store the result in **xd**.

B.227.3. Access

M	S	U
Always	Always	Always

B.227.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.227.5. IDL Operation

```
if (xlen() == 64) {
  X[xd] = X[xs1] >>> X[xs2][5:0];
} else {
  X[xd] = X[xs1] >>> X[xs2][4:0];
}
```

B.227.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCv_ADD => xs1_val + xs2_val,
    RISCv_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCv_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCv_AND => xs1_val & xs2_val,
    RISCv_OR => xs1_val | xs2_val,
    RISCv_XOR => xs1_val ^ xs2_val,
    RISCv_SLL => if sizeof(xlen) == 32
      then xs1_val << (xs2_val[4..0])
      else xs1_val << (xs2_val[5..0]),
    RISCv_SRL => if sizeof(xlen) == 32
      then xs1_val >> (xs2_val[4..0])
      else xs1_val >> (xs2_val[5..0]),
    RISCv_SUB => xs1_val - xs2_val,
    RISCv_SRA => if sizeof(xlen) == 32
      then shift_right_arith32(xs1_val, xs2_val[4..0])
      else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.227.7. Exceptions

This instruction does not generate synchronous exceptions.

B.228. srai

Shift right arithmetic immediate

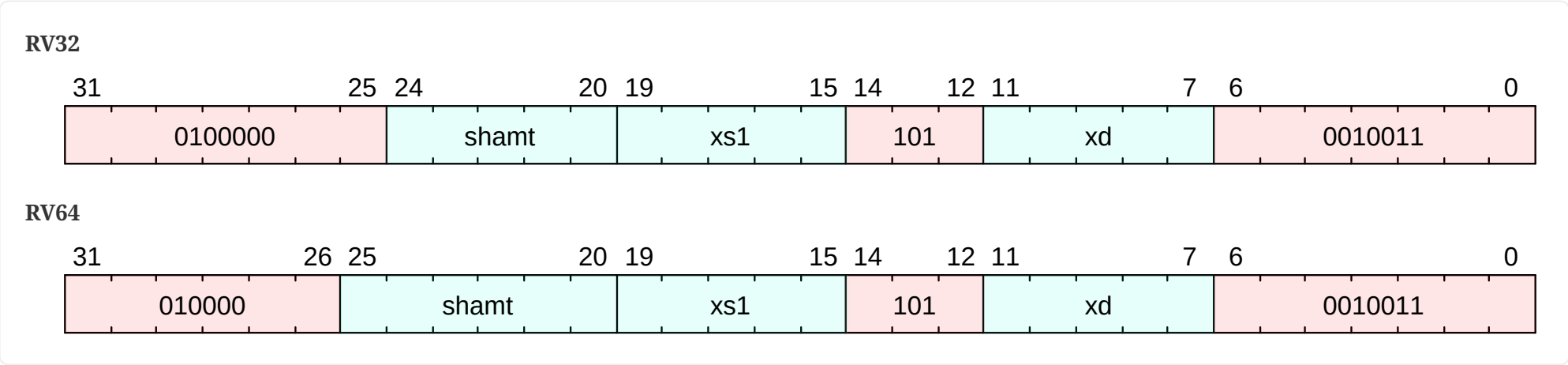
This instruction is defined by:

I

B.228.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.228.2. Description

Arithmetic shift (the original sign bit is copied into the vacated upper bits) the value in xs1 right by shamt, and store the result in xd.

B.228.3. Access

M	S	U
Always	Always	Always

B.228.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.228.5. IDL Operation

```
X[xd] = X[xs1] >>> shamt;
```

B.228.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  /* the decoder guaxd should ensure that shamt[5] = 0 for RV32 */
  let result : xlenbits = match op {
    RISCV_SLLI => if  sizeof(xlen) == 32
                  then xs1_val << shamt[4..0]
                  else xs1_val << shamt,
    RISCV_SRLI => if  sizeof(xlen) == 32
                  then xs1_val >> shamt[4..0]
                  else xs1_val >> shamt,
    RISCV_SRAI => if  sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, shamt[4..0])
                  else shift_right_arith64(xs1_val, shamt)
  };
};
```

```
X(xd) = result;  
RETIRE_SUCCESS  
}
```

B.228.7. Exceptions

This instruction does not generate synchronous exceptions.

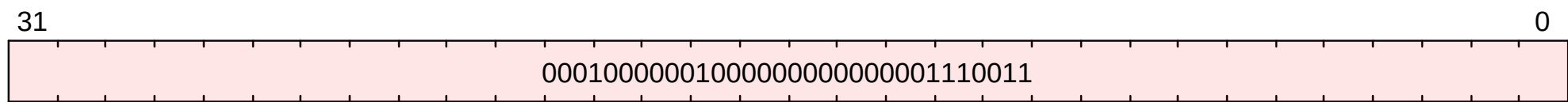
B.229. sret

Supervisor Mode Return from Trap

This instruction is defined by:

S

B.229.1. Encoding



B.229.2. Description

Returns from supervisor mode after handling a trap.

When [sret](#) is allowed to execute, its behavior depends on whether or not the current privilege mode is virtualized.

When the current privilege mode is (H)S-mode or M-mode

[sret](#) sets [hstatus](#) = 0, [mstatus.SPP](#) = 0, [mstatus.SIE](#) = [mstatus.SPIE](#), and [mstatus.SPIE](#) = 1, changes the privilege mode according to the table below, and then jumps to the address in [sepc](#).

Table 18. Next privilege mode following an [sret](#) in (H)S-mode or M-mode

mstatus.SPP	hstatus.SPV	Mode after sret
0	0	U-mode
0	1	VU-mode
1	0	(H)S-mode
1	1	VS-mode

When the current privilege mode is VS-mode

[sret](#) sets [vsstatus.SPP](#) = 0, [vsstatus.SIE](#) = [vstatus.SPIE](#), and [vsstatus.SPIE](#) = 1, changes the privilege mode according to the table below, and then jumps to the address in [vsepc](#).

Table 19. Next privilege mode following an [sret](#) in (H)S-mode or M-mode

vsstatus.SPP	Mode after sret
0	VU-mode
1	VS-mode

B.229.3. Access

M	S	U
Always	Sometimes	Never

Access is determined as follows:

mstatus.TSR	hstatus.VTSR	Behavior when executed from:				
		M-mode	U-mode	(H)S-mode	VU-mode	VS-mode
0	0	executes	Illegal Instruction	executes	Virtual Instruction	executes
0	1	executes	Illegal Instruction	executes	Virtual Instruction	Virtual Instruction
1	0	executes	Illegal Instruction	Illegal Instruction	Virtual Instruction	executes
1	1	executes	Illegal Instruction	Illegal Instruction	Virtual Instruction	Virtual Instruction

B.229.4. Decode Variables

B.229.5. IDL Operation

```
if (implemented?(ExtensionName::H)) {
  if (CSR[mstatus].TSR == 1'b0 && CSR[hstatus].VTSR == 1'b0) {
    if (mode() == PrivilegeMode::U) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    } else if (mode() == PrivilegeMode::VU) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  } else if (CSR[mstatus].TSR == 1'b0 && CSR[hstatus].VTSR == 1'b1) {
    if (mode() == PrivilegeMode::U) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    } else if (mode() == PrivilegeMode::VU || mode() == PrivilegeMode::VS) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  } else if (CSR[mstatus].TSR == 1'b1 && CSR[hstatus].VTSR == 1'b0) {
    if (mode() == PrivilegeMode::U || mode() == PrivilegeMode::S) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    } else if (mode() == PrivilegeMode::VU) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  } else if (CSR[mstatus].TSR == 1'b1 && CSR[hstatus].VTSR == 1'b1) {
    if (mode() == PrivilegeMode::U || mode() == PrivilegeMode::S) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    } else if (mode() == PrivilegeMode::VU || mode() == PrivilegeMode::VS) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  }
} else {
  if (mode() == PrivilegeMode::U) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
if (!virtual_mode?()) {
  if (implemented?(ExtensionName::H)) {
    if (CSR[hstatus].SPV == 1'b1) {
      if (CSR[mstatus].SPP == 1'b1) {
        set_mode(PrivilegeMode::VS);
      } else {
        set_mode(PrivilegeMode::VU);
      }
    } else {
      if (CSR[mstatus].SPP == 1'b1) {
        set_mode(PrivilegeMode::S);
      } else {
        set_mode(PrivilegeMode::U);
      }
    }
    CSR[hstatus].SPV = 0;
  } else {
    if (CSR[mstatus].SPP == 1'b1) {
      set_mode(PrivilegeMode::S);
    } else {
      set_mode(PrivilegeMode::U);
    }
  }
  CSR[mstatus].SIE = CSR[mstatus].SPIE;
  CSR[mstatus].SPIE = 1;
  CSR[mstatus].SPP = 2'b00;
  $pc = $bits(CSR[CSR[sepc]]);
} else {
  if (CSR[mstatus].TSR == 1'b1) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
  CSR[vsstatus].SPP = 0;
  CSR[vsstatus].SIE = CSR[vsstatus].SPIE;
  CSR[vsstatus].SPIE = 1;
  $pc = $bits(CSR[CSR[vsepc]]);
}
```

B.229.6. Sail Operation

```

{
  let sret_illegal : bool = match cur_privilege {
    User      => true,
    Supervisor => not(haveSupMode ()) | mstatus.TSR() == 0b1,
    Machine    => not(haveSupMode ())
  };
  if sret_illegal
  then { handle_illegal(); RETIRE_FAIL }
  else if not(ext_check_xret_priv (Supervisor))
  then { ext_fail_xret_priv(); RETIRE_FAIL }
  else {
    set_next_pc(exception_handler(cur_privilege, CTL_SRET(), PC));
    RETIRE_SUCCESS
  }
}

```

B.229.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- VirtualInstruction

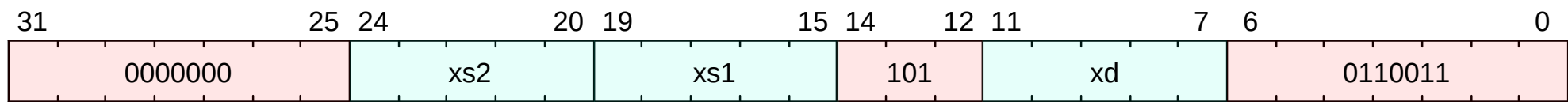
B.230. srl

Shift right logical

This instruction is defined by:

I

B.230.1. Encoding



B.230.2. Description

Logical shift the value in **xs1** right by the value in the lower bits of **xs2**, and store the result in **xd**.

B.230.3. Access

M	S	U
Always	Always	Always

B.230.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.230.5. IDL Operation

```
if (xlen() == 64) {
  X[xd] = X[xs1] >> X[xs2][5:0];
} else {
  X[xd] = X[xs1] >> X[xs2][4:0];
}
```

B.230.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCv_ADD => xs1_val + xs2_val,
    RISCv_SLT => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCv_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCv_AND => xs1_val & xs2_val,
    RISCv_OR => xs1_val | xs2_val,
    RISCv_XOR => xs1_val ^ xs2_val,
    RISCv_SLL => if sizeof(xlen) == 32
      then xs1_val << (xs2_val[4..0])
      else xs1_val << (xs2_val[5..0]),
    RISCv_SRL => if sizeof(xlen) == 32
      then xs1_val >> (xs2_val[4..0])
      else xs1_val >> (xs2_val[5..0]),
    RISCv_SUB => xs1_val - xs2_val,
    RISCv_SRA => if sizeof(xlen) == 32
      then shift_right_arith32(xs1_val, xs2_val[4..0])
      else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.230.7. Exceptions

This instruction does not generate synchronous exceptions.

B.231. srli

Shift right logical immediate

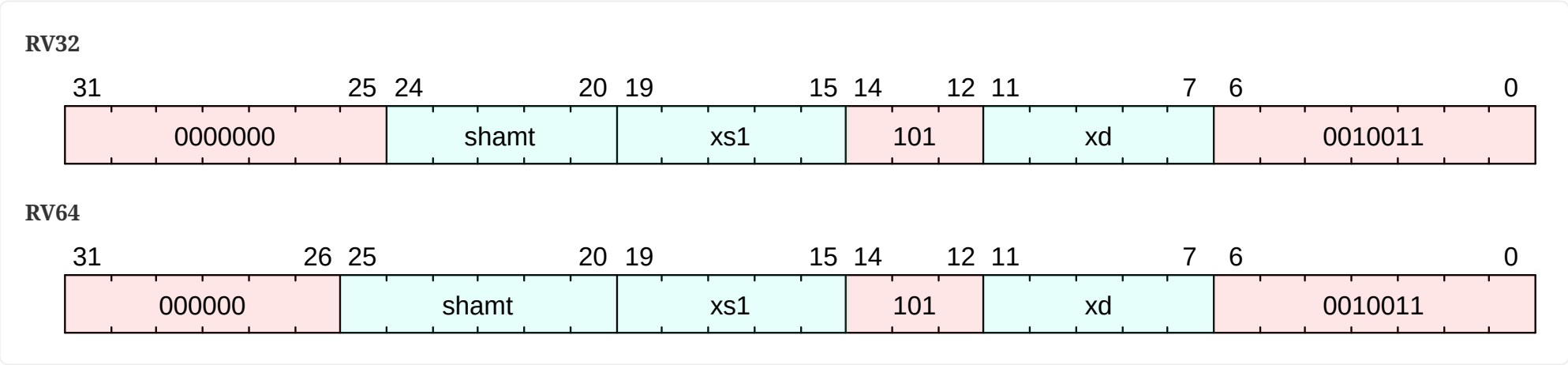
This instruction is defined by:

I

B.231.1. Encoding



This instruction has different encodings in RV32 and RV64.



B.231.2. Description

Shift the value in xs1 right by shamt, and store the result in xd

B.231.3. Access

M	S	U
Always	Always	Always

B.231.4. Decode Variables

RV32

Bits<5> shamt = \$encoding[24:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

RV64

Bits<6> shamt = \$encoding[25:20];

Bits<5> xs1 = \$encoding[19:15];

Bits<5> xd = \$encoding[11:7];

B.231.5. IDL Operation

```
X[xd] = X[xs1] >> shamt;
```

B.231.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  /* the decoder guaxd should ensure that shamt[5] = 0 for RV32 */
  let result : xlenbits = match op {
    RISCV_SLLI => if sizeof(xlen) == 32
      then xs1_val << shamt[4..0]
      else xs1_val << shamt,
    RISCV_SRLI => if sizeof(xlen) == 32
      then xs1_val >> shamt[4..0]
      else xs1_val >> shamt,
    RISCV_SRAI => if sizeof(xlen) == 32
      then shift_right_arith32(xs1_val, shamt[4..0])
      else shift_right_arith64(xs1_val, shamt)
  };
};
```



```
X(xd) = result;  
RETIRE_SUCCESS  
}
```

B.231.7. Exceptions

This instruction does not generate synchronous exceptions.

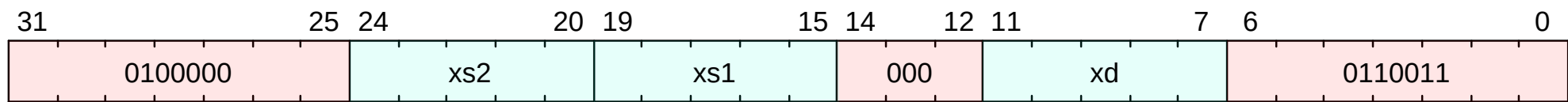
B.232. sub

Subtract

This instruction is defined by:

I

B.232.1. Encoding



B.232.2. Description

Subtract the value in xs2 from xs1, and store the result in xd

B.232.3. Access

M	S	U
Always	Always	Always

B.232.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.232.5. IDL Operation

```
XReg t0 = X[xs1];
XReg t1 = X[xs2];
X[xd] = t0 - t1;
```

B.232.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD  => xs1_val + xs2_val,
    RISCV_SLT  => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND  => xs1_val & xs2_val,
    RISCV_OR   => xs1_val | xs2_val,
    RISCV_XOR  => xs1_val ^ xs2_val,
    RISCV_SLL  => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL  => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB  => xs1_val - xs2_val,
    RISCV_SRA  => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.232.7. Exceptions

This instruction does not generate synchronous exceptions.

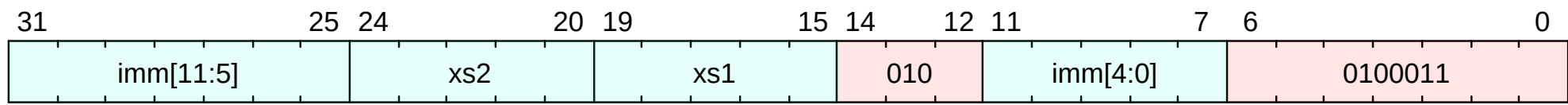
B.233. sw

Store word

This instruction is defined by:

I

B.233.1. Encoding



B.233.2. Description

Store 32 bits of data from register **xs2** to an address formed by adding **xs1** to a signed offset.

B.233.3. Access

M	S	U
Always	Always	Always

B.233.4. Decode Variables

```
Bits<12> imm = {$encoding[31:25], $encoding[11:7]};
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
```

B.233.5. IDL Operation

```
XReg virtual_address = X[xs1] + $signed(imm);
write_memory<32>(virtual_address, X[xs2][31:0], $encoding);
```

B.233.6. Sail Operation

```
{
  let offset : xlenbits = sign_extend(imm);
  /* Get the address, X(xs1) + offset.
     Some extensions perform additional checks on address validity. */
  match ext_data_get_addr(xs1, offset, Write(Data), width) {
    Ext_DataAddr_Error(e) => { ext_handle_data_check_error(e); RETIRE_FAIL },
    Ext_DataAddr_OK(vaddr) =>
      if check_misaligned(vaddr, width)
      then { handle_mem_exception(vaddr, E_SAMO_Addr_Align()); RETIRE_FAIL }
      else match translateAddr(vaddr, Write(Data)) {
        TR_Failure(e, _) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
        TR_Address(paddr, _) => {
          let eares : MemoryOpResult(unit) = match width {
            BYTE => mem_write_ea(paddr, 1, aq, rl, false),
            HALF => mem_write_ea(paddr, 2, aq, rl, false),
            WORD => mem_write_ea(paddr, 4, aq, rl, false),
            DOUBLE => mem_write_ea(paddr, 8, aq, rl, false)
          };
          match (eares) {
            MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL },
            MemValue(_) => {
              let xs2_val = X(xs2);
              let res : MemoryOpResult(bool) = match (width) {
                BYTE => mem_write_value(paddr, 1, xs2_val[7..0], aq, rl, false),
                HALF => mem_write_value(paddr, 2, xs2_val[15..0], aq, rl, false),
                WORD => mem_write_value(paddr, 4, xs2_val[31..0], aq, rl, false),
                DOUBLE if sizeof(xlen) >= 64
                  => mem_write_value(paddr, 8, xs2_val, aq, rl, false),
                _ => report_invalid_width(__FILE__, __LINE__, width, "store"),
              };
              match (res) {
                MemValue(true) => RETIRE_SUCCESS,
                MemValue(false) => internal_error(__FILE__, __LINE__, "store got false from mem_write_value"),
              }
            }
          }
        }
      }
  }
}
```

```
MemException(e) => { handle_mem_exception(vaddr, e); RETIRE_FAIL }  
    }  
    }  
    }  
    }  
    }  
    }
```

B.233.7. Exceptions

This instruction may result in the following synchronous exceptions:

- LoadAccessFault
- StoreAmoAccessFault
- StoreAmoAddressMisaligned
- StoreAmoPageFault

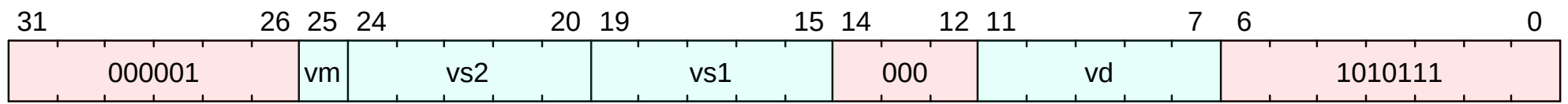
B.234. vandn.vv

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.234.1. Encoding



B.234.2. Description

No description available.

B.234.3. Access

M	S	U
Always	Always	Always

B.234.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.234.5. IDL Operation

B.234.6. Exceptions

This instruction does not generate synchronous exceptions.

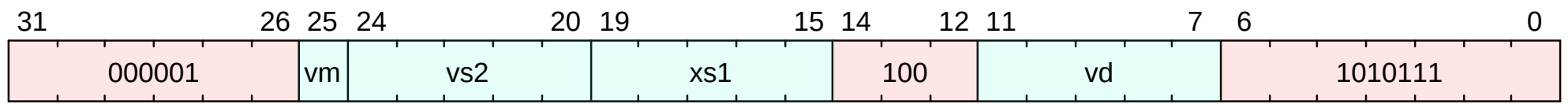
B.235. vandn.vx

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.235.1. Encoding



B.235.2. Description

No description available.

B.235.3. Access

M	S	U
Always	Always	Always

B.235.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.235.5. IDL Operation

B.235.6. Exceptions

This instruction does not generate synchronous exceptions.

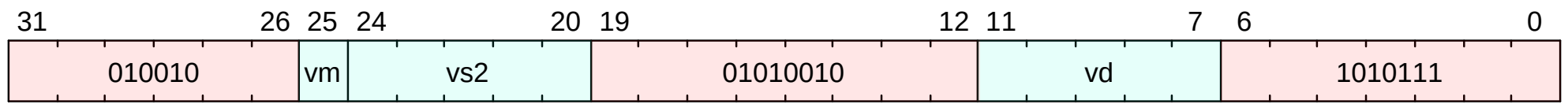
B.236. vbrev.v

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.236.1. Encoding



B.236.2. Description

No description available.

B.236.3. Access

M	S	U
Always	Always	Always

B.236.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.236.5. IDL Operation

B.236.6. Exceptions

This instruction does not generate synchronous exceptions.

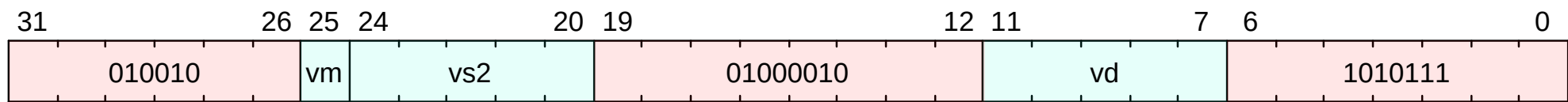
B.237. vbrev8.v

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.237.1. Encoding



B.237.2. Description

No description available.

B.237.3. Access

M	S	U
Always	Always	Always

B.237.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.237.5. IDL Operation

B.237.6. Exceptions

This instruction does not generate synchronous exceptions.

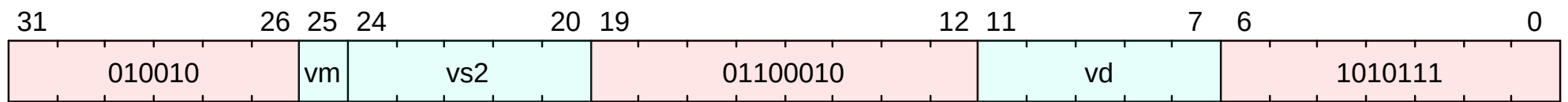
B.238. vclz.v

No synopsis available

This instruction is defined by:

Zvbb

B.238.1. Encoding



B.238.2. Description

No description available.

B.238.3. Access

M	S	U
Always	Always	Always

B.238.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.238.5. IDL Operation

B.238.6. Exceptions

This instruction does not generate synchronous exceptions.

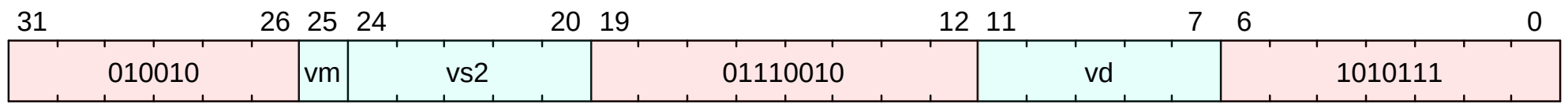
B.239. vcpop.v

No synopsis available

This instruction is defined by:

Zvbb

B.239.1. Encoding



B.239.2. Description

No description available.

B.239.3. Access

M	S	U
Always	Always	Always

B.239.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.239.5. IDL Operation

B.239.6. Exceptions

This instruction does not generate synchronous exceptions.

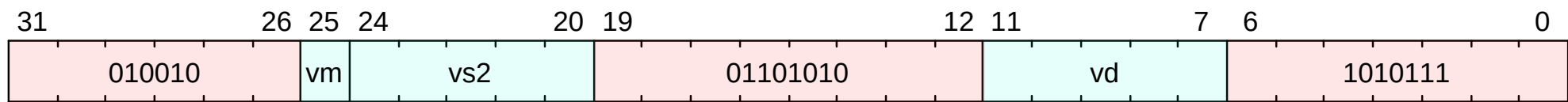
B.240. vctz.v

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.240.1. Encoding



B.240.2. Description

No description available.

B.240.3. Access

M	S	U
Always	Always	Always

B.240.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.240.5. IDL Operation

B.240.6. Exceptions

This instruction does not generate synchronous exceptions.

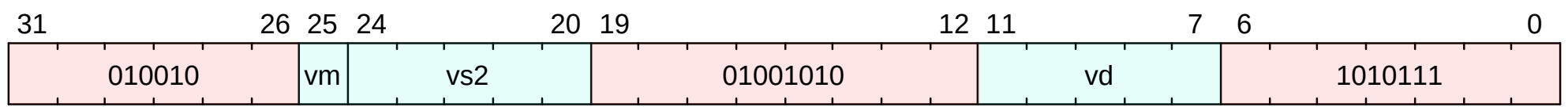
B.241. vrev8.v

No synopsis available

This instruction is defined by:

Zvbb

B.241.1. Encoding



B.241.2. Description

No description available.

B.241.3. Access

M	S	U
Always	Always	Always

B.241.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.241.5. IDL Operation

B.241.6. Exceptions

This instruction does not generate synchronous exceptions.

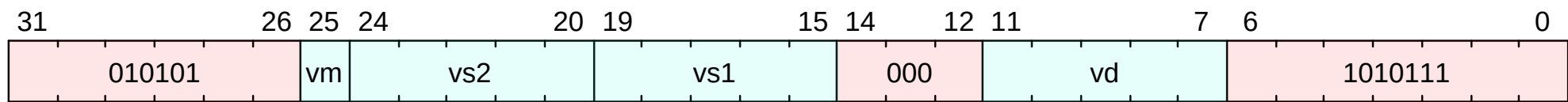
B.242. vrol.vv

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.242.1. Encoding



B.242.2. Description

No description available.

B.242.3. Access

M	S	U
Always	Always	Always

B.242.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.242.5. IDL Operation

B.242.6. Exceptions

This instruction does not generate synchronous exceptions.

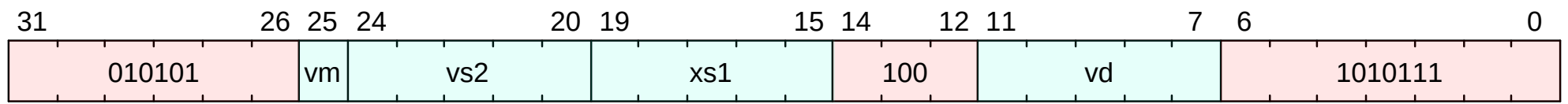
B.243. vrol.vx

No synopsis available

This instruction is defined by:

Zvbb

B.243.1. Encoding



B.243.2. Description

No description available.

B.243.3. Access

M	S	U
Always	Always	Always

B.243.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.243.5. IDL Operation

B.243.6. Exceptions

This instruction does not generate synchronous exceptions.

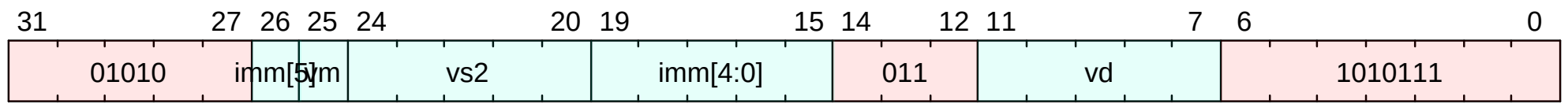
B.244. vror.vi

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.244.1. Encoding



B.244.2. Description

No description available.

B.244.3. Access

M	S	U
Always	Always	Always

B.244.4. Decode Variables

```
Bits<6> imm = {$encoding[26], $encoding[19:15]};
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vd = $encoding[11:7];
```

B.244.5. IDL Operation

B.244.6. Exceptions

This instruction does not generate synchronous exceptions.

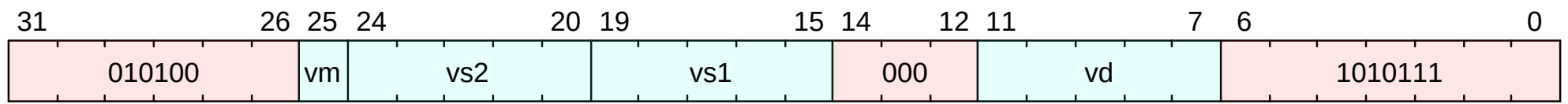
B.245. vror.vv

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.245.1. Encoding



B.245.2. Description

No description available.

B.245.3. Access

M	S	U
Always	Always	Always

B.245.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.245.5. IDL Operation

B.245.6. Exceptions

This instruction does not generate synchronous exceptions.

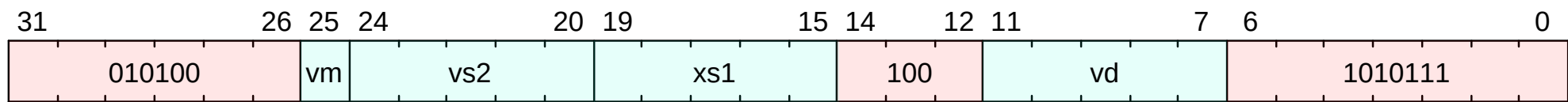
B.246. vror.vx

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.246.1. Encoding



B.246.2. Description

No description available.

B.246.3. Access

M	S	U
Always	Always	Always

B.246.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.246.5. IDL Operation

B.246.6. Exceptions

This instruction does not generate synchronous exceptions.

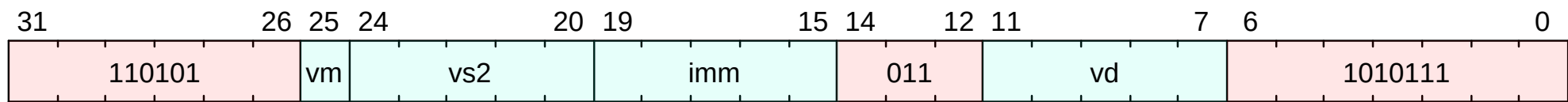
B.247. vwsll.vi

No synopsis available

This instruction is defined by:

[Zvbb](#)

B.247.1. Encoding



B.247.2. Description

No description available.

B.247.3. Access

M	S	U
Always	Always	Always

B.247.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> imm = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.247.5. IDL Operation

B.247.6. Exceptions

This instruction does not generate synchronous exceptions.

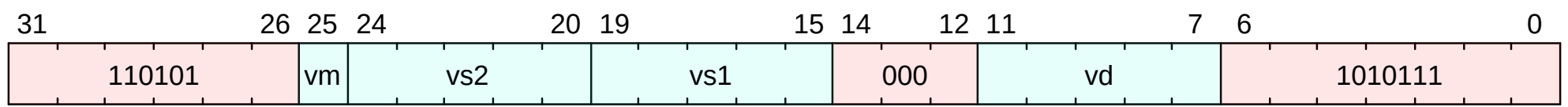
B.248. vwsll.vv

No synopsis available

This instruction is defined by:

Zvbb

B.248.1. Encoding



B.248.2. Description

No description available.

B.248.3. Access

M	S	U
Always	Always	Always

B.248.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> vs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.248.5. IDL Operation

B.248.6. Exceptions

This instruction does not generate synchronous exceptions.

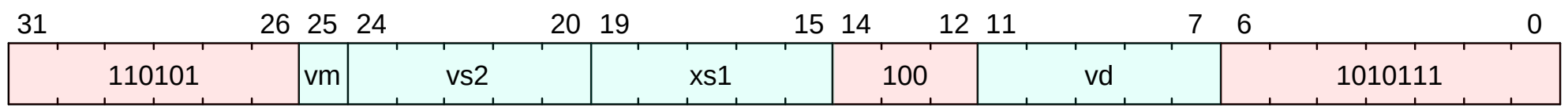
B.249. vwsll.vx

No synopsis available

This instruction is defined by:

Zvbb

B.249.1. Encoding



B.249.2. Description

No description available.

B.249.3. Access

M	S	U
Always	Always	Always

B.249.4. Decode Variables

```
Bits<1> vm = $encoding[25];
Bits<5> vs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> vd = $encoding[11:7];
```

B.249.5. IDL Operation

B.249.6. Exceptions

This instruction does not generate synchronous exceptions.

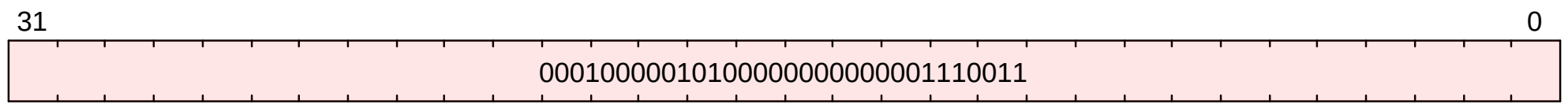
B.250. wfi

Wait for interrupt

This instruction is defined by:

Sm

B.250.1. Encoding



B.250.2. Description

Can causes the processor to enter a low-power state until the next interrupt occurs.

<%- if ext?:(H) -%> The behavior of wfi is affected by the mstatus.TW and hstatus.VTW bits, as summarized below.

mstatus.TW	hstatus.VTW	wfi behavior			
		HS-mode	U-mode	VS-mode	in VU-mode
0	0	Wait	Trap (I)	Wait	Trap (V)
0	1	Wait	Trap (I)	Trap (V)	Trap (V)
1	-	Trap (I)	Trap (I)	Trap (I)	Trap (I)
Trap (I) - Trap with Illegal Instruction code					
Trap (V) - Trap with Virtual Instruction code					

<%- else -%> The wfi instruction is also affected by mstatus.TW, as shown below:

mstatus.TW	wfi behavior	
	S-mode	U-mode
0	Wait	Trap (I)
1	Trap (I)	Trap (I)
Trap (I) - Trap with Illegal Instruction code		

<%- end -%>

When wfi is marked as causing a trap above, the implementation is allowed to wait for an unspecified period of time to see if an interrupt occurs before raising the trap. That period of time can be zero (i.e., wfi always causes a trap in the cases identified above).

B.250.3. Access

M	S	U
Always	Sometimes	Sometimes

<%- if ext?:(H) -%> The behavior of wfi is affected by the mstatus.TW and hstatus.VTW bits, as summarized below.

mstatus.TW	hstatus.VTW	wfi behavior			
		HS-mode	U-mode	VS-mode	in VU-mode
0	0	Wait	Trap (I)	Wait	Trap (V)
0	1	Wait	Trap (I)	Trap (V)	Trap (V)
1	-	Trap (I)	Trap (I)	Trap (I)	Trap (I)
Trap (I) - Trap with Illegal Instruction code					
Trap (V) - Trap with Virtual Instruction code					

<%- else -%> The wfi instruction is also affected by mstatus.TW, as shown below:

mstatus.TW	wfi behavior	
	S-mode	U-mode
0	Wait	Trap (I)
1	Trap (I)	Trap (I)
Trap (I) - Trap with Illegal Instruction code		

B.250.4. Decode Variables



B.250.5. IDL Operation

```
if (mode() == PrivilegeMode::U) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
if ((CSR[misa].S == 1) && (CSR[mstatus].TW == 1'b1)) {
  if (mode() != PrivilegeMode::M) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
if (CSR[misa].H == 1) {
  if (CSR[hstatus].VTW == 1'b0) {
    if (mode() == PrivilegeMode::VU) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  } else if (CSR[hstatus].VTW == 1'b1) {
    if ((mode() == PrivilegeMode::VS) || (mode() == PrivilegeMode::VU)) {
      raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    }
  }
}
}
wfi();
```

B.250.6. Sail Operation

```
match cur_privilege {
  Machine    => { platform_wfi(); RETIRE_SUCCESS },
  Supervisor => if mstatus.TW() == 0b1
                 then { handle_illegal(); RETIRE_FAIL }
                 else { platform_wfi(); RETIRE_SUCCESS },
  User       => { handle_illegal(); RETIRE_FAIL }
}
```

B.250.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction
- VirtualInstruction

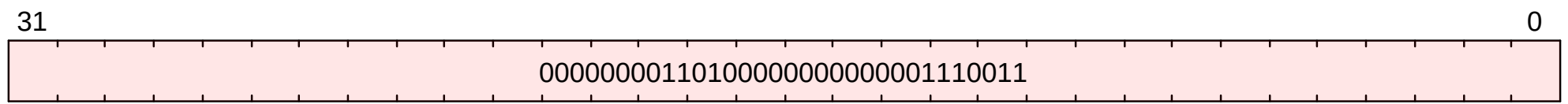
B.251. wrs.nto

Wait-on-Reservation-Set-with-No-Timeout

This instruction is defined by:

Zawrs

B.251.1. Encoding



B.251.2. Description

To mitigate the wasteful looping in such usages, a [wrs.nto](#) (WRS-with-no-timeout) instruction is provided. Instead of polling for a store to a specific memory location, software registers a reservation set that includes all the bytes of the memory location using the LR instruction. Then a subsequent [wrs.nto](#) instruction would cause the hart to temporarily stall execution in a low-power state until a store occurs to the reservation set or an interrupt is observed.

This instruction is not supported in a constrained LR/SC loop. While stalled, an implementation is permitted to occasionally terminate the stall and complete execution for any reason.

[wrs.nto](#) follows the rules of the WFI instruction for resuming execution on a pending interrupt.

When the TW (Timeout Wait) bit in [mstatus](#) is set and [wrs.nto](#) is executed in any privilege mode otherthan M mode, and it does not complete within an implementation-specific bounded time limit, the [wrs.nto](#) instruction will cause an illegal instruction exception.

When executing in VS or VU mode, if the VTW bit is set in [hstatus](#), the TW bit in [mstatus](#) is clear, and the [wrs.nto](#) does not complete within an implementation-specific bounded time limit, the [wrs.nto](#) instruction will cause a virtual instruction exception.

Since [wrs.nto](#) can complete execution for reasons other than stores to the reservation set, software will likely need a means of looping until the required stores have occurred.

[wrs.nto](#), unlike WFI, is not specified to cause an illegal instruction exception if executed in U-mode when the governing TW bit is 0. WFI is typically not expected to be used in U-mode and on many systems may promptly cause an illegal instruction exception if used at U-mode. Unlike WFI, [wrs.nto](#) is expected to be used by software in U-mode when waiting on memory but without a deadline for that wait.

B.251.3. Access

M	S	U
Always	Always	Always

B.251.4. Decode Variables

B.251.5. IDL Operation

B.251.6. Exceptions

This instruction does not generate synchronous exceptions.

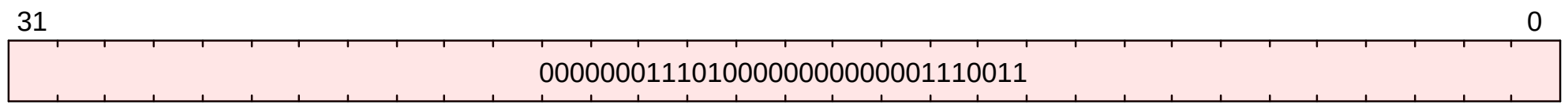
B.252. wrs.sto

Wait-on-Reservation-Set-with-Short-Timeout

This instruction is defined by:

Zawrs

B.252.1. Encoding



B.252.2. Description

Instead of polling for a store to a specific memory location, software registers a reservation set that includes all the bytes of the memory location using the LR instruction. A subsequent [wrs.sto](#) instruction would cause the hart to temporarily stall execution in a low-power state until a store occurs to the reservation set or an interrupt is observed. Sometimes the program waiting on a memory update may also need to carry out a task at a future time or otherwise place an upper bound on the wait. To support such use cases, [wrs.sto](#) bounds the stall duration to an implementation-define short timeout such that the stall is terminated on the timeout if no other conditions have occurred to terminate the stall. The program using this instruction may then determine if its deadline has been reached. [wrs.sto](#) causes the hart to temporarily stall execution in a low-power state as long as the reservation set is valid and no pending interrupts, even if disabled, are observed. For [wrs.sto](#) the stall duration is bounded by an implementation defined short timeout. These instructions are not supported in a constrained LR/SC loop. Hart execution may be stalled while the following conditions are all satisfied: a. The reservation set is valid b. If [wrs.sto](#), a "short" duration since start of stall has not elapsed c. No pending interrupt is observed (see the rules below)

While stalled, an implementation is permitted to occasionally terminate the stall and complete execution for any reason. [wrs.sto](#) follows the rules of the WFI instruction for resuming execution on a pending interrupt. Since [wrs.sto](#) can complete execution for reasons other than stores to the reservation set, software will likely need a means of looping until the required stores have occurred.

The duration of a [wrs.sto](#) instruction’s timeout may vary significantly within and among implementations. In typical implementations this duration should be roughly in the range of 10 to 100 times an on-chip cache miss latency or a cacheless access to main memory.

B.252.3. Access

M	S	U
Always	Always	Always

B.252.4. Decode Variables

B.252.5. IDL Operation

B.252.6. Exceptions

This instruction does not generate synchronous exceptions.

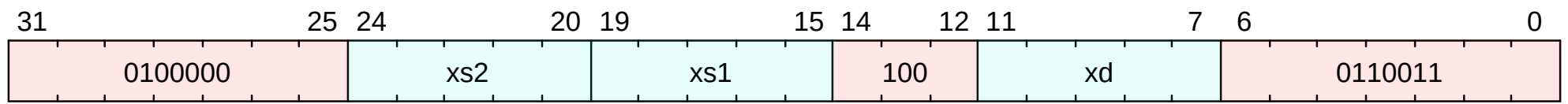
B.253. xnor

Exclusive NOR

This instruction is defined by:

([Zbb](#) || [Zbkb](#))

B.253.1. Encoding



B.253.2. Description

Performs the bit-wise exclusive-NOR operation on xs1 and xs2.

B.253.3. Access

M	S	U
Always	Always	Always

B.253.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.253.5. IDL Operation

```
if (implemented?(ExtensionName::B) && (CSR[misa].B == 1'b0)) {
  raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
}
X[xd] = ~(X[xs1] ^ X[xs2]);
```

B.253.6. Sail Operation

```
{
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  let result : xlenbits = match op {
    RISCV_ANDN => rs1_val & ~(rs2_val),
    RISCV_ORN  => rs1_val | ~(rs2_val),
    RISCV_XNOR => ~(rs1_val ^ rs2_val),
    RISCV_MAX  => to_bits(sizeof(xlen), max(signed(rs1_val), signed(rs2_val))),
    RISCV_MAXU => to_bits(sizeof(xlen), max(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_MIN  => to_bits(sizeof(xlen), min(signed(rs1_val), signed(rs2_val))),
    RISCV_MINU => to_bits(sizeof(xlen), min(unsigned(rs1_val), unsigned(rs2_val))),
    RISCV_ROL  => if sizeof(xlen) == 32
                  then rs1_val <<< rs2_val[4..0]
                  else rs1_val <<< rs2_val[5..0],
    RISCV_ROR  => if sizeof(xlen) == 32
                  then rs1_val >>> rs2_val[4..0]
                  else rs1_val >>> rs2_val[5..0]
  };
  X(rd) = result;
  RETIRE_SUCCESS
}
```

B.253.7. Exceptions

This instruction may result in the following synchronous exceptions:

- IllegalInstruction

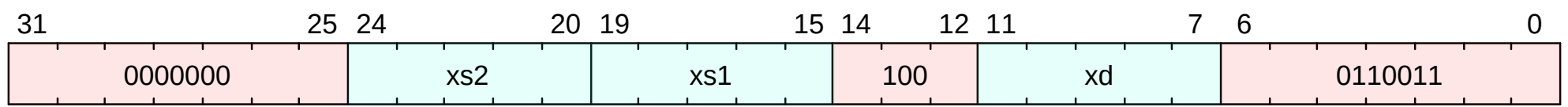
B.254. xor

Exclusive Or

This instruction is defined by:

I

B.254.1. Encoding



B.254.2. Description

Exclusive or xs1 with xs2, and store the result in xd

B.254.3. Access

M	S	U
Always	Always	Always

B.254.4. Decode Variables

```
Bits<5> xs2 = $encoding[24:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.254.5. IDL Operation

```
X[xd] = X[xs1] ^ X[xs2];
```

B.254.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let xs2_val = X(xs2);
  let result : xlenbits = match op {
    RISCV_ADD  => xs1_val + xs2_val,
    RISCV_SLT  => zero_extend(bool_to_bits(xs1_val <_s xs2_val)),
    RISCV_SLTU => zero_extend(bool_to_bits(xs1_val <_u xs2_val)),
    RISCV_AND  => xs1_val & xs2_val,
    RISCV_OR   => xs1_val | xs2_val,
    RISCV_XOR  => xs1_val ^ xs2_val,
    RISCV_SLL  => if sizeof(xlen) == 32
                  then xs1_val << (xs2_val[4..0])
                  else xs1_val << (xs2_val[5..0]),
    RISCV_SRL  => if sizeof(xlen) == 32
                  then xs1_val >> (xs2_val[4..0])
                  else xs1_val >> (xs2_val[5..0]),
    RISCV_SUB  => xs1_val - xs2_val,
    RISCV_SRA  => if sizeof(xlen) == 32
                  then shift_right_arith32(xs1_val, xs2_val[4..0])
                  else shift_right_arith64(xs1_val, xs2_val[5..0])
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.254.7. Exceptions

This instruction does not generate synchronous exceptions.

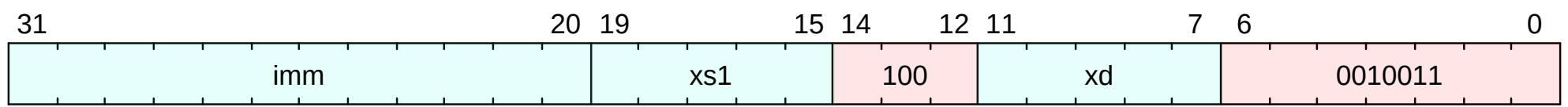
B.255. xori

Exclusive Or immediate

This instruction is defined by:

I

B.255.1. Encoding



B.255.2. Description

Exclusive or an immediate to the value in xs1, and store the result in xd

B.255.3. Access

M	S	U
Always	Always	Always

B.255.4. Decode Variables

```
Bits<12> imm = $encoding[31:20];
Bits<5> xs1 = $encoding[19:15];
Bits<5> xd = $encoding[11:7];
```

B.255.5. IDL Operation

```
X[xd] = X[xs1] ^ $signed(imm);
```

B.255.6. Sail Operation

```
{
  let xs1_val = X(xs1);
  let immext : xlenbits = sign_extend(imm);
  let result : xlenbits = match op {
    RISCV_ADDI => xs1_val + immext,
    RISCV_SLTI => zero_extend(bool_to_bits(xs1_val <_s immext)),
    RISCV_SLTIU => zero_extend(bool_to_bits(xs1_val <_u immext)),
    RISCV_ANDI => xs1_val & immext,
    RISCV_ORI  => xs1_val | immext,
    RISCV_XORI => xs1_val ^ immext
  };
  X(xd) = result;
  RETIRE_SUCCESS
}
```

B.255.7. Exceptions

This instruction does not generate synchronous exceptions.

Appendix C: CSR Details

C.1. cycle

Cycle counter for RDCYCLE Instruction

Alias for M-mode CSR [mcycle](#).

Privilege mode access is controlled with [mcounteren.CY](#), [scounteren.CY](#), and [hcounteren.CY](#) as follows:

mcounteren.CY	scounteren.CY	hcounteren.CY	cycle behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

C.1.1. Attributes

CSR Address	0xc00
Defining extension	Zicntr
Length	64-bit
Privilege Mode	U

C.1.2. Format

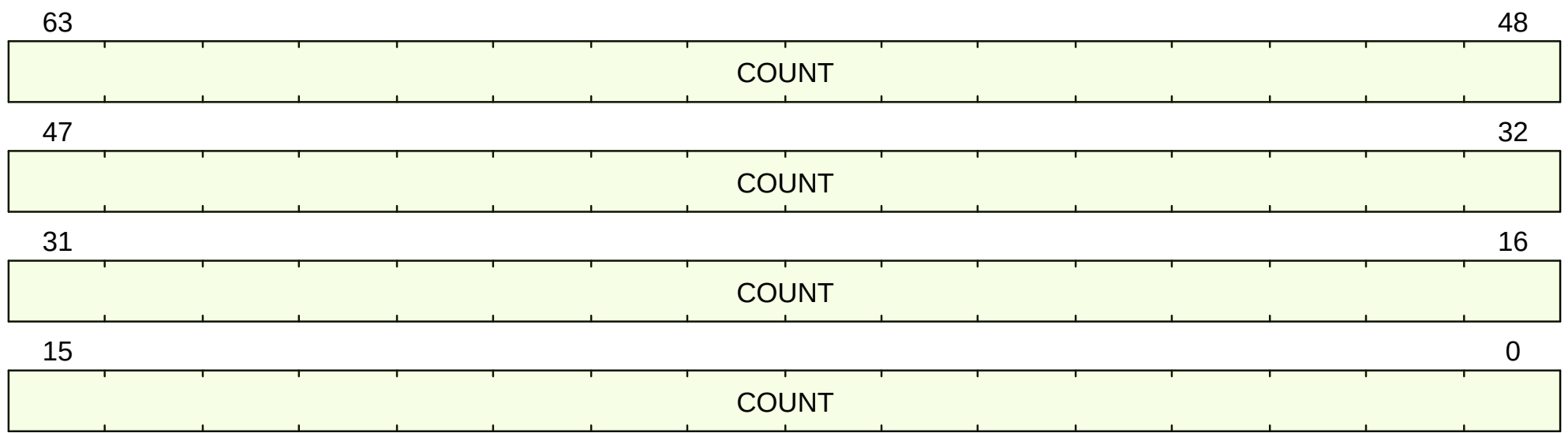


Figure 1. cycle format

C.1.3. Field Summary

Nam e	Location	Type	Reset Value
cycle.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.1.4. Fields

[cycle.COUNT](#) Field

Location:
63:0

Description:
Alias of [mcycle.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.1.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].CY == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].CY & CSR[scounteren].CY) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].CY == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].CY == 1'b0 && CSR[mcounteren].CY == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].CY == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].CY & CSR[scounteren].CY == 1'b0) && (CSR[mcounteren].CY == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].CY == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_mcycle();
```


C.2. fcsr

Floating-point control and status register (frm + fflags)

The floating-point control and status register, `fcsr`, is a RISC-V control and status register (CSR). It is a 32-bit read/write register that selects the dynamic rounding mode for floating-point arithmetic operations and holds the accrued exception flags, as shown in [Floating-Point Control and Status Register](#).

Floating-point control and status register

Unresolved directive in AC200-CRD.adoc - include::images/wavedrom/float-csr.adoc[]

The `fcsr` register can be read and written with the `FRCSR` and `FSCSR` instructions, which are assembler pseudoinstructions built on the underlying CSR access instructions. `FRCSR` reads `fcsr` by copying it into integer register `rd`. `FSCSR` swaps the value in `fcsr` by copying the original value into integer register `rd`, and then writing a new value obtained from integer register `rs1` into `fcsr`.

The fields within the `fcsr` can also be accessed individually through different CSR addresses, and separate assembler pseudoinstructions are defined for these accesses. The `FRRM` instruction reads the Rounding Mode field `frm` (`fcsr` bits 7—5) and copies it into the least-significant three bits of integer register `rd`, with zero in all other bits. `FSRM` swaps the value in `frm` by copying the original value into integer register `rd`, and then writing a new value obtained from the three least-significant bits of integer register `rs1` into `frm`. `FRFLAGS` and `FSFLAGS` are defined analogously for the Accrued Exception Flags field `fflags` (`fcsr` bits 4—0).

Bits 31—8 of the `fcsr` are reserved for other standard extensions. If these extensions are not present, implementations shall ignore writes to these bits and supply a zero value when read. Standard software should preserve the contents of these bits.

Floating-point operations use either a static rounding mode encoded in the instruction, or a dynamic rounding mode held in `frm`. Rounding modes are encoded as shown in [Table 7](#). A value of 111 in the instruction’s `rm` field selects the dynamic rounding mode held in `frm`. The behavior of floating-point instructions that depend on rounding mode when executed with a reserved rounding mode is *reserved*, including both static reserved rounding modes (101-110) and dynamic reserved rounding modes (101-111). Some instructions, including widening conversions, have the `rm` field but are nevertheless mathematically unaffected by the rounding mode; software should set their `rm` field to RNE (000) but implementations must treat the `rm` field as usual (in particular, with regard to decoding legal vs. reserved encodings).



The C99 language standard effectively mandates the provision of a dynamic rounding mode register. In typical implementations, writes to the dynamic rounding mode CSR state will serialize the pipeline. Static rounding modes are used to implement specialized arithmetic operations that often have to switch frequently between different rounding modes.

The ratified version of the F spec mandated that an illegal-instruction exception was raised when an instruction was executed with a reserved dynamic rounding mode. This has been weakened to reserved, which matches the behavior of static rounding-mode instructions. Raising an illegal-instruction exception is still valid behavior when encountering a reserved encoding, so implementations compatible with the ratified spec are compatible with the weakened spec.

The accrued exception flags indicate the exception conditions that have arisen on any floating-point arithmetic instruction since the field was last reset by software, as shown in [Table 8](#). The base RISC-V ISA does not support generating a trap on the setting of a floating-point exception flag.

Table 20. Accrued exception flag encoding.

Flag Mnemonic	Flag Meaning
NV	Invalid Operation
DZ	Divide by Zero
OF	Overflow
UF	Underflow
NX	Inexact



As allowed by the standard, we do not support traps on floating-point exceptions in the F extension, but instead require explicit checks of the flags in software. We considered adding branches controlled directly by the contents of the floating-point accrued exception flags, but ultimately chose to omit these instructions to keep the ISA simple.

C.2.1. Attributes

CSR Address	0x3
Defining extension	F
Length	32-bit
Privilege Mode	U

C.2.2. Format

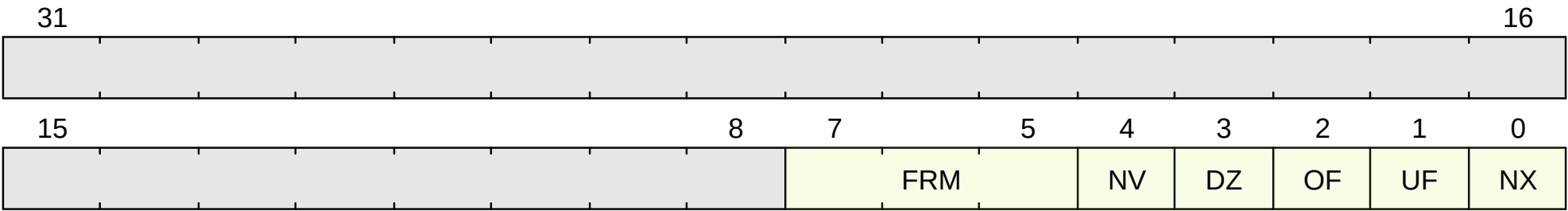


Figure 2. fcsr format

C.2.3. Field Summary

Na me	Location	Type	Reset Value
fcsr.FRM	7:5	RW-H	UNDEFINED_LEGAL
fcsr.NV	4	RW-H	UNDEFINED_LEGAL
fcsr.DZ	3	RW-H	UNDEFINED_LEGAL
fcsr.OF	2	RW-H	UNDEFINED_LEGAL
fcsr.UF	1	RW-H	UNDEFINED_LEGAL
fcsr.NX	0	RW-H	UNDEFINED_LEGAL

C.2.4. Fields

[fcsr.FRM](#) Field

Location:

7:5

Description:

Rounding modes are encoded as follows:

.Rounding mode encoding.
[%autowidth,float="center",align="center",cols="",<","options="header"]
!===
!Rounding Mode |Mnemonic |Meaning
!000 !RNE !Round to Nearest, ties to Even
!001 !RTZ !Round towards Zero
!010 !RDN !Round Down (towards -∞)
!011 !RUP !Round Up (towards +∞)
!100 !RMM !Round to Nearest, ties to Max Magnitude
!101 ! *!Reserved for future use.*
!110 ! *!Reserved for future use.*
!111 !DYN !In instruction’s *rm* field, selects dynamic rounding mode; In Rounding Mode register, *reserved*.
!===

A value of 111 in the instruction’s *rm* field selects the dynamic rounding mode held in [frm](#). The behavior of floating-point instructions that depend on rounding mode when executed with a reserved rounding mode is *reserved*, including both static reserved rounding modes (101-110) and dynamic reserved rounding modes (101-111). Some instructions, including widening conversions, have the *rm* field but are nevertheless mathematically unaffected by the rounding mode; software should set their *rm* field to RNE (000) but implementations must treat the *rm* field as usual (in particular, with regard to decoding legal vs. reserved encodings).

Type:

RW-H

Reset value:
UNDEFINED_LEGAL

fcsr.NV Field

Location:
4

Description:
Invalid Operation

Cumulative error flag for floating point operations.

Set by hardware when a floating point operation is invalid and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fcsr.DZ Field

Location:
3

Description:
Divide by zero

Cumulative error flag for floating point operations.

Set by hardware when a floating point divide attempts to divide by zero and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fcsr.OF Field

Location:
2

Description:
Overflow

Cumulative error flag for floating point operations.

Set by hardware when a floating point operation overflows and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fcsr.UF Field

Location:
1

Description:

Underflow

Cumulative error flag for floating point operations.

Set by hardware when a floating point operation underflows and stays set until explicitly cleared by software.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

fcsr.NX Field

Location:

0

Description:

Inexact

Cumulative error flag for floating point operations.

Set by hardware when a floating point operation is inexact and stays set until explicitly cleared by software.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

C.3. fflags

Floating-Point Accrued Exceptions

The accrued exception flags indicate the exception conditions that have arisen on any floating-point arithmetic instruction since the field was last reset by software.

The base RISC-V ISA does not support generating a trap on the setting of a floating-point exception flag.

As allowed by the standard, we do not support traps on floating-point exceptions in the F extension, but instead require explicit checks of the flags in software. We considered adding branches controlled directly by the contents of the floating-point accrued exception flags, but ultimately chose to omit these instructions to keep the ISA simple.

C.3.1. Attributes

CSR Address	0x1
Defining extension	F
Length	32-bit
Privilege Mode	U

C.3.2. Format

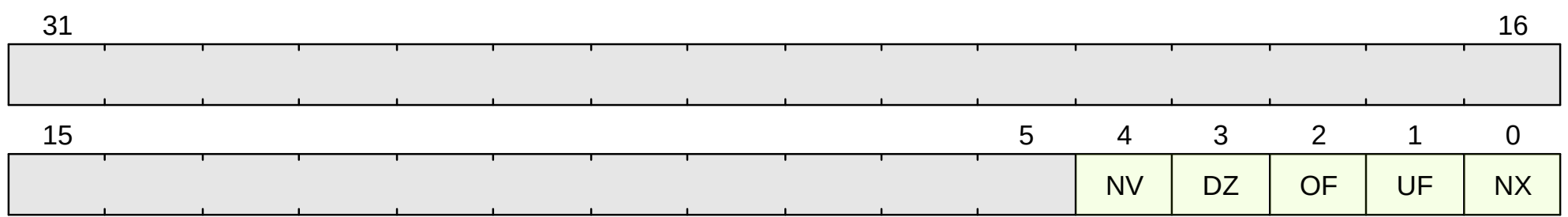


Figure 3. fflags format

C.3.3. Field Summary

Na me	Location	Type	Reset Value
fflags.NV	4	RW-H	UNDEFINED_LEGAL
fflags.DZ	3	RW-H	UNDEFINED_LEGAL
fflags.OF	2	RW-H	UNDEFINED_LEGAL
fflags.UF	1	RW-H	UNDEFINED_LEGAL
fflags.NX	0	RW-H	UNDEFINED_LEGAL

C.3.4. Fields

[fflags.NV](#) Field

Location:
4

Description:
Set by hardware when a floating point operation is invalid and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fflags.DZ Field

Location:
3

Description:
Set by hardware when a floating point divide attempts to divide by zero and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fflags.OF Field

Location:
2

Description:
Set by hardware when a floating point operation overflows and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fflags.UF Field

Location:
1

Description:
Set by hardware when a floating point operation underflows and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

fflags.NX Field

Location:
0

Description:
Set by hardware when a floating point operation is inexact and stays set until explicitly cleared by software.

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

C.3.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
NV = CSR[fcsr].NV = csr_value.NV;
return csr_value.NV;

DZ = CSR[fcsr].DZ = csr_value.DZ;
return csr_value.DZ;

OF = CSR[fcsr].OF = csr_value.OF;
return csr_value.OF;

UF = CSR[fcsr].UF = csr_value.UF;
return csr_value.UF;

NX = CSR[fcsr].NX = csr_value.NX;
return csr_value.NX;
```

C.3.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return (CSR[fcsr].NV << 4) | (CSR[fcsr].DZ << 3) | (CSR[fcsr].OF << 2) | (CSR[fcsr].UF << 1) | CSR[fcsr].NX;
```

C.4. frm

Floating-Point Dynamic Rounding Mode

Rounding modes are encoded as follows:

Table 21. Rounding mode encoding.

!Rounding Mode	Mnemon ic	Meaning !000 !RNE !Round to Nearest, ties to Even !001 !RTZ !Round towards Zero !010 !RDN !Round Down (towards -\infty) !011 !RUP !Round Up (towards +\infty) !100 !RMM !Round to Nearest, ties to Max Magnitude !101 ! !Reserved for future use. !110 ! !Reserved for future use. !111 !DYN !In instruction’s <i>rm</i> field, selects dynamic rounding mode; In Rounding Mode register, reserved.

The behavior of floating-point instructions that depend on rounding mode when executed with a reserved rounding mode is *reserved*, including both static reserved rounding modes (101-110) and dynamic reserved rounding modes (101-111).

Some instructions, including widening conversions, have the *rm* field but are nevertheless mathematically unaffected by the rounding mode; software should set their *rm* field to RNE (000) but implementations must treat the *rm* field as usual (in particular, with regard to decoding legal vs. reserved encodings).

C.4.1. Attributes

CSR Address	0x2
Defining extension	F
Length	32-bit
Privilege Mode	U

C.4.2. Format



Figure 4. *frm* format

C.4.3. Field Summary

Name	Location	Type	Reset Value
frm.RO UNDIN GMODE	2:0	RW-H	UNDEFINED_LEGAL

C.4.4. Fields

frm.ROUNDINGMODE Field

Location:

2:0

Description:

Rounding mode data.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

C.4.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through `csrrw`), the following determines the written value:


```
ROUNDINGMODE = CSR[fcsr].FRM = csr_value.ROUNDINGMODE;  
return csr_value.ROUNDINGMODE;
```

C.4.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return CSR[fcsr].FRM;
```

C.5. hpmcounter10

User-mode Hardware Performance Counter 7

Alias for M-mode CSR [mhpmcounter10](#).

Privilege mode access is controlled with [mcounteren.HPM10](#) <%- if ext?:(S) -%> , [scounteren.HPM10](#) <%- if ext?:(H) -%> , and [hcounteren.HPM10](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM10	scounteren.HPM10	hcounteren.HPM10	hpmcounter10 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM10	scounteren.HPM10	hpmcounter10 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM10	hpmcounter10 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.5.1. Attributes

CSR Address	0xc0a
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.5.2. Format

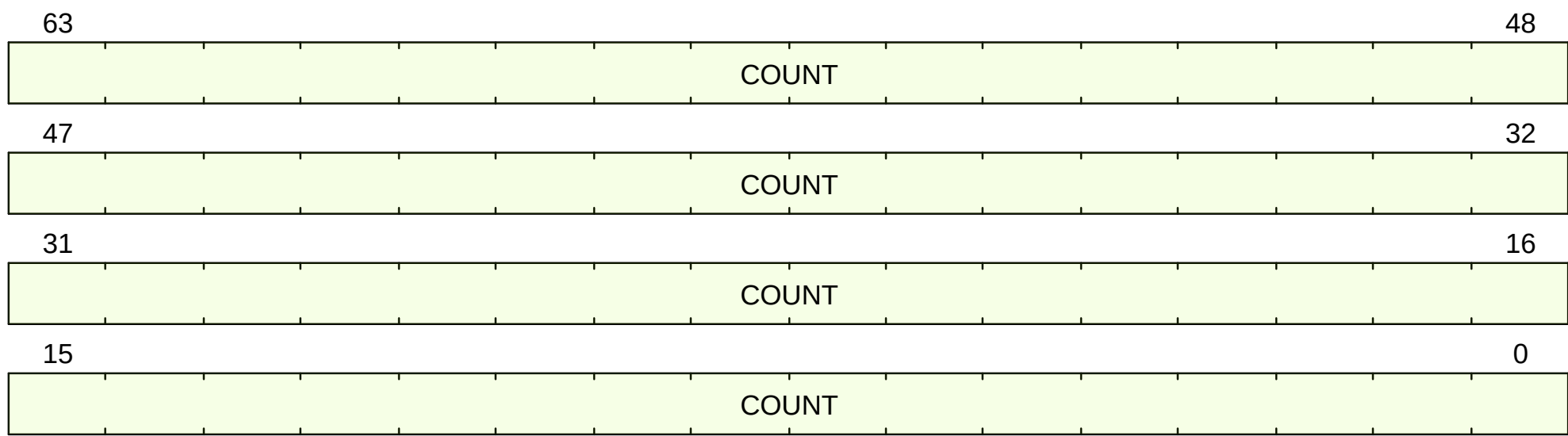


Figure 5. *hpmcounter10* format

C.5.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter10.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.5.4. Fields

hpmcounter10.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter10.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.5.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM10 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM10 & CSR[scounteren].HPM10) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM10 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM10 == 1'b0 && CSR[mcounteren].HPM10 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM10 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM10 & CSR[scounteren].HPM10) == 1'b0 && (CSR[mcounteren].HPM10 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM10 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(10);
```

C.6. hpmcounter11

User-mode Hardware Performance Counter 8

Alias for M-mode CSR [mhpmcounter11](#).

Privilege mode access is controlled with [mcounteren.HPM11](#) <%- if ext?(:S) -%> , [scounteren.HPM11](#) <%- if ext?(:H) -%> , and [hcounteren.HPM11](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM11	scounteren.HPM11	hcounteren.HPM11	hpmcounter11 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM11	scounteren.HPM11	hpmcounter11 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM11	hpmcounter11 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.6.1. Attributes

CSR Address	0xc0b
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.6.2. Format

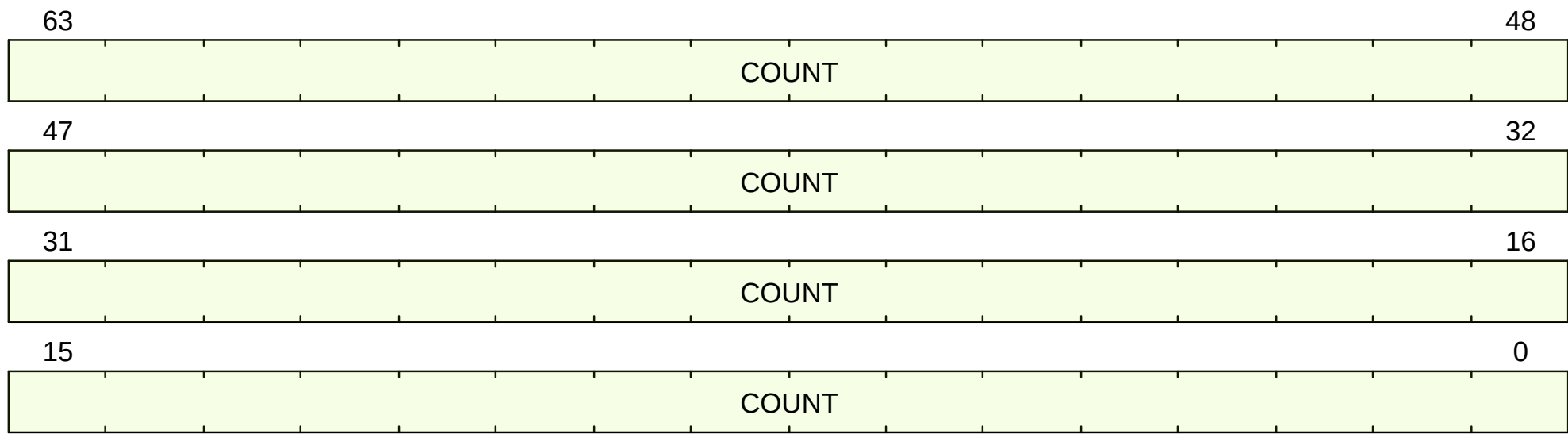


Figure 6. hpmcounter11 format

C.6.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter11.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.6.4. Fields

hpmcounter11.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter11.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.6.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM11 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM11 & CSR[scounteren].HPM11) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM11 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM11 == 1'b0 && CSR[mcounteren].HPM11 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM11 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM11 & CSR[scounteren].HPM11) == 1'b0 && (CSR[mcounteren].HPM11 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM11 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(11);
```

C.7. hpmcounter12

User-mode Hardware Performance Counter 9

Alias for M-mode CSR [mhpmcounter12](#).

Privilege mode access is controlled with [mcounteren.HPM12](#) <%- if ext?:(S) -%> , [scounteren.HPM12](#) <%- if ext?:(H) -%> , and [hcounteren.HPM12](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM12	scounteren.HPM12	hcounteren.HPM12	hpmcounter12 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM12	scounteren.HPM12	hpmcounter12 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM12	hpmcounter12 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.7.1. Attributes

CSR Address	0xc0c
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.7.2. Format

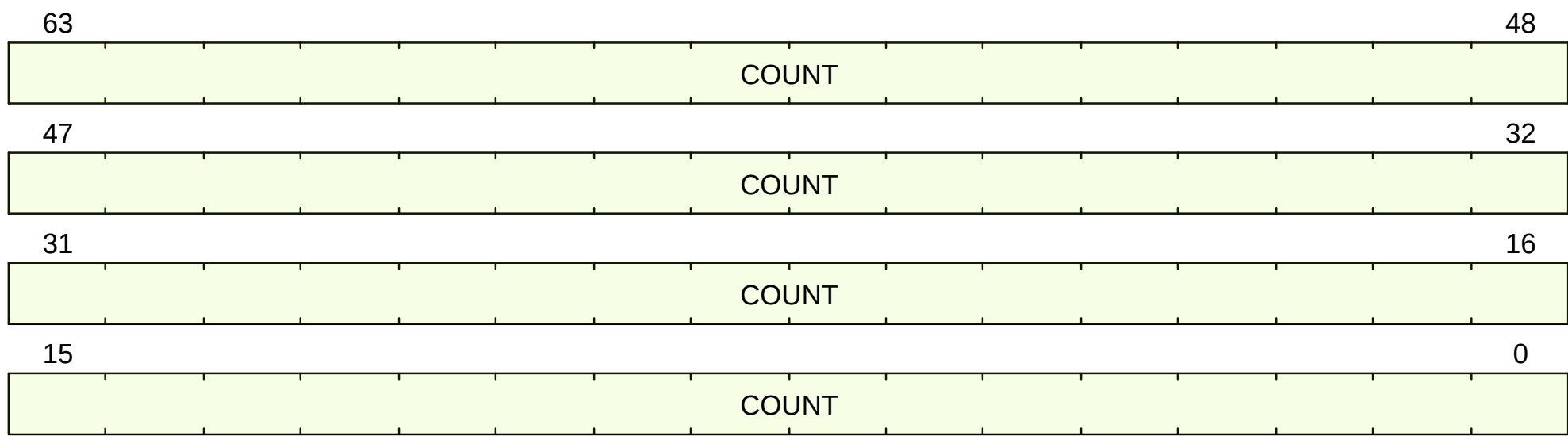


Figure 7. *hpmcounter12* format

C.7.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter12.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.7.4. Fields

hpmcounter12.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter12.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.7.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM12 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM12 & CSR[scounteren].HPM12) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM12 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM12 == 1'b0 && CSR[mcounteren].HPM12 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM12 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM12 & CSR[scounteren].HPM12) == 1'b0 && (CSR[mcounteren].HPM12 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM12 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(12);
```

C.8. hpmcounter13

User-mode Hardware Performance Counter 10

Alias for M-mode CSR [mhpmcounter13](#).

Privilege mode access is controlled with [mcounteren.HPM13](#) <%- if ext?(:S) -%> , [scounteren.HPM13](#) <%- if ext?(:H) -%> , and [hcounteren.HPM13](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM13	scounteren.HPM13	hcounteren.HPM13	hpmcounter13 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM13	scounteren.HPM13	hpmcounter13 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM13	hpmcounter13 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.8.1. Attributes

CSR Address	0xc0d
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.8.2. Format

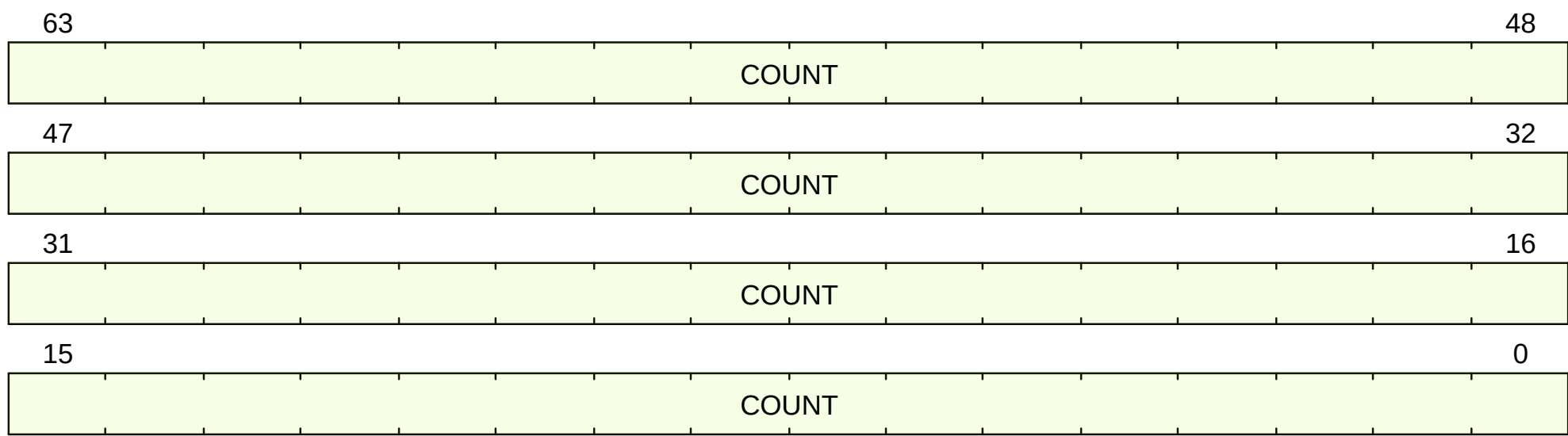


Figure 8. hpmcounter13 format

C.8.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter13.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.8.4. Fields

hpmcounter13.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter13.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.8.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM13 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM13 & CSR[scounteren].HPM13) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM13 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM13 == 1'b0 && CSR[mcounteren].HPM13 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM13 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM13 & CSR[scounteren].HPM13) == 1'b0 && (CSR[mcounteren].HPM13 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM13 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(13);
```

C.9. hpmcounter14

User-mode Hardware Performance Counter 11

Alias for M-mode CSR [mhpmcounter14](#).

Privilege mode access is controlled with [mcounteren.HPM14](#) <%- if ext?:(S) -%> , [scounteren.HPM14](#) <%- if ext?:(H) -%> , and [hcounteren.HPM14](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM14	scounteren.HPM14	hcounteren.HPM14	hpmcounter14 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM14	scounteren.HPM14	hpmcounter14 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM14	hpmcounter14 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.9.1. Attributes

CSR Address	0xc0e
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.9.2. Format

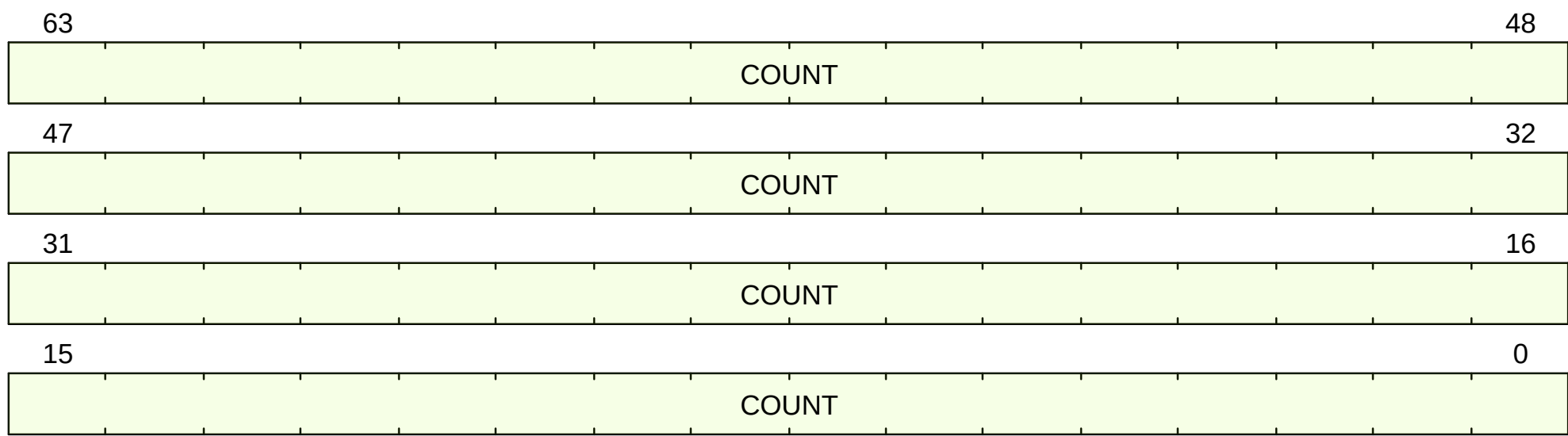


Figure 9. hpmcounter14 format

C.9.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter14.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.9.4. Fields

hpmcounter14.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter14.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.9.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM14 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM14 & CSR[scounteren].HPM14) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM14 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM14 == 1'b0 && CSR[mcounteren].HPM14 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM14 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM14 & CSR[scounteren].HPM14) == 1'b0 && (CSR[mcounteren].HPM14 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM14 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(14);
```

C.10. hpmcounter15

User-mode Hardware Performance Counter 12

Alias for M-mode CSR [mhpmcounter15](#).

Privilege mode access is controlled with [mcounteren.HPM15](#) <%- if ext?:(S) -%> , [scounteren.HPM15](#) <%- if ext?:(H) -%> , and [hcounteren.HPM15](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM15	scounteren.HPM15	hcounteren.HPM15	hpmcounter15 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM15	scounteren.HPM15	hpmcounter15 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM15	hpmcounter15 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.10.1. Attributes

CSR Address	0xc0f
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.10.2. Format

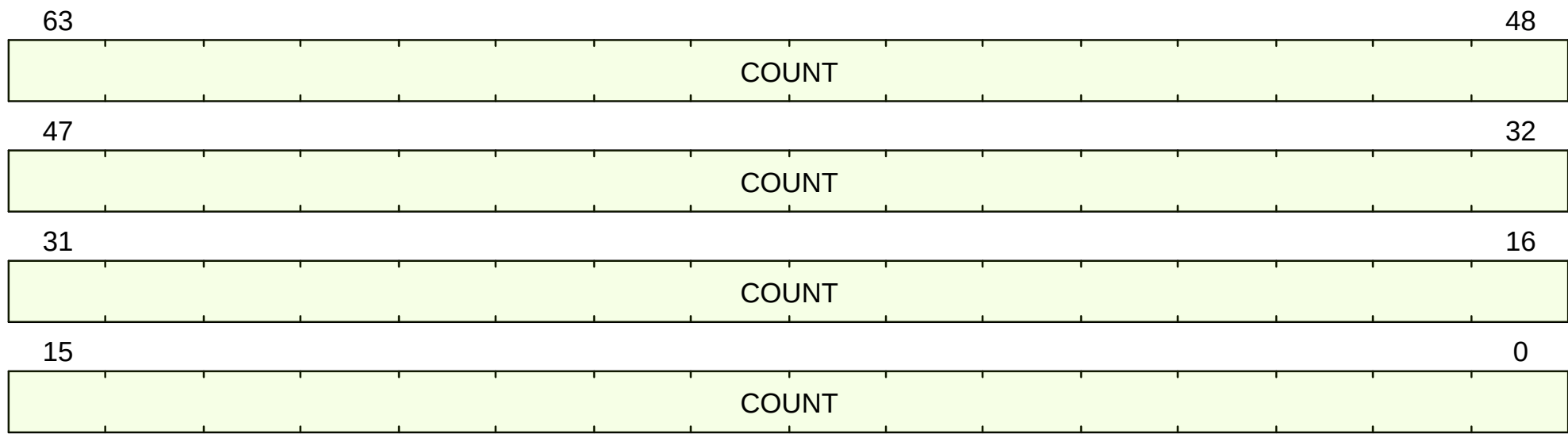


Figure 10. hpmcounter15 format

C.10.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter15.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.10.4. Fields

hpmcounter15.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter15.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.10.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM15 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM15 & CSR[scounteren].HPM15) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM15 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM15 == 1'b0 && CSR[mcounteren].HPM15 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM15 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM15 & CSR[scounteren].HPM15) == 1'b0 && (CSR[mcounteren].HPM15 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM15 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(15);
```

C.11. hpmcounter16

User-mode Hardware Performance Counter 13

Alias for M-mode CSR [mhpmcounter16](#).

Privilege mode access is controlled with [mcounteren.HPM16](#) <%- if ext?:(S) -%> , [scounteren.HPM16](#) <%- if ext?:(H) -%> , and [hcounteren.HPM16](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM16	scounteren.HPM16	hcounteren.HPM16	hpmcounter16 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM16	scounteren.HPM16	hpmcounter16 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM16	hpmcounter16 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.11.1. Attributes

CSR Address	0xc10
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.11.2. Format

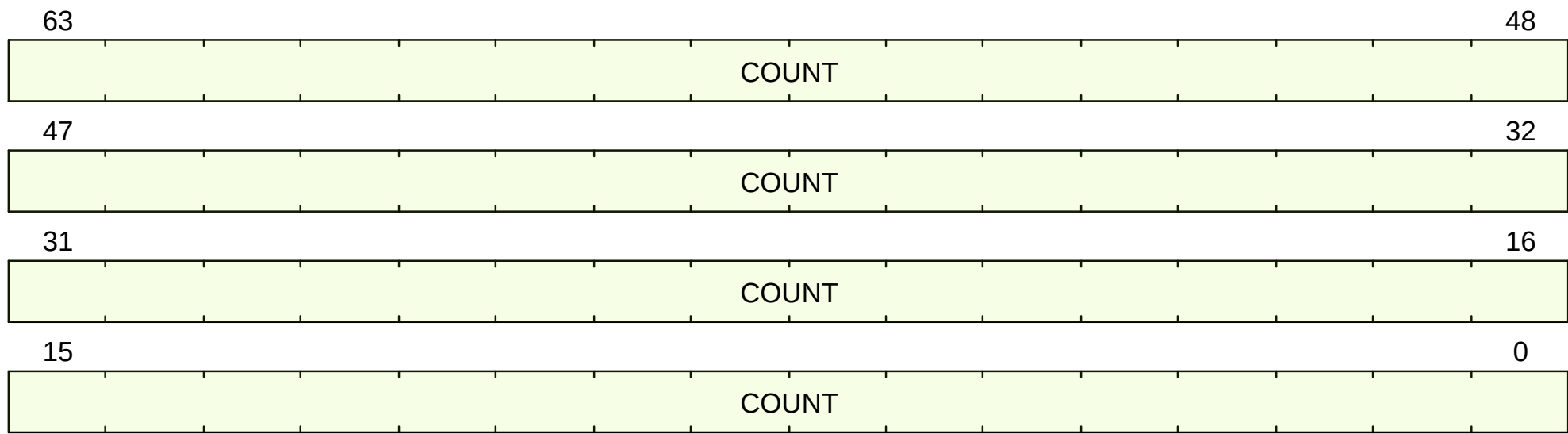


Figure 11. hpmcounter16 format

C.11.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter16.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.11.4. Fields

hpmcounter16.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter16.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.11.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM16 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM16 & CSR[scounteren].HPM16) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM16 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM16 == 1'b0 && CSR[mcounteren].HPM16 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM16 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM16 & CSR[scounteren].HPM16) == 1'b0 && (CSR[mcounteren].HPM16 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM16 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(16);
```

C.12. hpmcounter17

User-mode Hardware Performance Counter 14

Alias for M-mode CSR [mhpmcounter17](#).

Privilege mode access is controlled with [mcounteren.HPM17](#) <%- if ext?(:S) -%> , [scounteren.HPM17](#) <%- if ext?(:H) -%> , and [hcounteren.HPM17](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM17	scounteren.HPM17	hcounteren.HPM17	hpmcounter17 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM17	scounteren.HPM17	hpmcounter17 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM17	hpmcounter17 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.12.1. Attributes

CSR Address	0xc11
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.12.2. Format

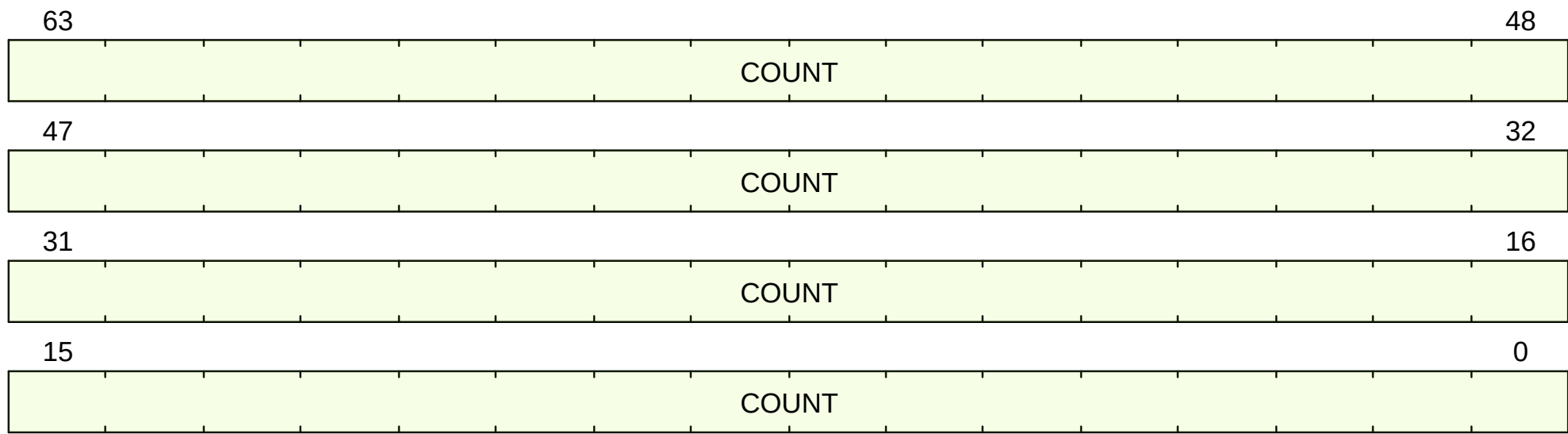


Figure 12. hpmcounter17 format

C.12.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter17.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.12.4. Fields

hpmcounter17.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter17.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.12.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM17 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM17 & CSR[scounteren].HPM17) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM17 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM17 == 1'b0 && CSR[mcounteren].HPM17 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM17 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM17 & CSR[scounteren].HPM17) == 1'b0 && (CSR[mcounteren].HPM17 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM17 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(17);
```

C.13. hpmcounter18

User-mode Hardware Performance Counter 15

Alias for M-mode CSR [mhpmcounter18](#).

Privilege mode access is controlled with [mcounteren.HPM18](#) <%- if ext?:(S) -%> , [scounteren.HPM18](#) <%- if ext?:(H) -%> , and [hcounteren.HPM18](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM18	scounteren.HPM18	hcounteren.HPM18	hpmcounter18 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM18	scounteren.HPM18	hpmcounter18 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM18	hpmcounter18 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.13.1. Attributes

CSR Address	0xc12
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.13.2. Format

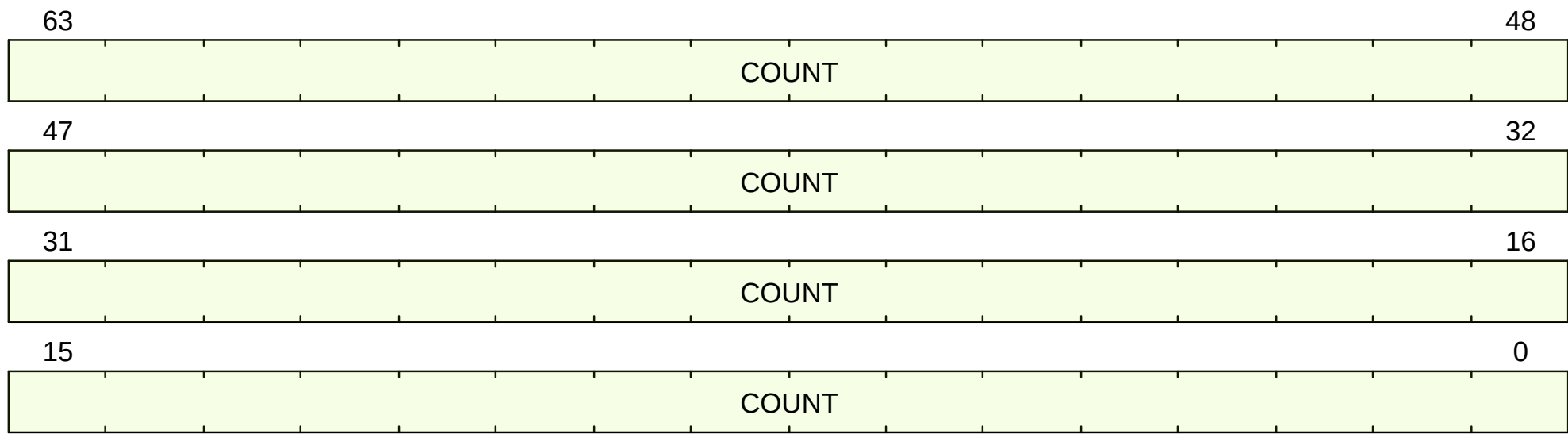


Figure 13. hpmcounter18 format

C.13.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter18.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.13.4. Fields

hpmcounter18.COUNT Field

Location:
63:0

Description:
Alias of mhpmcounter18.COUNT.

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.13.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM18 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM18 & CSR[scounteren].HPM18) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM18 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM18 == 1'b0 && CSR[mcounteren].HPM18 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM18 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM18 & CSR[scounteren].HPM18) == 1'b0 && (CSR[mcounteren].HPM18 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM18 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(18);
```

C.14. hpmcounter19

User-mode Hardware Performance Counter 16

Alias for M-mode CSR [mhpmcounter19](#).

Privilege mode access is controlled with [mcounteren.HPM19](#) <%- if ext?:(S) -%> , [scounteren.HPM19](#) <%- if ext?:(H) -%> , and [hcounteren.HPM19](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM19	scounteren.HPM19	hcounteren.HPM19	hpmcounter19 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM19	scounteren.HPM19	hpmcounter19 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM19	hpmcounter19 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.14.1. Attributes

CSR Address	0xc13
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.14.2. Format

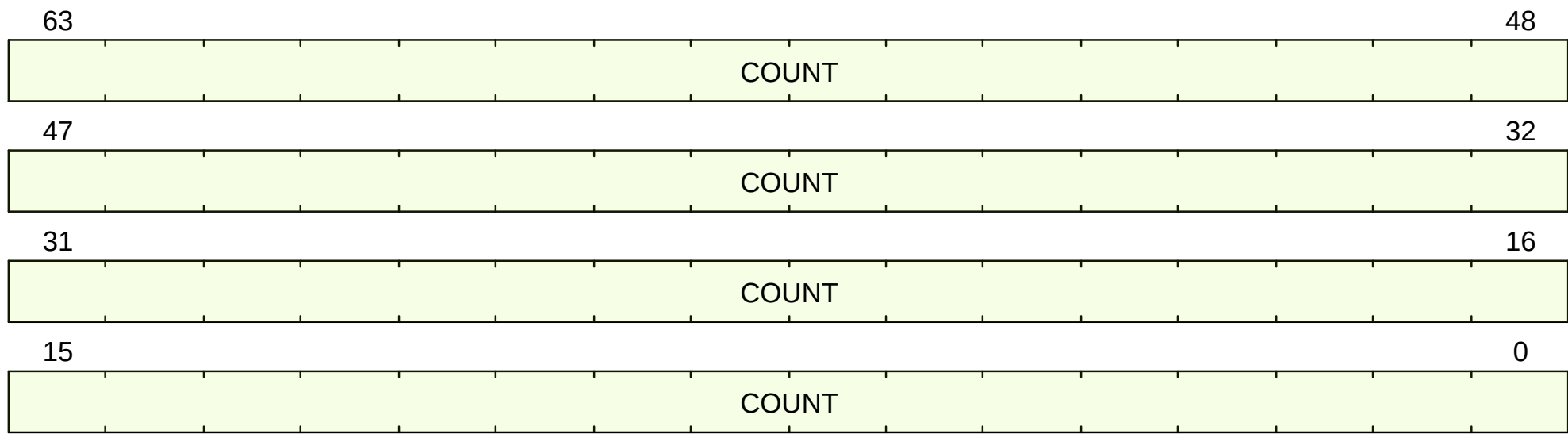


Figure 14. hpmcounter19 format

C.14.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter19.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.14.4. Fields

hpmcounter19.COUNT Field

Location:

63:0

Description:

Alias of [mhpmcounter19.COUNT](#).

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

C.14.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM19 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM19 & CSR[scounteren].HPM19) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM19 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM19 == 1'b0 && CSR[mcounteren].HPM19 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM19 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM19 & CSR[scounteren].HPM19) == 1'b0 && (CSR[mcounteren].HPM19 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM19 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(19);
```

C.15. hpmcounter20

User-mode Hardware Performance Counter 17

Alias for M-mode CSR [mhpmcounter20](#).

Privilege mode access is controlled with [mcounteren.HPM20](#) <%- if ext?:(S) -%> , [scounteren.HPM20](#) <%- if ext?:(H) -%> , and [hcounteren.HPM20](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM20	scounteren.HPM20	hcounteren.HPM20	hpmcounter20 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM20	scounteren.HPM20	hpmcounter20 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM20	hpmcounter20 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.15.1. Attributes

CSR Address	0xc14
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.15.2. Format

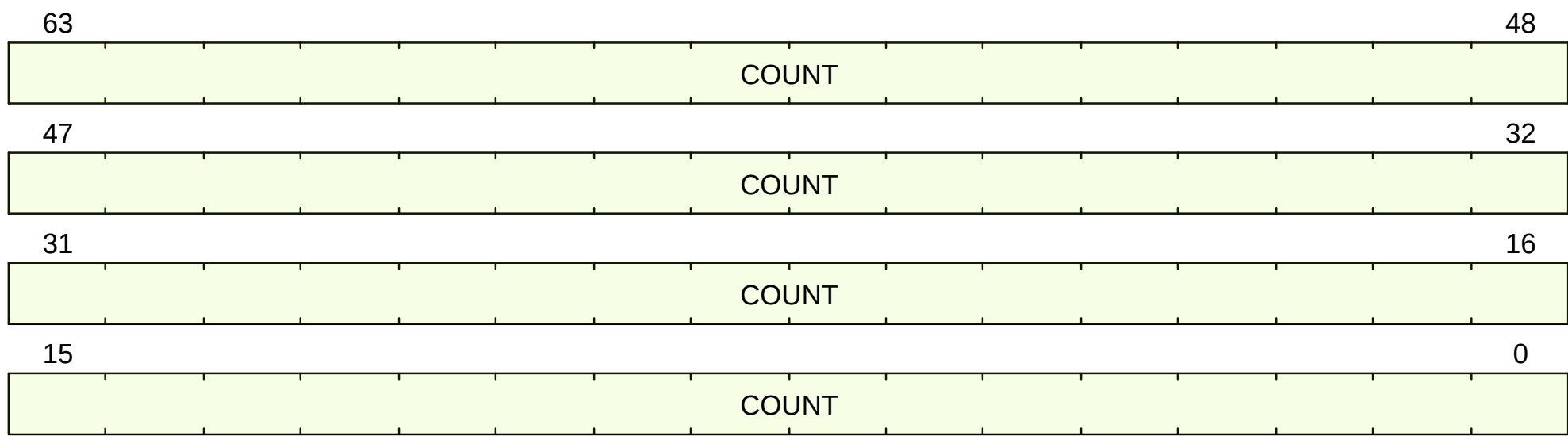


Figure 15. hpmcounter20 format

C.15.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter20.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.15.4. Fields

hpmcounter20.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter20.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.15.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM20 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM20 & CSR[scounteren].HPM20) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM20 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM20 == 1'b0 && CSR[mcounteren].HPM20 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM20 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM20 & CSR[scounteren].HPM20) == 1'b0 && (CSR[mcounteren].HPM20 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM20 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(20);
```

C.16. hpmcounter21

User-mode Hardware Performance Counter 18

Alias for M-mode CSR [mhpmcounter21](#).

Privilege mode access is controlled with [mcounteren.HPM21](#) <%- if ext?(:S) -%> , [scounteren.HPM21](#) <%- if ext?(:H) -%> , and [hcounteren.HPM21](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM21	scounteren.HPM21	hcounteren.HPM21	hpmcounter21 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM21	scounteren.HPM21	hpmcounter21 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM21	hpmcounter21 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.16.1. Attributes

CSR Address	0xc15
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.16.2. Format

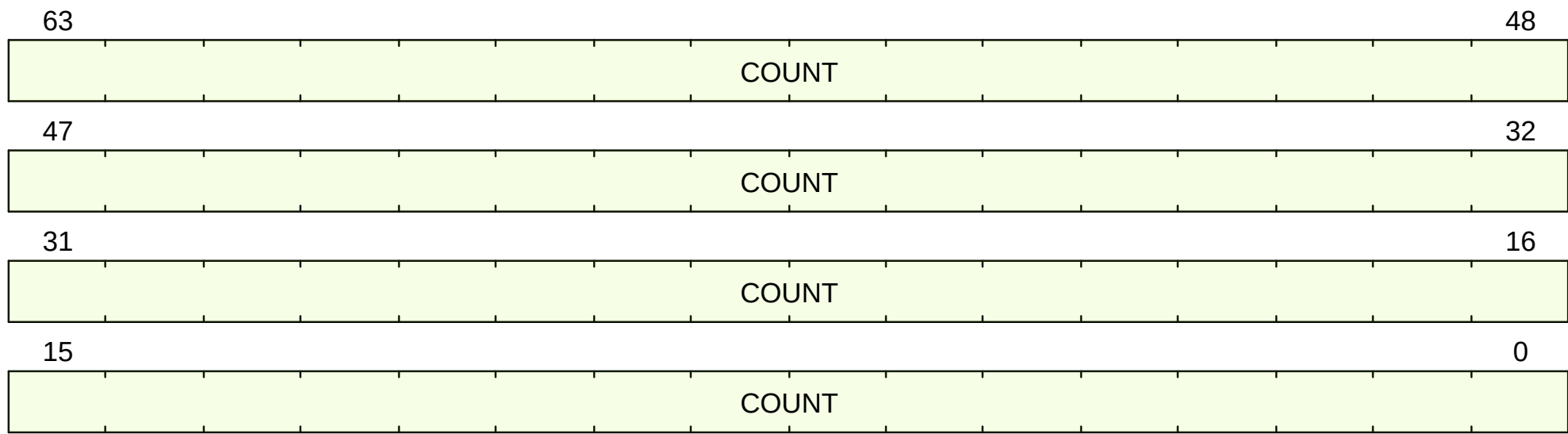


Figure 16. hpmcounter21 format

C.16.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter21.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.16.4. Fields

hpmcounter21.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter21.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.16.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM21 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM21 & CSR[scounteren].HPM21) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM21 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM21 == 1'b0 && CSR[mcounteren].HPM21 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM21 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM21 & CSR[scounteren].HPM21) == 1'b0 && (CSR[mcounteren].HPM21 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM21 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(21);
```

C.17. hpmcounter22

User-mode Hardware Performance Counter 19

Alias for M-mode CSR [mhpmcounter22](#).

Privilege mode access is controlled with [mcounteren.HPM22](#) <%- if ext?:(S) -%> , [scounteren.HPM22](#) <%- if ext?:(H) -%> , and [hcounteren.HPM22](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM22	scounteren.HPM22	hcounteren.HPM22	hpmcounter22 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM22	scounteren.HPM22	hpmcounter22 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM22	hpmcounter22 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.17.1. Attributes

CSR Address	0xc16
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.17.2. Format

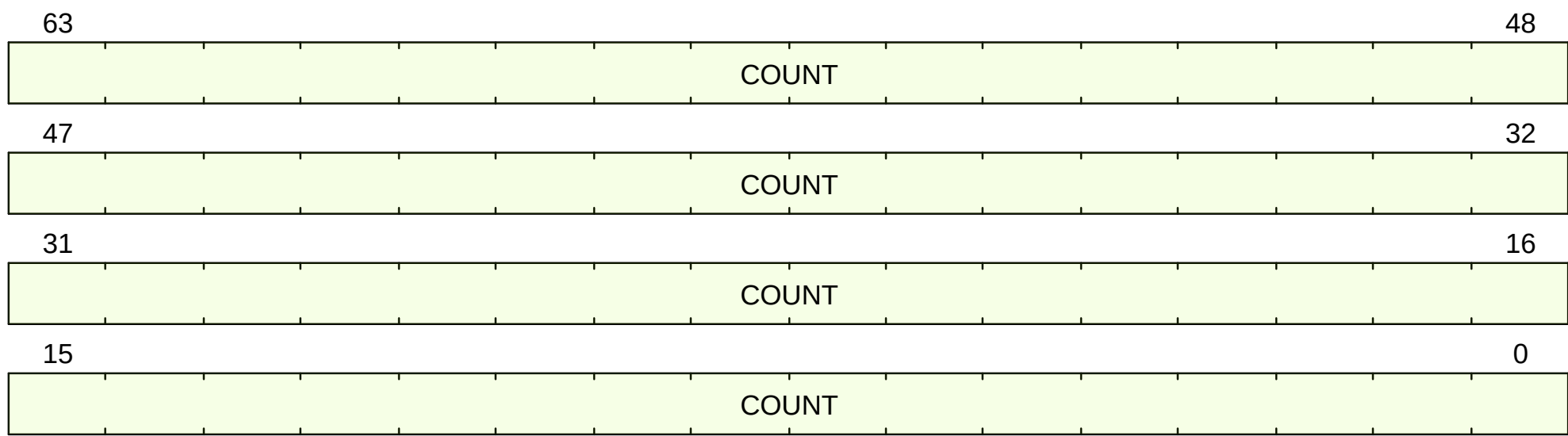


Figure 17. hpmcounter22 format

C.17.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter22.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.17.4. Fields

hpmcounter22.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter22.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.17.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM22 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM22 & CSR[scounteren].HPM22) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM22 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM22 == 1'b0 && CSR[mcounteren].HPM22 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM22 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM22 & CSR[scounteren].HPM22) == 1'b0 && (CSR[mcounteren].HPM22 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM22 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(22);
```

C.18. hpmcounter23

User-mode Hardware Performance Counter 20

Alias for M-mode CSR [mhpmcounter23](#).

Privilege mode access is controlled with [mcounteren.HPM23](#) <%- if ext?:(S) -%> , [scounteren.HPM23](#) <%- if ext?:(H) -%> , and [hcounteren.HPM23](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM23	scounteren.HPM23	hcounteren.HPM23	hpmcounter23 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM23	scounteren.HPM23	hpmcounter23 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM23	hpmcounter23 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.18.1. Attributes

CSR Address	0xc17
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.18.2. Format

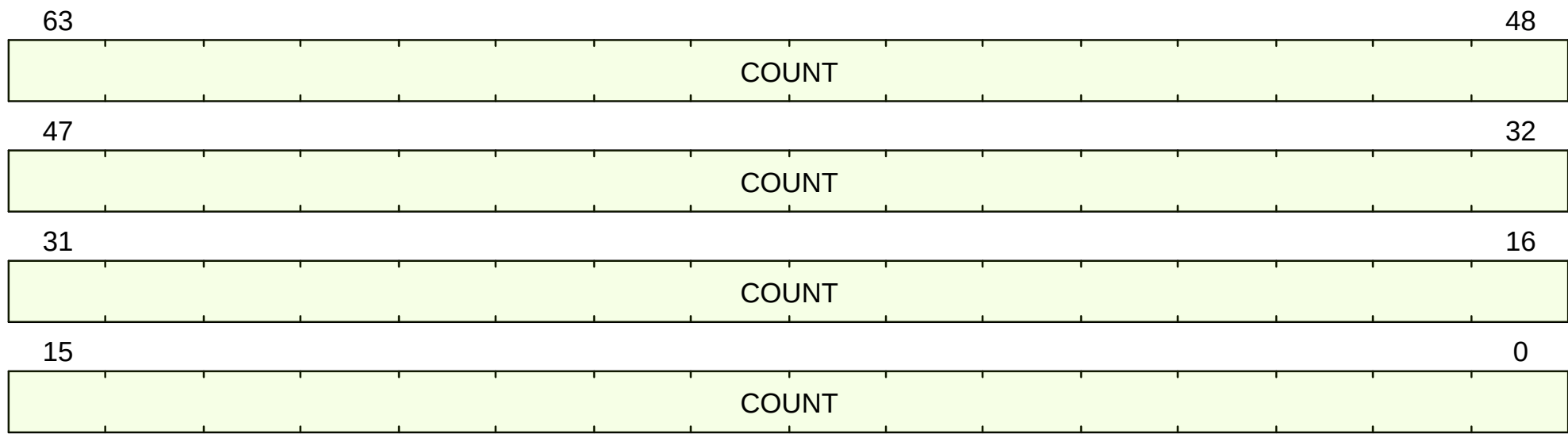


Figure 18. hpmcounter23 format

C.18.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter23.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.18.4. Fields

hpmcounter23.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter23.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.18.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM23 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM23 & CSR[scounteren].HPM23) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM23 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM23 == 1'b0 && CSR[mcounteren].HPM23 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM23 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM23 & CSR[scounteren].HPM23) == 1'b0 && (CSR[mcounteren].HPM23 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM23 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(23);
```

C.19. hpmcounter24

User-mode Hardware Performance Counter 21

Alias for M-mode CSR [mhpmcounter24](#).

Privilege mode access is controlled with [mcounteren.HPM24](#) <%- if ext?(:S) -%> , [scounteren.HPM24](#) <%- if ext?(:H) -%> , and [hcounteren.HPM24](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM24	scounteren.HPM24	hcounteren.HPM24	hpmcounter24 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM24	scounteren.HPM24	hpmcounter24 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM24	hpmcounter24 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.19.1. Attributes

CSR Address	0xc18
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.19.2. Format

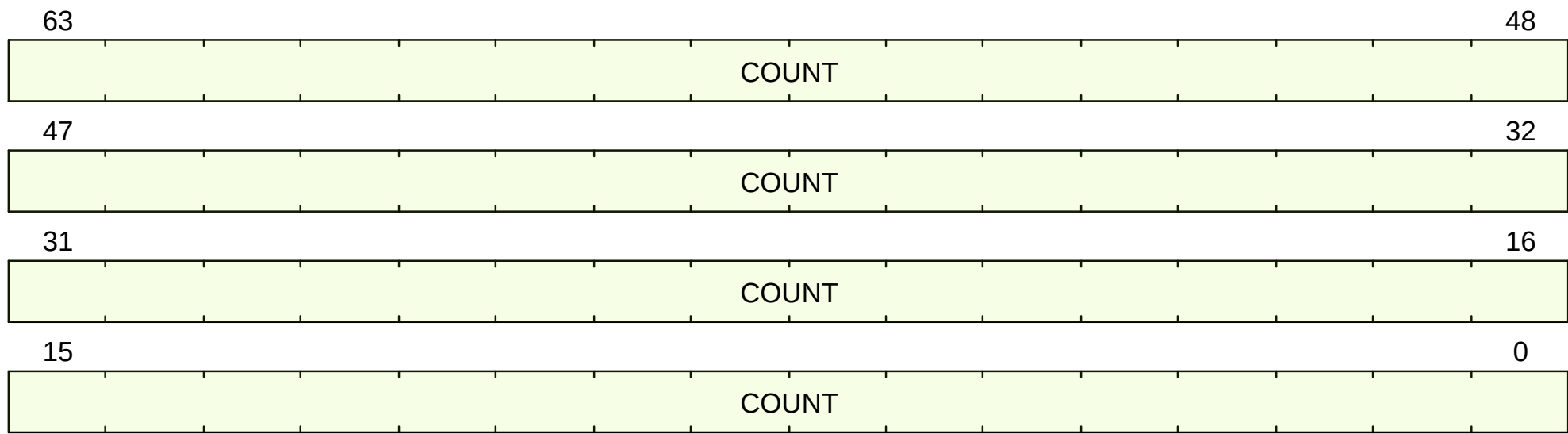


Figure 19. hpmcounter24 format

C.19.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter24.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.19.4. Fields

hpmcounter24.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter24.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.19.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM24 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM24 & CSR[scounteren].HPM24) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM24 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM24 == 1'b0 && CSR[mcounteren].HPM24 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM24 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM24 & CSR[scounteren].HPM24) == 1'b0 && (CSR[mcounteren].HPM24 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM24 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(24);
```

C.20. hpmcounter25

User-mode Hardware Performance Counter 22

Alias for M-mode CSR [mhpmcounter25](#).

Privilege mode access is controlled with [mcounteren.HPM25](#) <%- if ext?(:S) -%> , [scounteren.HPM25](#) <%- if ext?(:H) -%> , and [hcounteren.HPM25](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM25	scounteren.HPM25	hcounteren.HPM25	hpmcounter25 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM25	scounteren.HPM25	hpmcounter25 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM25	hpmcounter25 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.20.1. Attributes

CSR Address	0xc19
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.20.2. Format

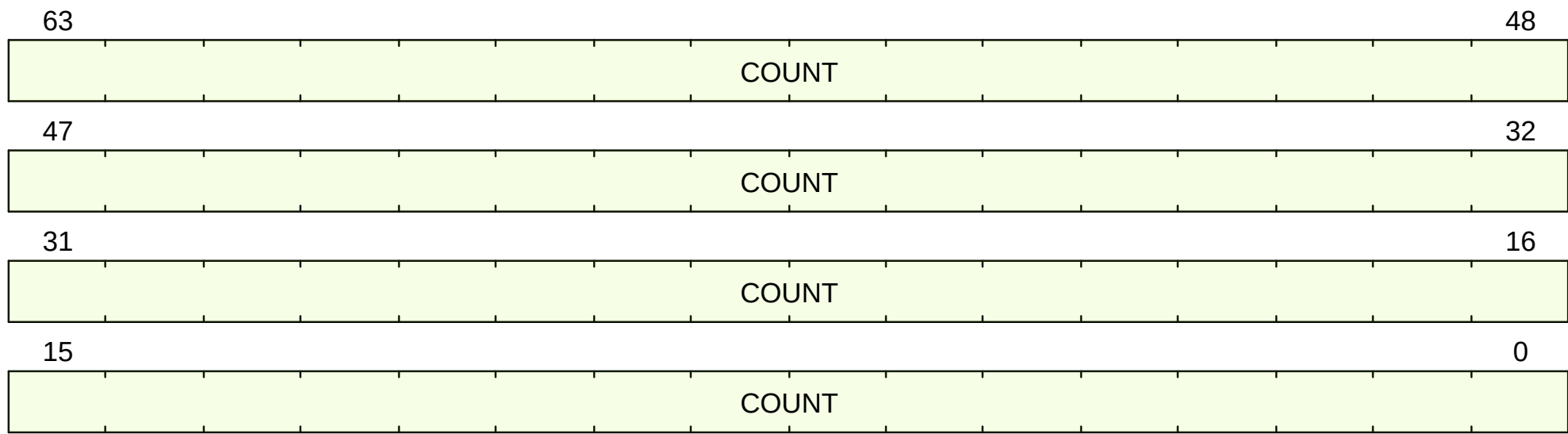


Figure 20. hpmcounter25 format

C.20.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter25.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.20.4. Fields

hpmcounter25.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter25.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.20.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM25 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM25 & CSR[scounteren].HPM25) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM25 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM25 == 1'b0 && CSR[mcounteren].HPM25 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM25 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM25 & CSR[scounteren].HPM25) == 1'b0 && (CSR[mcounteren].HPM25 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM25 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(25);
```

C.21. hpmcounter26

User-mode Hardware Performance Counter 23

Alias for M-mode CSR [mhpmcounter26](#).

Privilege mode access is controlled with [mcounteren.HPM26](#) <%- if ext?:(S) -%> , [scounteren.HPM26](#) <%- if ext?:(H) -%> , and [hcounteren.HPM26](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM26	scounteren.HPM26	hcounteren.HPM26	hpmcounter26 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM26	scounteren.HPM26	hpmcounter26 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM26	hpmcounter26 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.21.1. Attributes

CSR Address	0xc1a
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.21.2. Format

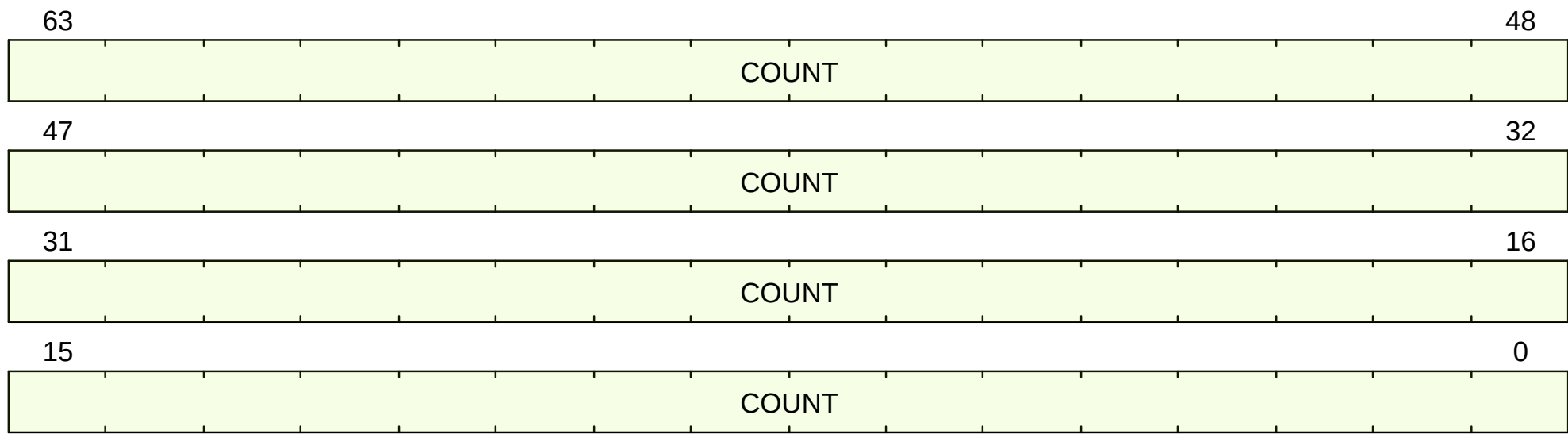


Figure 21. hpmcounter26 format

C.21.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter26.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.21.4. Fields

hpmcounter26.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter26.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.21.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM26 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM26 & CSR[scounteren].HPM26) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM26 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM26 == 1'b0 && CSR[mcounteren].HPM26 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM26 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM26 & CSR[scounteren].HPM26) == 1'b0 && (CSR[mcounteren].HPM26 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM26 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(26);
```

C.22. hpmcounter27

User-mode Hardware Performance Counter 24

Alias for M-mode CSR [mhpmcounter27](#).

Privilege mode access is controlled with [mcounteren.HPM27](#) <%- if ext?(:S) -%> , [scounteren.HPM27](#) <%- if ext?(:H) -%> , and [hcounteren.HPM27](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM27	scounteren.HPM27	hcounteren.HPM27	hpmcounter27 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM27	scounteren.HPM27	hpmcounter27 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM27	hpmcounter27 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.22.1. Attributes

CSR Address	0xc1b
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.22.2. Format

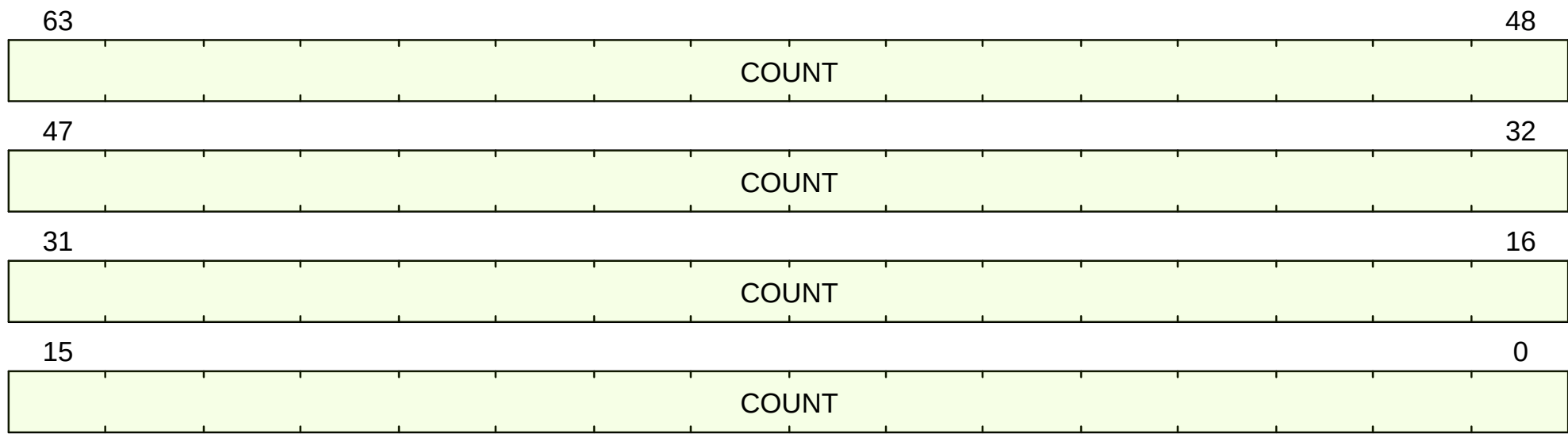


Figure 22. hpmcounter27 format

C.22.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter27.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.22.4. Fields

hpmcounter27.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter27.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.22.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM27 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM27 & CSR[scounteren].HPM27) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM27 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM27 == 1'b0 && CSR[mcounteren].HPM27 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM27 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM27 & CSR[scounteren].HPM27) == 1'b0 && (CSR[mcounteren].HPM27 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM27 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(27);
```

C.23. hpmcounter28

User-mode Hardware Performance Counter 25

Alias for M-mode CSR [mhpmcounter28](#).

Privilege mode access is controlled with [mcounteren.HPM28](#) <%- if ext?:(S) -%> , [scounteren.HPM28](#) <%- if ext?:(H) -%> , and [hcounteren.HPM28](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM28	scounteren.HPM28	hcounteren.HPM28	hpmcounter28 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM28	scounteren.HPM28	hpmcounter28 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM28	hpmcounter28 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.23.1. Attributes

CSR Address	0xc1c
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.23.2. Format

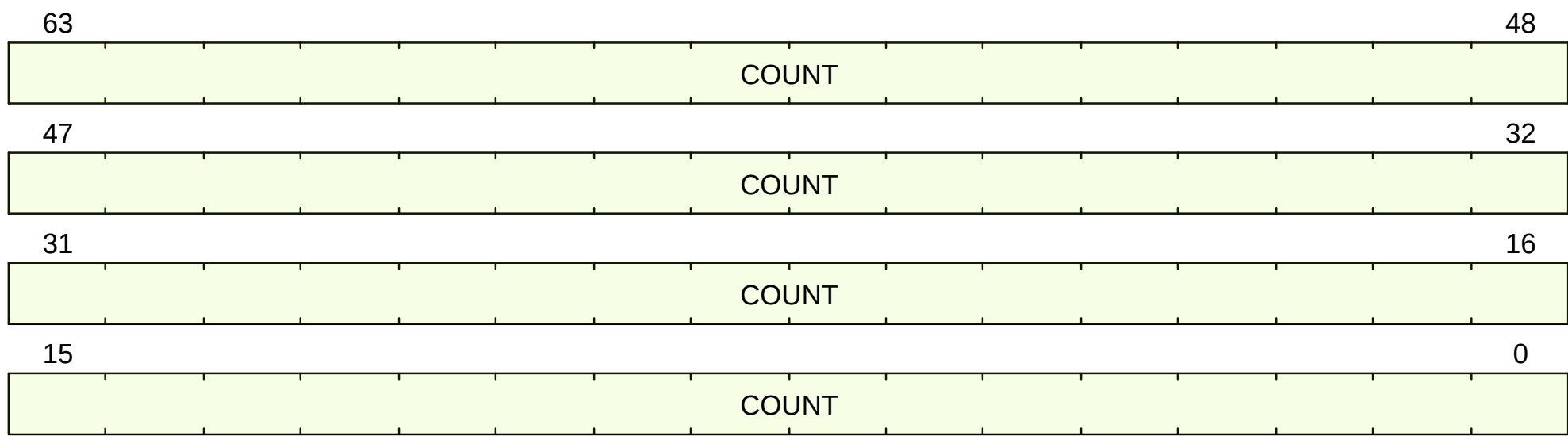


Figure 23. hpmcounter28 format

C.23.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter28.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.23.4. Fields

hpmcounter28.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter28.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.23.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM28 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM28 & CSR[scounteren].HPM28) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM28 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM28 == 1'b0 && CSR[mcounteren].HPM28 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM28 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM28 & CSR[scounteren].HPM28) == 1'b0 && (CSR[mcounteren].HPM28 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM28 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(28);
```

C.24. hpmcounter29

User-mode Hardware Performance Counter 26

Alias for M-mode CSR [mhpmcounter29](#).

Privilege mode access is controlled with [mcounteren.HPM29](#) <%- if ext?:(S) -%> , [scounteren.HPM29](#) <%- if ext?:(H) -%> , and [hcounteren.HPM29](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM29	scounteren.HPM29	hcounteren.HPM29	hpmcounter29 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM29	scounteren.HPM29	hpmcounter29 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM29	hpmcounter29 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.24.1. Attributes

CSR Address	0xc1d
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.24.2. Format

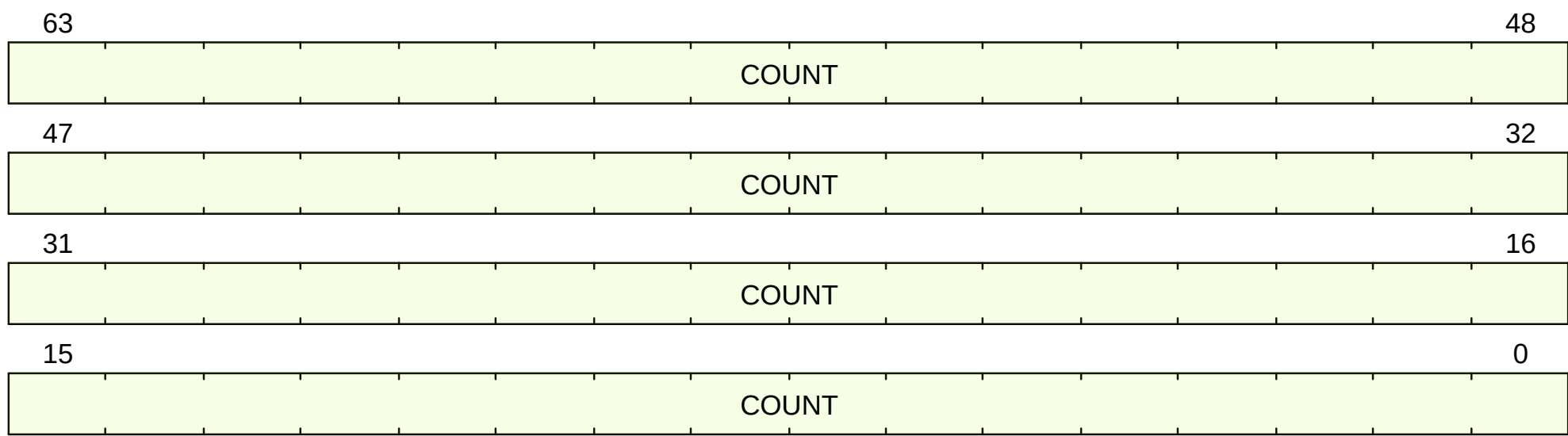


Figure 24. *hpmcounter29* format

C.24.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter29.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.24.4. Fields

hpmcounter29.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter29.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.24.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM29 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM29 & CSR[scounteren].HPM29) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM29 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM29 == 1'b0 && CSR[mcounteren].HPM29 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM29 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM29 & CSR[scounteren].HPM29) == 1'b0 && (CSR[mcounteren].HPM29 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM29 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(29);
```

C.25. hpmcounter3

User-mode Hardware Performance Counter 0

Alias for M-mode CSR [mhpmcounter3](#).

Privilege mode access is controlled with [mcounteren.HPM3](#) <%- if ext?(:S) -%> , [scounteren.HPM3](#) <%- if ext?(:H) -%> , and [hcounteren.HPM3](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM3	scounteren.HPM3	hcounteren.HPM3	hpmcounter3 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM3	scounteren.HPM3	hpmcounter3 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM3	hpmcounter3 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.25.1. Attributes

CSR Address	0xc03
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.25.2. Format

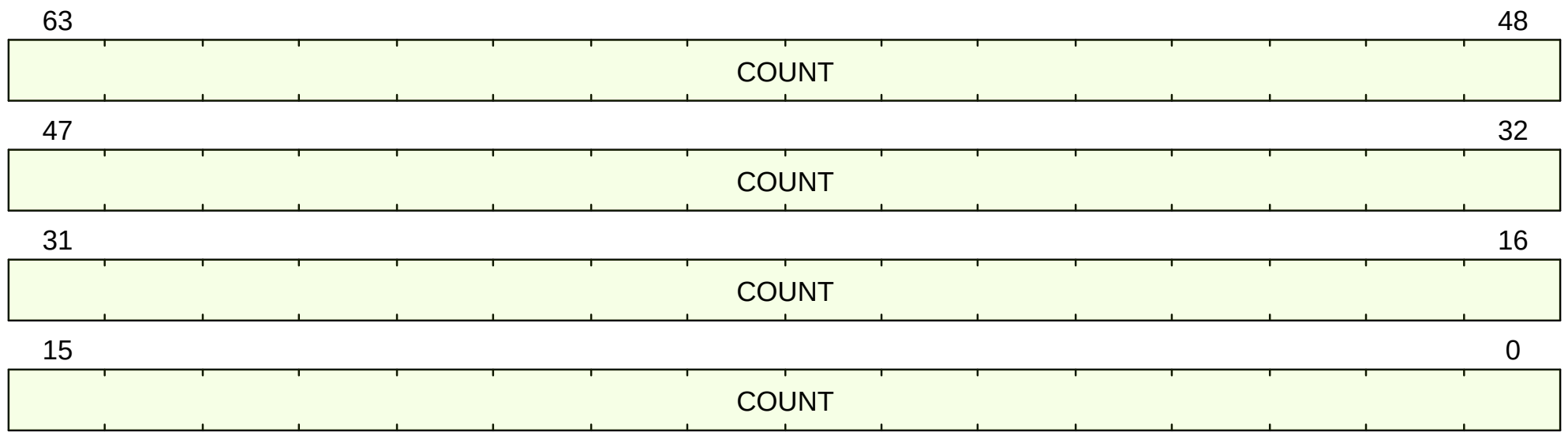


Figure 25. hpmcounter3 format

C.25.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter3.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.25.4. Fields

[hpmcounter3.COUNT](#) Field

Location:
63:0

Description:
Alias of [mhpmcounter3.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.25.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM3 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM3 & CSR[scounteren].HPM3) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM3 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM3 == 1'b0 && CSR[mcounteren].HPM3 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM3 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM3 & CSR[scounteren].HPM3 == 1'b0) && (CSR[mcounteren].HPM3 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM3 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(3);
```

C.26. hpmcounter30

User-mode Hardware Performance Counter 27

Alias for M-mode CSR [mhpmcounter30](#).

Privilege mode access is controlled with [mcounteren.HPM30](#) <%- if ext?:(S) -%> , [scounteren.HPM30](#) <%- if ext?:(H) -%> , and [hcounteren.HPM30](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM30	scounteren.HPM30	hcounteren.HPM30	hpmcounter30 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM30	scounteren.HPM30	hpmcounter30 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM30	hpmcounter30 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.26.1. Attributes

CSR Address	0xc1e
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.26.2. Format

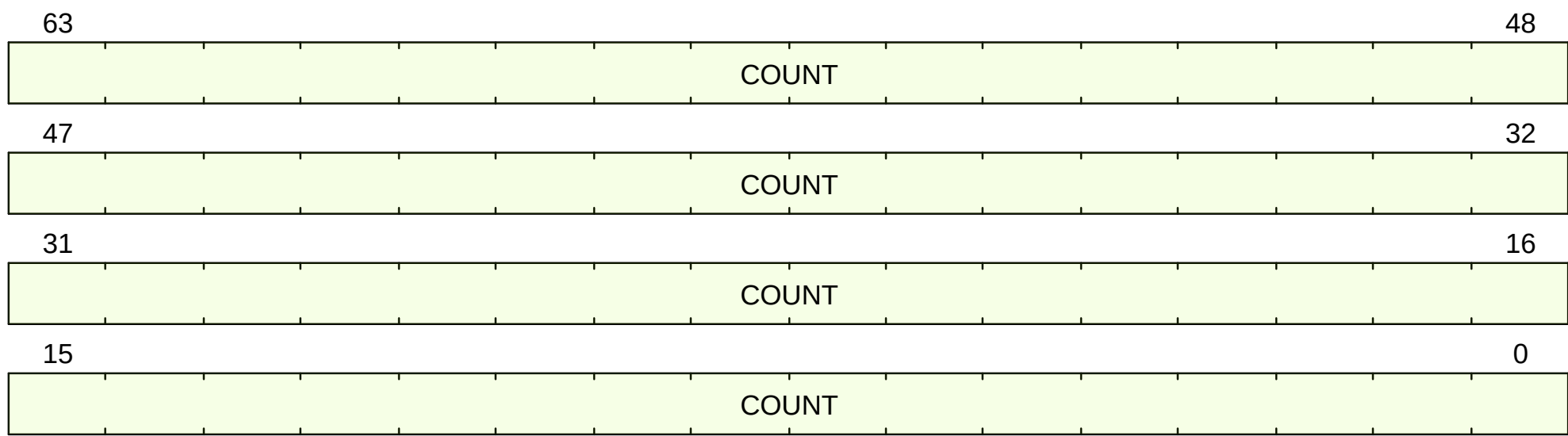


Figure 26. hpmcounter30 format

C.26.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter30.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.26.4. Fields

hpmcounter30.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter30.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.26.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM30 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM30 & CSR[scounteren].HPM30) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM30 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM30 == 1'b0 && CSR[mcounteren].HPM30 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM30 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM30 & CSR[scounteren].HPM30) == 1'b0 && (CSR[mcounteren].HPM30 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM30 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(30);
```

C.27. hpmcounter31

User-mode Hardware Performance Counter 28

Alias for M-mode CSR [mhpmcounter31](#).

Privilege mode access is controlled with [mcounteren.HPM31](#) <%- if ext?:(S) -%> , [scounteren.HPM31](#) <%- if ext?:(H) -%> , and [hcounteren.HPM31](#) <%- end -%> <%- end -%> as follows:

<%- if ext?:(H) -%>

mcounteren.HPM31	scounteren.HPM31	hcounteren.HPM31	hpmcounter31 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?:(S) -%>

mcounteren.HPM31	scounteren.HPM31	hpmcounter31 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM31	hpmcounter31 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.27.1. Attributes

CSR Address	0xc1f
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.27.2. Format

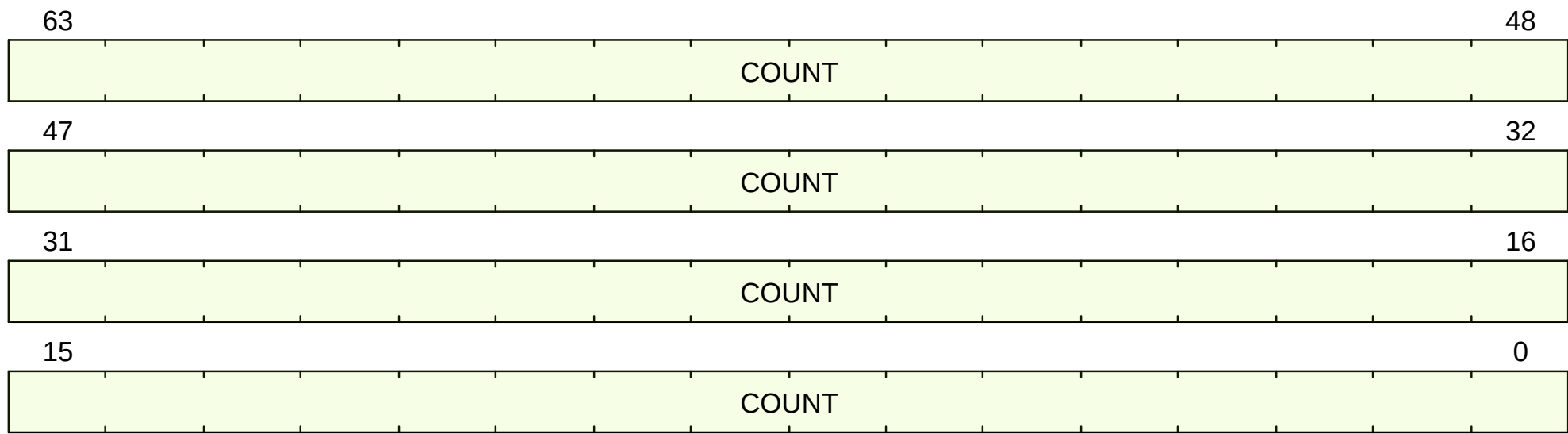


Figure 27. hpmcounter31 format

C.27.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter31.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.27.4. Fields

hpmcounter31.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter31.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.27.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM31 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM31 & CSR[scounteren].HPM31) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM31 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM31 == 1'b0 && CSR[mcounteren].HPM31 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM31 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM31 & CSR[scounteren].HPM31) == 1'b0 && (CSR[mcounteren].HPM31 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM31 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(31);
```

C.28. hpmcounter4

User-mode Hardware Performance Counter 1

Alias for M-mode CSR [mhpmcounter4](#).

Privilege mode access is controlled with [mcounteren.HPM4](#) <%- if ext?(:S) -%> , [scounteren.HPM4](#) <%- if ext?(:H) -%> , and [hcounteren.HPM4](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM4	scounteren.HPM4	hcounteren.HPM4	hpmcounter4 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM4	scounteren.HPM4	hpmcounter4 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM4	hpmcounter4 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.28.1. Attributes

CSR Address	0xc04
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.28.2. Format

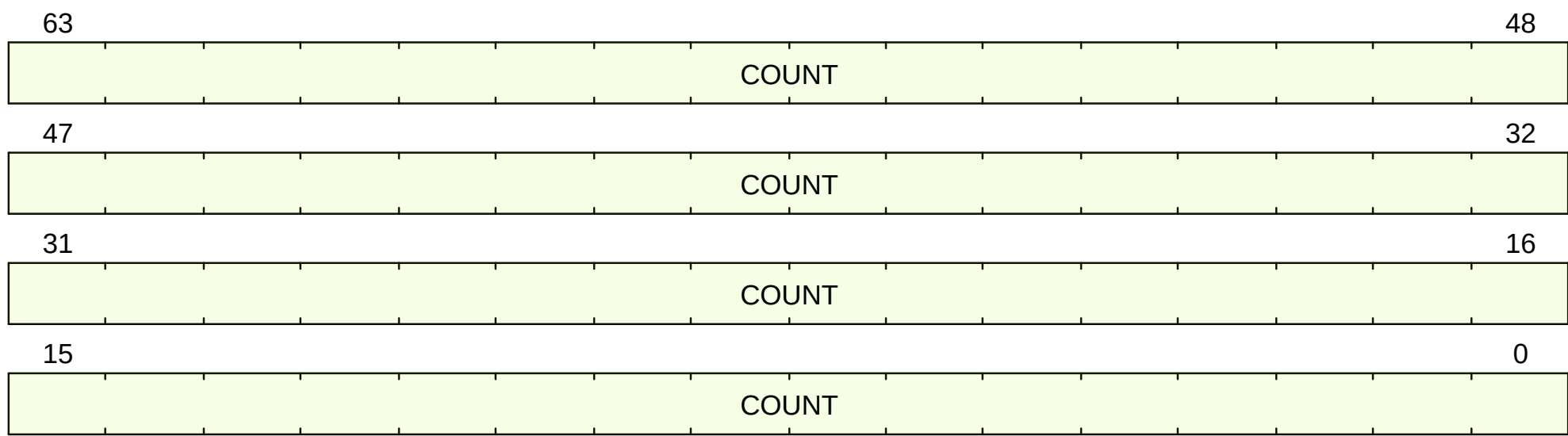


Figure 28. hpmcounter4 format

C.28.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter4.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.28.4. Fields

[hpmcounter4.COUNT](#) Field

Location:
63:0

Description:
Alias of [mhpmcounter4.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.28.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM4 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM4 & CSR[scounteren].HPM4) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM4 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM4 == 1'b0 && CSR[mcounteren].HPM4 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM4 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM4 & CSR[scounteren].HPM4) == 1'b0 && (CSR[mcounteren].HPM4 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM4 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(4);
```

C.29. hpmcounter5

User-mode Hardware Performance Counter 2

Alias for M-mode CSR [mhpmcounter5](#).

Privilege mode access is controlled with [mcounteren.HPM5](#) <%- if ext?(:S) -%> , [scounteren.HPM5](#) <%- if ext?(:H) -%> , and [hcounteren.HPM5](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM5	scounteren.HPM5	hcounteren.HPM5	hpmcounter5 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM5	scounteren.HPM5	hpmcounter5 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM5	hpmcounter5 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.29.1. Attributes

CSR Address	0xc05
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.29.2. Format

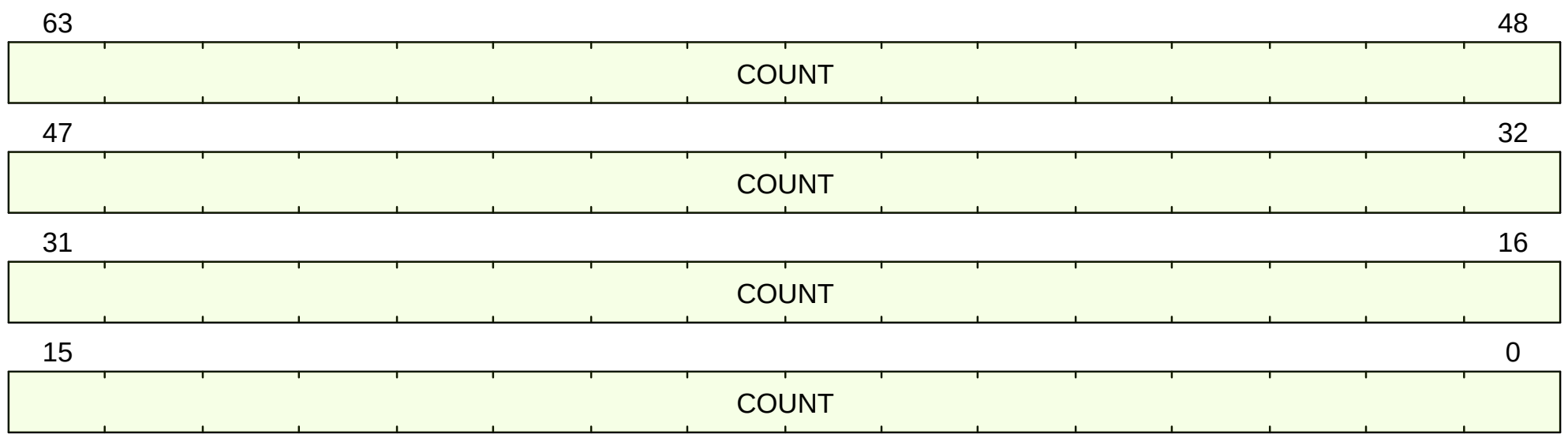


Figure 29. hpmcounter5 format

C.29.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter5.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.29.4. Fields

hpmcounter5.COUNT Field

Location:
63:0

Description:
Alias of [mhpmcounter5.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.29.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM5 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM5 & CSR[scounteren].HPM5) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM5 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM5 == 1'b0 && CSR[mcounteren].HPM5 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM5 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM5 & CSR[scounteren].HPM5 == 1'b0) && (CSR[mcounteren].HPM5 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM5 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(5);
```

C.30. hpmcounter6

User-mode Hardware Performance Counter 3

Alias for M-mode CSR [mhpmcounter6](#).

Privilege mode access is controlled with [mcounteren.HPM6](#) <%- if ext?(:S) -%> , [scounteren.HPM6](#) <%- if ext?(:H) -%> , and [hcounteren.HPM6](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM6	scounteren.HPM6	hcounteren.HPM6	hpmcounter6 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM6	scounteren.HPM6	hpmcounter6 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM6	hpmcounter6 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.30.1. Attributes

CSR Address	0xc06
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.30.2. Format

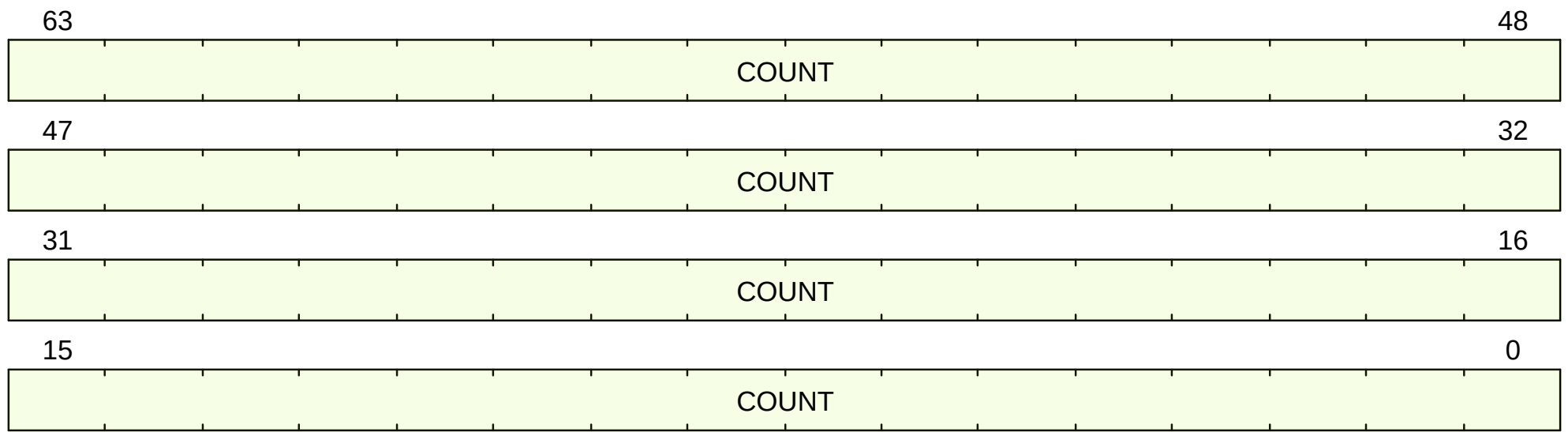


Figure 30. hpmcounter6 format

C.30.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter6.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.30.4. Fields

[hpmcounter6.COUNT](#) Field

Location:
63:0

Description:
Alias of [mhpmcounter6.COUNT](#).

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.30.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM6 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM6 & CSR[scounteren].HPM6) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM6 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM6 == 1'b0 && CSR[mcounteren].HPM6 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM6 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM6 & CSR[scounteren].HPM6) == 1'b0 && (CSR[mcounteren].HPM6 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM6 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(6);
```

C.31. hpmcounter7

User-mode Hardware Performance Counter 4

Alias for M-mode CSR [mhpmcounter7](#).

Privilege mode access is controlled with [mcounteren.HPM7](#) <%- if ext?(:S) -%> , [scounteren.HPM7](#) <%- if ext?(:H) -%> , and [hcounteren.HPM7](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM7	scounteren.HPM7	hcounteren.HPM7	hpmcounter7 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM7	scounteren.HPM7	hpmcounter7 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM7	hpmcounter7 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.31.1. Attributes

CSR Address	0xc07
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.31.2. Format

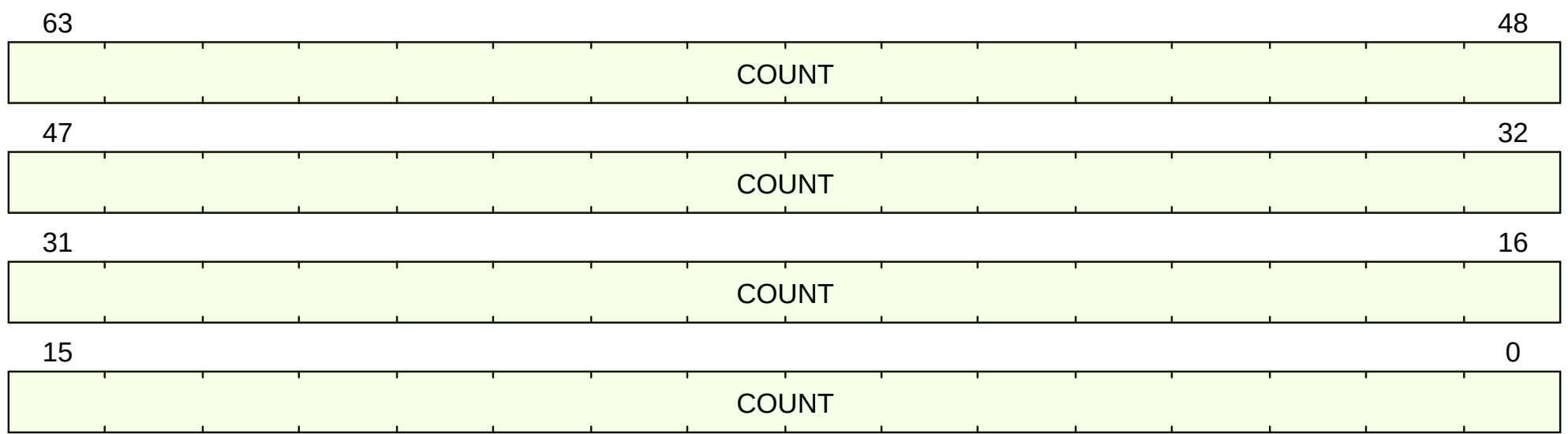


Figure 31. hpmcounter7 format

C.31.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter7.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.31.4. Fields

hpmcounter7.COUNT Field

Location:
63:0

Description:
Alias of mhpmpcounter7.COUNT.

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.31.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM7 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM7 & CSR[scounteren].HPM7) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM7 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM7 == 1'b0 && CSR[mcounteren].HPM7 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM7 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM7 & CSR[scounteren].HPM7) == 1'b0 && (CSR[mcounteren].HPM7 == 1'b1 {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM7 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(7);
```

C.32. hpmcounter8

User-mode Hardware Performance Counter 5

Alias for M-mode CSR [mhpmcounter8](#).

Privilege mode access is controlled with [mcounteren.HPM8](#) <%- if ext?(:S) -%> , [scounteren.HPM8](#) <%- if ext?(:H) -%> , and [hcounteren.HPM8](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM8	scounteren.HPM8	hcounteren.HPM8	hpmcounter8 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM8	scounteren.HPM8	hpmcounter8 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM8	hpmcounter8 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.32.1. Attributes

CSR Address	0xc08
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.32.2. Format

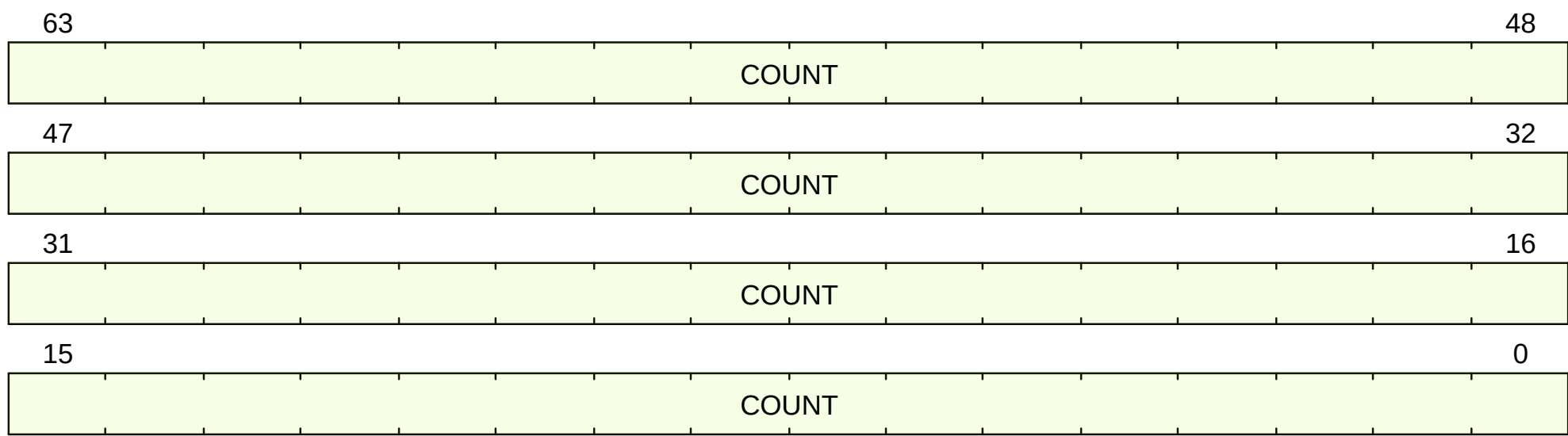


Figure 32. hpmcounter8 format

C.32.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter8.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.32.4. Fields

hpmcounter8.COUNT Field

Location:
63:0

Description:
Alias of mhpmcounter8.COUNT.

Type:
RO-H

Reset value:
UNDEFINED_LEGAL

C.32.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM8 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM8 & CSR[scounteren].HPM8) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM8 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM8 == 1'b0 && CSR[mcounteren].HPM8 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM8 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM8 & CSR[scounteren].HPM8 == 1'b0) && (CSR[mcounteren].HPM8 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM8 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(8);
```

C.33. hpmcounter9

User-mode Hardware Performance Counter 6

Alias for M-mode CSR [mhpmcounter9](#).

Privilege mode access is controlled with [mcounteren.HPM9](#) <%- if ext?(:S) -%> , [scounteren.HPM9](#) <%- if ext?(:H) -%> , and [hcounteren.HPM9](#) <%- end -%> <%- end -%> as follows:

<%- if ext?(:H) -%>

mcounteren.HPM9	scounteren.HPM9	hcounteren.HPM9	hpmcounter9 behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

<%- elsif ext?(:S) -%>

mcounteren.HPM9	scounteren.HPM9	hpmcounter9 behavior	
		S-mode	U-mode
0	-	IllegalInstruction	IllegalInstruction
1	0	read-only	IllegalInstruction
1	1	read-only	read-only

<%- else -%>

mcounteren.HPM9	hpmcounter9 behavior
	U-mode
0	IllegalInstruction
1	read-only

<%- end -%>

C.33.1. Attributes

CSR Address	0xc09
Defining extension	Zihpm
Length	64-bit
Privilege Mode	U

C.33.2. Format

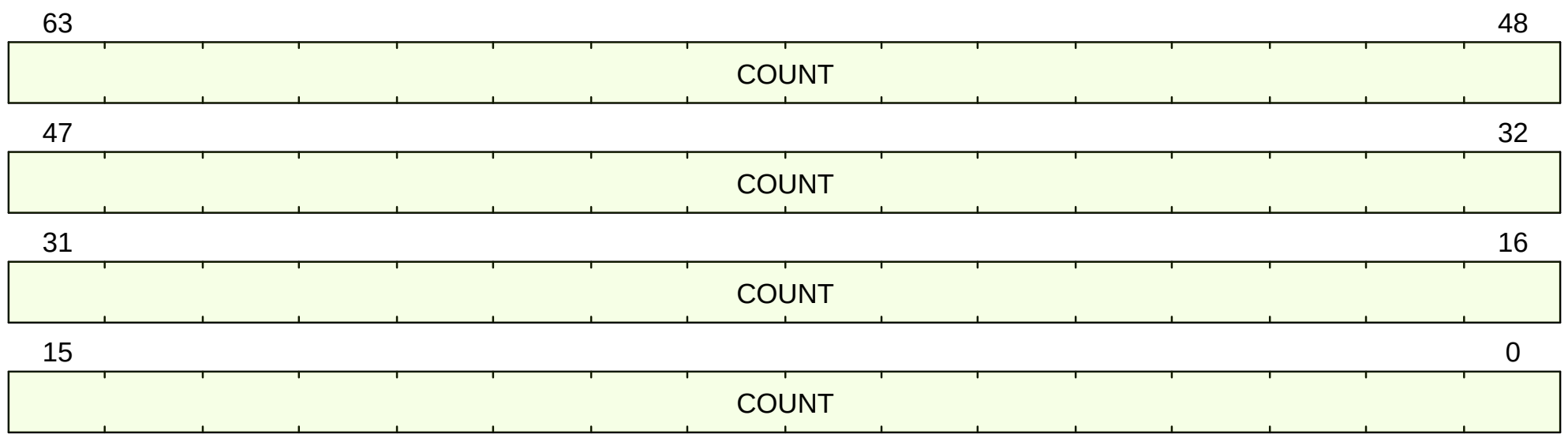


Figure 33. hpmcounter9 format

C.33.3. Field Summary

Name	Location	Type	Reset Value
hpmcounter9.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.33.4. Fields

hpmcounter9.COUNT Field

Location:

63:0

Description:

Alias of [mhpmpcounter9.COUNT](#).

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

C.33.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].HPM9 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].HPM9 & CSR[scounteren].HPM9) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].HPM9 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].HPM9 == 1'b0 && CSR[mcounteren].HPM9 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM9 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].HPM9 & CSR[scounteren].HPM9 == 1'b0) && (CSR[mcounteren].HPM9 == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].HPM9 == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return read_hpm_counter(9);
```

C.34. instret

Instructions retired counter for RDINSTRET Instruction

Alias for M-mode CSR [minstret](#).

Privilege mode access is controlled with [mcounteren.IR](#), [scounteren.IR](#), and [hcounteren.IR](#) as follows:

mcounteren.IR	scounteren.IR	hcounteren.IR	instret behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	IllegalInstruction	IllegalInstruction	IllegalInstruction	IllegalInstruction
1	0	0	read-only	IllegalInstruction	VirtualInstruction	VirtualInstruction
1	1	0	read-only	read-only	VirtualInstruction	VirtualInstruction
1	0	1	read-only	IllegalInstruction	read-only	VirtualInstruction
1	1	1	read-only	read-only	read-only	read-only

C.34.1. Attributes

CSR Address	0xc02
Defining extension	Zicntr
Length	64-bit
Privilege Mode	U

C.34.2. Format

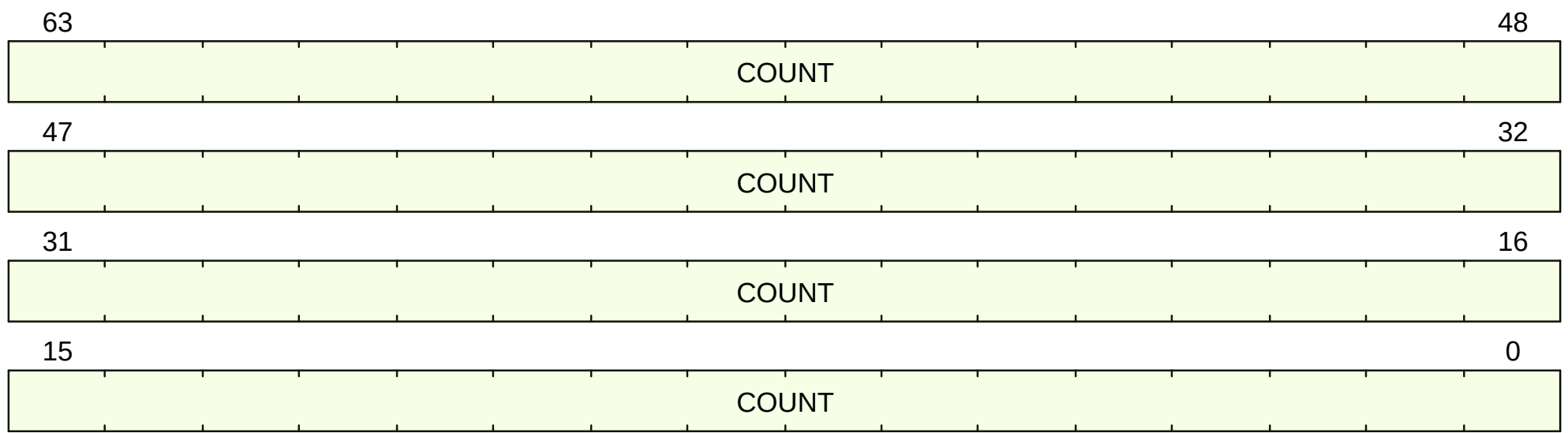


Figure 34. instret format

C.34.3. Field Summary

Nam e	Location	Type	Reset Value
instret.COUNT	63:0	RO-H	0

C.34.4. Fields

[instret.COUNT](#) Field

Location:
63:0

Description:
Alias of [minstret.COUNT](#).

Type:
RO-H

Reset value:
0

C.34.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (mode() == PrivilegeMode::S) {
  if (CSR[mcounteren].IR == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::U) {
  if (CSR[misa].S == 1'b1) {
    if ((CSR[mcounteren].IR & CSR[scounteren].IR) == 1'b0) {
      raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
  } else if (CSR[mcounteren].IR == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VS) {
  if (CSR[hcounteren].IR == 1'b0 && CSR[mcounteren].IR == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].IR == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
} else if (mode() == PrivilegeMode::VU) {
  if (CSR[hcounteren].IR & CSR[scounteren].IR == 1'b0) && (CSR[mcounteren].IR == 1'b1) {
    raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
  } else if (CSR[mcounteren].IR == 1'b0) {
    raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
  }
}
return CSR[minstret].COUNT;
```

C.35. marchid

Machine Architecture ID

The [marchid](#) CSR is an MXLEN-bit read-only register encoding the base microarchitecture of the hart. This register must be readable in any implementation, but a value of 0 can be returned to indicate the field is not implemented. The combination of [mvendorid](#) and [marchid](#) should uniquely identify the type of hart microarchitecture that is implemented.

Open-source project architecture IDs are allocated globally by RISC-V International, and have non-zero architecture IDs with a zero most-significant-bit (MSB). Commercial architecture IDs are allocated by each commercial vendor independently, but must have the MSB set and cannot contain zero in the remaining MXLEN-1 bits.



The intent is for the architecture ID to represent the microarchitecture associated with the repo around which development occurs rather than a particular organization. Commercial fabrications of open-source designs should (and might be required by the license to) retain the original architecture ID. This will aid in reducing fragmentation and tool support costs, as well as provide attribution. Open-source architecture IDs are administered by RISC-V International and should only be allocated to released, functioning open-source projects. Commercial architecture IDs can be managed independently by any registered vendor but are required to have IDs disjoint from the open-source architecture IDs (MSB set) to prevent collisions if a vendor wishes to use both closed-source and open-source microarchitectures.

The convention adopted within the following Implementation field can be used to segregate branches of the same architecture design, including by organization. The [misa](#) register also helps distinguish different variants of a design.

C.35.1. Attributes

CSR Address	0xf12
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.35.2. Format

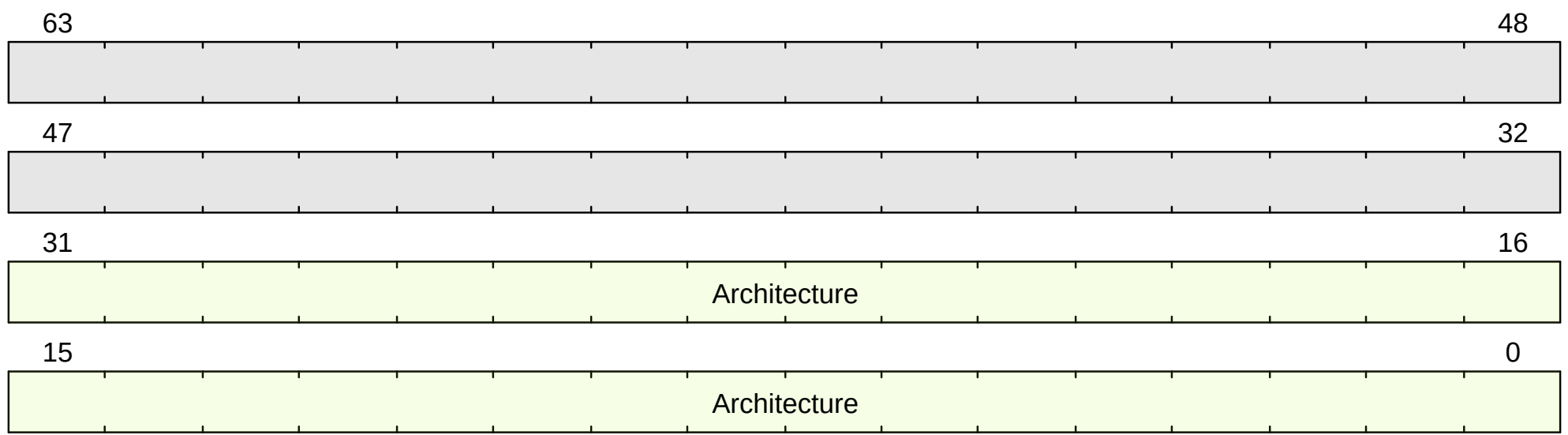


Figure 35. marchid format

C.35.3. Field Summary

Name	Location	Type	Reset Value
marchid.Architecture	63:0	RO	UNDEFINED_LEGAL

C.35.4. Fields

[marchid.Architecture](#) Field

Location:

63:0

Description:

Vendor-specific microarchitecture ID.

Type:

RO

Reset value:

UNDEFINED_LEGAL

C.36. mcause

Machine Cause

Reports the cause of the latest exception.

C.36.1. Attributes

CSR Address	0x342
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.36.2. Format

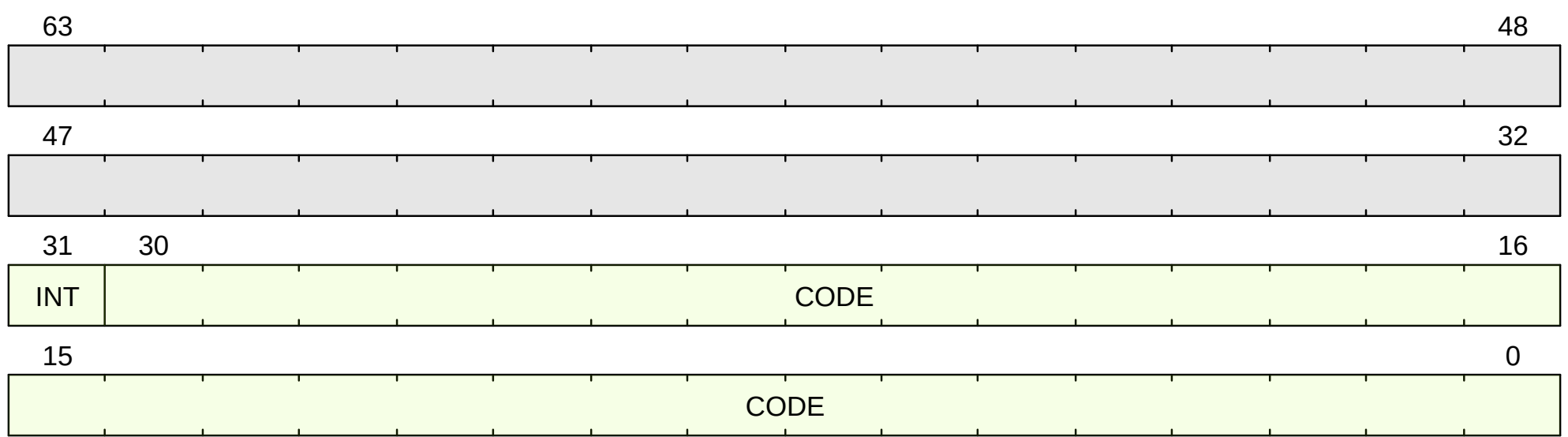


Figure 36. mcause format

C.36.3. Field Summary

Nam e	Location	Type	Reset Value
mcause.INT	63	RW-RH	0
mcause.CODE	62:0	RW-RH	0

C.36.4. Fields

mcause.INT Field

Location:
63

Description:
Written by hardware when a trap is taken into M-mode.

When set, the last exception was caused by an asynchronous Interrupt.

mcause.INT is writable.

[when,"TRAP_ON_ILLEGAL_WLRL == true"]
If mcause is written with an undefined cause (combination of mcause.INT and mcause.CODE), an Illegal Instruction exception occurs.

[when,"TRAP_ON_ILLEGAL_WLRL == false"]
If mcause is written with an undefined cause (combination of mcause.INT and mcause.CODE), neither mcause.INT nor mcause.CODE are modified.

Type:
RW-RH

Reset value:

0

mcause.CODE Field

Location:

62:0

Description:

Written by hardware when a trap is taken into M-mode.

Holds the interrupt or exception code for the last taken trap.

mcause.CODE is writable.

[when,"TRAP_ON_ILLEGAL_WLRL == true"]

If mcause is written with an undefined cause (combination of mcause.INT and mcause.CODE), an Illegal Instruction exception occurs.

[when,"TRAP_ON_ILLEGAL_WLRL == false"]

If mcause is written with an undefined cause (combination of mcause.INT and mcause.CODE), neither mcause.INT nor mcause.CODE are modified.

Valid interrupt codes are:

[separator="!"]

!===

<%- implemented_interrupt_codes.sort_by{ |code| code.num }.each do |code| -%>

! <%= code.num %> ! <%= code.name %>

<%- end -%>

!===

Valid exception codes are:

[separator="!"]

!===

<%- implemented_exception_codes.sort_by{ |code| code.num }.each do |code| -%>

! <%= code.num %> ! <%= code.name %>

<%- end -%>

!===

Type:

RW-RH

Reset value:

0

C.36.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through csrrw), the following determines the written value:

```
INT = # the write only holds if the INT/CODE combination is valid
if (csr_value.INT == 1) {
  if (valid_interrupt_code?(csr_value.CODE)) {
    return 1;
  }
  return ILLEGAL_WLRL;
} else {
  if (valid_exception_code?(csr_value.CODE)) {
    return 1;
  }
  return ILLEGAL_WLRL;
}

CODE = # the write only holds if the INT/CODE combination is valid
if (csr_value.INT == 1) {
  if (valid_interrupt_code?(csr_value.CODE)) {
    return csr_value.CODE;
  }
  return ILLEGAL_WLRL;
```

```
} else {  
    if (valid_exception_code?(csr_value.CODE)) {  
        return csr_value.CODE;  
    }  
    return ILLEGAL_WLRL;  
}
```


C.37. mcontext

Machine Context

This register must be implemented if [hcontext](#) is implemented, and is optional otherwise. It is only accessible in M-mode and Debug mode.

[hcontext](#) is primarily useful to set triggers on hypervisor systems that only fire when a given VM is executing. It is also useful in systems where M-Mode implements something like a hypervisor directly.

C.37.1. Attributes

CSR Address	0x7a8
Defining extension	Sdtrig
Length	64-bit
Privilege Mode	M

C.37.2. Format

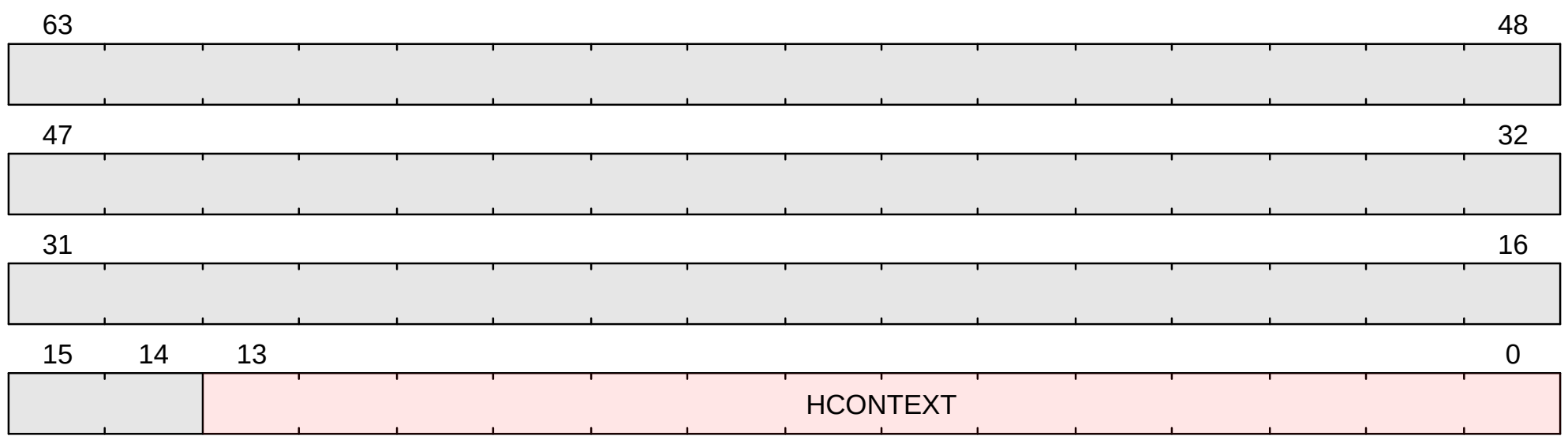


Figure 37. `mcontext` format

C.37.3. Field Summary

Name	Location	Type	Reset Value
mcontext.HCONTEXT	13:0	RW	0

C.37.4. Fields

[mcontext.HCONTEXT](#) Field

Location:
13:0

Description:
M-Mode or HS-Mode (using [hcontext](#)) software can write a context number to this register, which can be used to set triggers that only fire in that specific context.

An implementation may tie any number of upper bits in this field to 0. If the H extension is not implemented, it's recommended to implement 6 bits on RV32 and 13 bits on RV64 (as visible through the [mcontext](#) register). If the H extension is implemented, it's recommended to implement 7 bits on RV32 and 14 bits on RV64.

Type:
RW

Reset value:
0

C.37.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
HCONTEXT = # check if MCONTEXT is available
if (!MCONTEXT_AVAILABLE) {
    unimplemented_csr($encoding);
}

# enforce width of HCONTEXT
Bits<14> hcontext_value = csr_value.HCONTEXT & ((14'1 << DBG_HCONTEXT_WIDTH) - 1);
return hcontext_value;
```

C.37.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (!MCONTEXT_AVAILABLE) {
    unimplemented_csr($encoding);
}
return $bits(CSR[CSR[mcontext]]);
```

C.38. mcounteren

Machine Counter Enable

The counter-enable [mcounteren](#) register is a 32-bit register that controls the availability of the hardware performance-monitoring counters to <%- if ext?(:S) -%> S-mode <%- elsif ext?(:U) -%> U-mode <%- else -%> the next-lower privileged mode <%- end -%> .

The settings in this register only control accessibility. The act of reading or writing this register does not affect the underlying counters, which continue to increment even when not accessible.

When the CY, TM, IR, or HPMn bit in the mcounteren register is clear, attempts to read the [cycle](#), [time](#), [instret](#), or [hpmcountern](#) register while executing in <%- if ext?(:S) -%> S-mode <%- elsif ext?(:U) -%> U-mode <%- else -%> S-mode or U-mode <%- end -%> will cause an [IllegalInstruction](#) exception. When one of these bits is set, access to the corresponding register is permitted in <%- if ext?(:S) -%> S-mode <%- elsif ext?(:U) -%> U-mode <%- else -%> the next implemented privilege mode (S-mode if implemented, otherwise U-mode). <%- end -%>



The counter-enable bits support two common use cases with minimal hardware. For harts that do not need high-performance timers and counters, machine-mode software can trap accesses and implement all features in software. For harts that need high-performance timers and counters but are not concerned with obfuscating the underlying hardware counters, the counters can be directly exposed to lower privilege modes.

The [cycle](#), [instret](#), and [hpmcountern](#) CSRs are read-only shadows of [mcycle](#), [minstret](#), and [mhpmpcounter n](#), respectively. The [time](#) CSR is a read-only shadow of the memory-mapped [mtime](#) register. <%- if possible_xlens.include?(32) -%> Analogously, on RV32I the [cycleh](#), [instreth](#) and [hpmcounternh](#) CSRs are read-only shadows of [mcycleh](#), [minstreth](#) and [mhpmpcounternh](#), respectively. On RV32I the [timeh](#) CSR is a read-only shadow of the upper 32 bits of the memory-mapped [mtime](#) register, while time shadows only the lower 32 bits of [mtime](#). <%- end -%>



Implementations can convert reads of the [time](#) and [timeh](#) CSRs into loads to the memory-mapped [mtime](#) register, or emulate this functionality on behalf of less-privileged modes in M-mode software.

<%- if !ext?(:U) -%> In harts with U-mode, the [mcounteren](#) CSR must be implemented, but all fields are WARL and may be read-only zero, indicating reads to the corresponding counter will cause an [IllegalInstruction](#) exception when executing in a less-privileged mode. In harts without U-mode, the [mcounteren](#) register should not exist. <%- end -%>

<%- if ext?(:S) -%>

The [cycle](#), [instret](#), and [hpmcountern](#) CSRs can also be made available to U-mode through the [scounteren](#) CSR <%- if ext?(:H) -%> and to VS-mode and/or VU-mode through [hcounteren](#) <%- end -%> . <%- end -%>

C.38.1. Attributes

CSR Address	0x306
Defining extension	U
Length	32-bit
Privilege Mode	M

C.38.2. Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HPM31	HPM30	HPM29	HPM28	HPM27	HPM26	HPM25	HPM24	HPM23	HPM22	HPM21	HPM20	HPM19	HPM18	HPM17	HPM16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HPM15	HPM14	HPM13	HPM12	HPM11	HPM10	HPM9	HPM8	HPM7	HPM6	HPM5	HPM4	HPM3	IR	TM	CY

Figure 38. mcounteren format

C.38.3. Field Summary

Name	Location	Type	Reset Value
mcoun teren.C Y	0	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.T M	1	RO	0
mcoun teren.I R	2	RW	UNDEFINED_LEGAL
		RO	

Name	Location	Type	Reset Value
mcoun teren.H PM3	3	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM4	4	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM5	5	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM6	6	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM7	7	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM8	8	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM9	9	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM10	10	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM11	11	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM12	12	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM13	13	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM14	14	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM15	15	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM16	16	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM17	17	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM18	18	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM19	19	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM20	20	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM21	21	RW	UNDEFINED_LEGAL
		RO	
mcoun teren.H PM22	22	RW	UNDEFINED_LEGAL
		RO	

Name	Location	Type	Reset Value
mcouteren.H PM23	23	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM24	24	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM25	25	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM26	26	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM27	27	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM28	28	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM29	29	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM30	30	RW	UNDEFINED_LEGAL
		RO	
mcouteren.H PM31	31	RW	UNDEFINED_LEGAL
		RO	

C.38.4. Fields

[mcouteren.CY](#) Field

Location:

0

Description:

When set, the [cycle](#) CSR (an alias of [mcycle](#)) is accessible to

<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When [scounteren.CY](#) is also set, [cycle](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.CY](#) is also set, [cycle](#) is further accessible to VS-mode.

When [hcounteren.CY](#) && [scounteren.CY](#) are both set, [cycle](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.TM Field

Location:

1

Description:

Placeholder for delegating [time](#) to less-privileged modes; however, since [time](#) is memory-mapped rather than a CSR, this field is always read-only zero.

Type:

RO

Reset value:

0

mcounteren.IR Field

Location:

2

Description:

When set, the [instret](#) CSR (an alias of [minstret](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.IR](#) is also set, [instret](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.IR](#) is also set, [instret](#) is further accessible to VS-mode.

When [hcounteren.IR](#) && [scounteren.IR](#) are both set, [instret](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.HPM3 Field

Location:

3

Description:

When set, the [hpmcounter3](#) CSR (an alias of [mhpmcounter3](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM3](#) is also set, [hpmcounter3](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM3](#) is also set, [hpmcounter3](#) is further accessible to VS-mode.

When [hcounteren.HPM3](#) && [scounteren.HPM3](#) are both set, [hpmcounter3](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM4](#) Field

Location:

4

Description:

When set, the [hpmcounter4](#) CSR (an alias of [mhpmcounter4](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM4](#) is also set, [hpmcounter4](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM4](#) is also set, [hpmcounter4](#) is further accessible to VS-mode.

When [hcounteren.HPM4](#) && [scounteren.HPM4](#) are both set, [hpmcounter4](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM5](#) Field

Location:

5

Description:

When set, the [hpmcounter5](#) CSR (an alias of [mhpmcounter5](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM5](#) is also set, [hpmcounter5](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM5](#) is also set, [hpmcounter5](#) is further accessible to VS-mode.

When [hcounteren.HPM5](#) && [scounteren.HPM5](#) are both set, [hpmcounter5](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcouteren.HPM6 Field

Location:

6

Description:

When set, the [hpmcounter6](#) CSR (an alias of [mhpmcounter6](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scouteren.HPM6](#) is also set, [hpmcounter6](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM6](#) is also set, [hpmcounter6](#) is further accessible to VS-mode.

When [hcounteren.HPM6](#) && [scouteren.HPM6](#) are both set, [hpmcounter6](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcouteren.HPM7 Field

Location:

7

Description:

When set, the [hpmcounter7](#) CSR (an alias of [mhpmcounter7](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scouteren.HPM7](#) is also set, [hpmcounter7](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM7](#) is also set, [hpmcounter7](#) is further accessible to VS-mode.

When [hcounteren.HPM7](#) && [scouteren.HPM7](#) are both set, [hpmcounter7](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcouteren.HPM8 Field

Location:
8

Description:

When set, the [hpmcounter8](#) CSR (an alias of [mhpmcounter8](#)) is accessible to

<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When [scounteren.HPM8](#) is also set, [hpmcounter8](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM8](#) is also set, [hpmcounter8](#) is further accessible to VS-mode.

When [hcounteren.HPM8](#) && [scounteren.HPM8](#) are both set, [hpmcounter8](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcouteren.HPM9 Field

Location:
9

Description:

When set, the [hpmcounter9](#) CSR (an alias of [mhpmcounter9](#)) is accessible to

<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When [scounteren.HPM9](#) is also set, [hpmcounter9](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM9](#) is also set, [hpmcounter9](#) is further accessible to VS-mode.

When [hcounteren.HPM9](#) && [scounteren.HPM9](#) are both set, [hpmcounter9](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounteren.HPM10 Field

Location:

10

Description:

When set, the [hpmcounter10](#) CSR (an alias of [mhpmcounter10](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM10](#) is also set, [hpmcounter10](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM10](#) is also set, [hpmcounter10](#) is further accessible to VS-mode.

When [hcounteren.HPM10](#) && [scounteren.HPM10](#) are both set, [hpmcounter10](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.HPM11 Field

Location:

11

Description:

When set, the [hpmcounter11](#) CSR (an alias of [mhpmcounter11](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM11](#) is also set, [hpmcounter11](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM11](#) is also set, [hpmcounter11](#) is further accessible to VS-mode.

When [hcounteren.HPM11](#) && [scounteren.HPM11](#) are both set, [hpmcounter11](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.HPM12 Field

Location:

12

Description:

When set, the [hpmcounter12](#) CSR (an alias of [mhpmcounter12](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>
```

```
<%- if ext?(:S) -%>
When scounteren.HPM12 is also set, hpmcounter12 is further accessible to U-mode.
<%- end -%>
```

```
<%- if ext?(:H) -%>
When hcounteren.HPM12 is also set, hpmcounter12 is further accessible to VS-mode.
```

```
When hcounteren.HPM12 && scounteren.HPM12 are both set, hpmcounter12 is further accessible to VU-mode.
<%- end -%>
```

Type:

- RW
 - RO
- Reset value:**
- UNDEFINED_LEGAL

[mcounteren.HPM13](#) Field

Location:

13

Description:

When set, the [hpmcounter13](#) CSR (an alias of [mhpmcounter13](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>
```

```
<%- if ext?(:S) -%>
When scounteren.HPM13 is also set, hpmcounter13 is further accessible to U-mode.
<%- end -%>
```

```
<%- if ext?(:H) -%>
When hcounteren.HPM13 is also set, hpmcounter13 is further accessible to VS-mode.
```

```
When hcounteren.HPM13 && scounteren.HPM13 are both set, hpmcounter13 is further accessible to VU-mode.
<%- end -%>
```

Type:

- RW
 - RO
- Reset value:**
- UNDEFINED_LEGAL

[mcounteren.HPM14](#) Field

Location:

14

Description:

When set, the [hpmcounter14](#) CSR (an alias of [mhpmcounter14](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
```

```
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When scounteren.HPM14 is also set, hpmcounter14 is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When hcounteren.HPM14 is also set, hpmcounter14 is further accessible to VS-mode.

When hcounteren.HPM14 && scounteren.HPM14 are both set, hpmcounter14 is further accessible to VU-mode.
<%- end -%>
```

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM15](#) Field

Location:

15

Description:

When set, the [hpmcounter15](#) CSR (an alias of [mhpmcounter15](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When scounteren.HPM15 is also set, hpmcounter15 is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When hcounteren.HPM15 is also set, hpmcounter15 is further accessible to VS-mode.

When hcounteren.HPM15 && scounteren.HPM15 are both set, hpmcounter15 is further accessible to VU-mode.
<%- end -%>
```

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM16](#) Field

Location:

16

Description:

When set, the [hpmcounter16](#) CSR (an alias of [mhpmcounter16](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
```

When [scounteren.HPM16](#) is also set, [hpmcounter16](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM16](#) is also set, [hpmcounter16](#) is further accessible to VS-mode.

When [hcounteren.HPM16](#) && [scounteren.HPM16](#) are both set, [hpmcounter16](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM17](#) Field

Location:

17

Description:

When set, the [hpmcounter17](#) CSR (an alias of [mhpmcounter17](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM17](#) is also set, [hpmcounter17](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM17](#) is also set, [hpmcounter17](#) is further accessible to VS-mode.

When [hcounteren.HPM17](#) && [scounteren.HPM17](#) are both set, [hpmcounter17](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM18](#) Field

Location:

18

Description:

When set, the [hpmcounter18](#) CSR (an alias of [mhpmcounter18](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM18](#) is also set, [hpmcounter18](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM18](#) is also set, [hpmcounter18](#) is further accessible to VS-mode.

When [hcounteren.HPM18](#) && [scounteren.HPM18](#) are both set, [hpmcounter18](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM19](#) Field

Location:

19

Description:

When set, the [hpmcounter19](#) CSR (an alias of [mhpmcounter19](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM19](#) is also set, [hpmcounter19](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM19](#) is also set, [hpmcounter19](#) is further accessible to VS-mode.

When [hcounteren.HPM19](#) && [scounteren.HPM19](#) are both set, [hpmcounter19](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM20](#) Field

Location:

20

Description:

When set, the [hpmcounter20](#) CSR (an alias of [mhpmcounter20](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM20](#) is also set, [hpmcounter20](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM20](#) is also set, [hpmcounter20](#) is further accessible to VS-mode.

When [hcounteren.HPM20](#) && [scounteren.HPM20](#) are both set, [hpmcounter20](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcouteren.HPM21 Field

Location:

21

Description:

When set, the [hpmcounter21](#) CSR (an alias of [mhpmcounter21](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM21](#) is also set, [hpmcounter21](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM21](#) is also set, [hpmcounter21](#) is further accessible to VS-mode.

When [hcounteren.HPM21](#) && [scounteren.HPM21](#) are both set, [hpmcounter21](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcouteren.HPM22 Field

Location:

22

Description:

When set, the [hpmcounter22](#) CSR (an alias of [mhpmcounter22](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM22](#) is also set, [hpmcounter22](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM22](#) is also set, [hpmcounter22](#) is further accessible to VS-mode.

When [hcounteren.HPM22](#) && [scounteren.HPM22](#) are both set, [hpmcounter22](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcouteren.HPM23 Field

Location:
23

Description:
When set, the [hpmcounter23](#) CSR (an alias of [mhpmcounter23](#)) is accessible to
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When [scouteren.HPM23](#) is also set, [hpmcounter23](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM23](#) is also set, [hpmcounter23](#) is further accessible to VS-mode.

When [hcounteren.HPM23](#) && [scouteren.HPM23](#) are both set, [hpmcounter23](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcouteren.HPM24 Field

Location:
24

Description:
When set, the [hpmcounter24](#) CSR (an alias of [mhpmcounter24](#)) is accessible to
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When [scouteren.HPM24](#) is also set, [hpmcounter24](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM24](#) is also set, [hpmcounter24](#) is further accessible to VS-mode.

When [hcounteren.HPM24](#) && [scouteren.HPM24](#) are both set, [hpmcounter24](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounteren.HPM25 Field

Location:

25

Description:

When set, the [hpmcounter25](#) CSR (an alias of [mhpmcounter25](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM25](#) is also set, [hpmcounter25](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM25](#) is also set, [hpmcounter25](#) is further accessible to VS-mode.

When [hcounteren.HPM25](#) && [scounteren.HPM25](#) are both set, [hpmcounter25](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.HPM26 Field

Location:

26

Description:

When set, the [hpmcounter26](#) CSR (an alias of [mhpmcounter26](#)) is accessible to

<%- if ext?(:S) -%>

S-mode.

<%- else -%>

U-mode.

<%- end -%>

<%- if ext?(:S) -%>

When [scounteren.HPM26](#) is also set, [hpmcounter26](#) is further accessible to U-mode.

<%- end -%>

<%- if ext?(:H) -%>

When [hcounteren.HPM26](#) is also set, [hpmcounter26](#) is further accessible to VS-mode.

When [hcounteren.HPM26](#) && [scounteren.HPM26](#) are both set, [hpmcounter26](#) is further accessible to VU-mode.

<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounteren.HPM27 Field

Location:

27

Description:

When set, the [hpmcounter27](#) CSR (an alias of [mhpmcounter27](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>
```

```
<%- if ext?(:S) -%>
When scounteren.HPM27 is also set, hpmcounter27 is further accessible to U-mode.
<%- end -%>
```

```
<%- if ext?(:H) -%>
When hcounteren.HPM27 is also set, hpmcounter27 is further accessible to VS-mode.
```

```
When hcounteren.HPM27 && scounteren.HPM27 are both set, hpmcounter27 is further accessible to VU-mode.
<%- end -%>
```

Type:

- RW
 - RO
- Reset value:**
- UNDEFINED_LEGAL

[mcounteren.HPM28](#) Field

Location:

28

Description:

When set, the [hpmcounter28](#) CSR (an alias of [mhpmcounter28](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>
```

```
<%- if ext?(:S) -%>
When scounteren.HPM28 is also set, hpmcounter28 is further accessible to U-mode.
<%- end -%>
```

```
<%- if ext?(:H) -%>
When hcounteren.HPM28 is also set, hpmcounter28 is further accessible to VS-mode.
```

```
When hcounteren.HPM28 && scounteren.HPM28 are both set, hpmcounter28 is further accessible to VU-mode.
<%- end -%>
```

Type:

- RW
 - RO
- Reset value:**
- UNDEFINED_LEGAL

[mcounteren.HPM29](#) Field

Location:

29

Description:

When set, the [hpmcounter29](#) CSR (an alias of [mhpmcounter29](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
```

```
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When scounteren.HPM29 is also set, hpmcounter29 is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When hcounteren.HPM29 is also set, hpmcounter29 is further accessible to VS-mode.

When hcounteren.HPM29 && scounteren.HPM29 are both set, hpmcounter29 is further accessible to VU-mode.
<%- end -%>
```

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM30](#) Field

Location:

30

Description:

When set, the [hpmcounter30](#) CSR (an alias of [mhpmcounter30](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
When scounteren.HPM30 is also set, hpmcounter30 is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When hcounteren.HPM30 is also set, hpmcounter30 is further accessible to VS-mode.

When hcounteren.HPM30 && scounteren.HPM30 are both set, hpmcounter30 is further accessible to VU-mode.
<%- end -%>
```

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcounteren.HPM31](#) Field

Location:

31

Description:

When set, the [hpmcounter31](#) CSR (an alias of [mhpmcounter31](#)) is accessible to

```
<%- if ext?(:S) -%>
S-mode.
<%- else -%>
U-mode.
<%- end -%>

<%- if ext?(:S) -%>
```

When [scounteren.HPM31](#) is also set, [hpmcounter31](#) is further accessible to U-mode.
<%- end -%>

<%- if ext?(:H) -%>
When [hcounteren.HPM31](#) is also set, [hpmcounter31](#) is further accessible to VS-mode.

When [hcounteren.HPM31](#) && [scounteren.HPM31](#) are both set, [hpmcounter31](#) is further accessible to VU-mode.
<%- end -%>

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

C.39. mcountinhibit

Machine Counter Inhibit

Bits to inhibit (stops counting) performance counters.

The counter-inhibit register `mcountinhibit` is a **WARL** register that controls which of the hardware performance-monitoring counters increment. The settings in this register only control whether the counters increment; their accessibility is not affected by the setting of this register.

When the CY, IR, or HPM n bit in the `mcountinhibit` register is clear, the `mcycle`, `minstret`, or `mhpmcounter $n$` register increments as usual. When the CY, IR, or HPM n _bit is set, the corresponding counter does not increment.

The `mcycle` CSR may be shared between harts on the same core, in which case the `mcountinhibit.CY` field is also shared between those harts, and so writes to `mcountinhibit.CY` will be visible to those harts.

If the `mcountinhibit` register is not implemented, the implementation behaves as though the register were set to zero.



When the `mcycle` and `minstret` counters are not needed, it is desirable to conditionally inhibit them to reduce energy consumption. Providing a single CSR to inhibit all counters also allows the counters to be atomically sampled.

Because the `mtime` counter can be shared between multiple cores, it cannot be inhibited with the `mcountinhibit` mechanism.

C.39.1. Attributes

CSR Address	0x320
Defining extension	Sm
Length	32-bit
Privilege Mode	M

C.39.2. Format

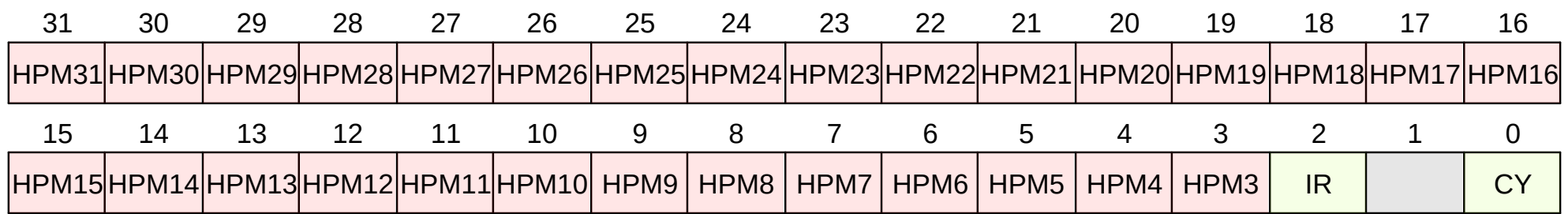


Figure 39. mcountinhibit format

C.39.3. Field Summary

Name	Location	Type	Reset Value
<code>mcountinhibit.CY</code>	0	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.IR</code>	2	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.HPM3</code>	3	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.HPM4</code>	4	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.HPM5</code>	5	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.HPM6</code>	6	RW	UNDEFINED_LEGAL
		RO	
<code>mcountinhibit.HPM7</code>	7	RW	UNDEFINED_LEGAL
		RO	

Name	Location	Type	Reset Value
mcount inhibit. HPM8	8	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM9	9	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM10	10	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM11	11	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM12	12	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM13	13	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM14	14	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM15	15	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM16	16	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM17	17	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM18	18	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM19	19	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM20	20	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM21	21	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM22	22	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM23	23	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM24	24	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM25	25	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM26	26	RW	UNDEFINED_LEGAL
		RO	
mcount inhibit. HPM27	27	RW	UNDEFINED_LEGAL
		RO	

Name	Location	Type	Reset Value
mcountinhibit.HPM28	28	RW	UNDEFINED_LEGAL
		RO	
mcountinhibit.HPM29	29	RW	UNDEFINED_LEGAL
		RO	
mcountinhibit.HPM30	30	RW	UNDEFINED_LEGAL
		RO	
mcountinhibit.HPM31	31	RW	UNDEFINED_LEGAL
		RO	

C.39.4. Fields

[mcountinhibit.CY](#) Field

Location:
0

Description:
When set, [mcycle.COUNT](#) stops counting in all privilege modes.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

[mcountinhibit.IR](#) Field

Location:
2

Description:
When set, [minstret.COUNT](#) stops counting in all privilege modes.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

[mcountinhibit.HPM3](#) Field

Location:
3

Description:
[when="COUNTINHIBIT_EN[3] == true"]
When set, [hpmcounter3.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[3] == false"]
Since hpmcounter3 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM4 Field

Location:
4

Description:
[when="COUNTINHIBIT_EN[4] == true"]
When set, [hpmcounter4.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[4] == false"]
Since hpmcounter4 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM5 Field

Location:
5

Description:
[when="COUNTINHIBIT_EN[5] == true"]
When set, [hpmcounter5.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[5] == false"]
Since hpmcounter5 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM6 Field

Location:
6

Description:
[when="COUNTINHIBIT_EN[6] == true"]
When set, [hpmcounter6.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[6] == false"]
Since hpmcounter6 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM7 Field

Location:

7

Description:

[when="COUNTINHIBIT_EN[7] == true"]
When set, [hpmcounter7.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[7] == false"]
Since hpmcounter7 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM8 Field

Location:

8

Description:

[when="COUNTINHIBIT_EN[8] == true"]
When set, [hpmcounter8.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[8] == false"]
Since hpmcounter8 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM9 Field

Location:

9

Description:

[when="COUNTINHIBIT_EN[9] == true"]
When set, [hpmcounter9.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[9] == false"]
Since hpmcounter9 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM10 Field

Location:

10

Description:

[when="COUNTINHIBIT_EN[10] == true"]
When set, [hpmcounter10.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[10] == false"]
Since hpmcounter10 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhbit.HPM11](#) Field

Location:

11

Description:

[when="COUNTINHIBIT_EN[11] == true"]
When set, [hpmcounter11.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[11] == false"]
Since hpmcounter11 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhbit.HPM12](#) Field

Location:

12

Description:

[when="COUNTINHIBIT_EN[12] == true"]
When set, [hpmcounter12.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[12] == false"]
Since hpmcounter12 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhbit.HPM13](#) Field

Location:

13

Description:

[when="COUNTINHIBIT_EN[13] == true"]
When set, [hpmcounter13.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[13] == false"]

Since hpmcounter13 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM14 Field

Location:

14

Description:

[when="COUNTINHIBIT_EN[14] == true"]
When set, [hpmcounter14.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[14] == false"]
Since hpmcounter14 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM15 Field

Location:

15

Description:

[when="COUNTINHIBIT_EN[15] == true"]
When set, [hpmcounter15.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[15] == false"]
Since hpmcounter15 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM16 Field

Location:

16

Description:

[when="COUNTINHIBIT_EN[16] == true"]
When set, [hpmcounter16.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[16] == false"]
Since hpmcounter16 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM17 Field

Location:
17

Description:
[when="COUNTINHIBIT_EN[17] == true"]
When set, [hpmcounter17.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[17] == false"]
Since hpmcounter17 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM18 Field

Location:
18

Description:
[when="COUNTINHIBIT_EN[18] == true"]
When set, [hpmcounter18.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[18] == false"]
Since hpmcounter18 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM19 Field

Location:
19

Description:
[when="COUNTINHIBIT_EN[19] == true"]
When set, [hpmcounter19.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[19] == false"]
Since hpmcounter19 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM20 Field

Location:

20

Description:

[when="COUNTINHIBIT_EN[20] == true"]
When set, [hpmcounter20.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[20] == false"]
Since hpmcounter20 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM21 Field

Location:

21

Description:

[when="COUNTINHIBIT_EN[21] == true"]
When set, [hpmcounter21.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[21] == false"]
Since hpmcounter21 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM22 Field

Location:

22

Description:

[when="COUNTINHIBIT_EN[22] == true"]
When set, [hpmcounter22.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[22] == false"]
Since hpmcounter22 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM23 Field

Location:

23

Description:

[when="COUNTINHIBIT_EN[23] == true"]
When set, [hpmcounter23.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[23] == false"]
Since hpmcounter23 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhibit](#).**HPM24** Field

Location:

24

Description:

[when="COUNTINHIBIT_EN[24] == true"]
When set, [hpmcounter24.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[24] == false"]
Since hpmcounter24 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhibit](#).**HPM25** Field

Location:

25

Description:

[when="COUNTINHIBIT_EN[25] == true"]
When set, [hpmcounter25.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[25] == false"]
Since hpmcounter25 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mcountinhibit](#).**HPM26** Field

Location:

26

Description:

[when="COUNTINHIBIT_EN[26] == true"]
When set, [hpmcounter26.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[26] == false"]

Since hpmcounter26 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM27 Field

Location:

27

Description:

[when="COUNTINHIBIT_EN[27] == true"]
When set, [hpmcounter27.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[27] == false"]
Since hpmcounter27 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM28 Field

Location:

28

Description:

[when="COUNTINHIBIT_EN[28] == true"]
When set, [hpmcounter28.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[28] == false"]
Since hpmcounter28 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mcounthinhibit.HPM29 Field

Location:

29

Description:

[when="COUNTINHIBIT_EN[29] == true"]
When set, [hpmcounter29.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[29] == false"]
Since hpmcounter29 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM30 Field

Location:
30

Description:
[when="COUNTINHIBIT_EN[30] == true"]
When set, [hpmcounter30.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[30] == false"]
Since hpmcounter30 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

mcounthinhibit.HPM31 Field

Location:
31

Description:
[when="COUNTINHIBIT_EN[31] == true"]
When set, [hpmcounter31.COUNT](#) stops counting in all privilege modes.

[when="COUNTINHIBIT_EN[31] == false"]
Since hpmcounter31 is not implemented, this field is read-only zero.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

C.40. mcycle

Machine Cycle Counter

Counts the number of clock cycles executed by the processor core on which the hart is running. The counter has 64-bit precision on all RV32 and RV64 harts.

The [mcycle](#) CSR may be shared between harts on the same core, in which case writes to [mcycle](#) will be visible to those harts. The platform should provide a mechanism to indicate which harts share an [mcycle](#) CSR.

C.40.1. Attributes

CSR Address	0xb00
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.40.2. Format

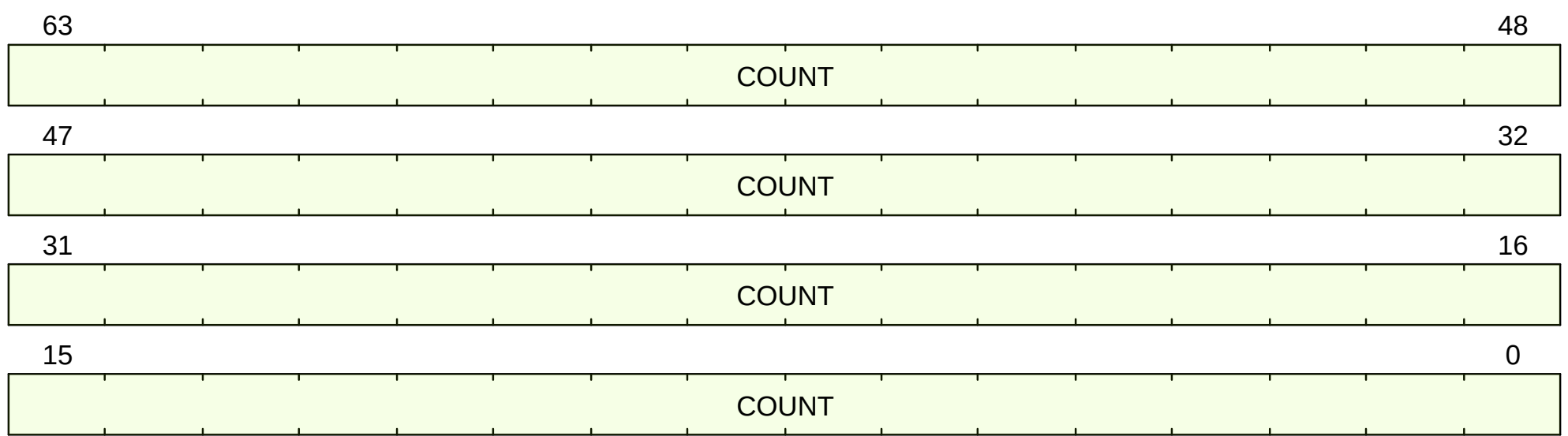


Figure 40. mcycle format

C.40.3. Field Summary

Nam e	Location	Type	Reset Value
mcycle.COUNT	63:0	RW-RH	UNDEFINED_LEGAL

C.40.4. Fields

[mcycle.COUNT](#) Field

Location:

63:0

Description:

Cycle counter.

<%- if ext?(:Zicntr) -%>
Aliased as [cycle](#).
<%- end -%>

Increments every cycle unless:

- [mcountinhibit.CY](#) <%- if ext?(:Smcdeleg) -%>or its alias [scountinhibit.CY](#)<%- end -%> is set <%- if ext?(:Smcntrpmf) -%>
- [mcyclecfg.MINH](#) is set and the current privilege level is M <%- if ext?(:S) -%>
- [mcyclecfg.SINH](#) <%- if ext?(:Sccfg) -%>or its alias [instretcfg.SINH](#)<%- end -%> is set and the current privilege level is (H)S <%- end -%>

```
<%- if ext?(:U) -%>
```

- `mcyclecfg.UINH` <%- if ext?(:Sccfg) -%>or its alias `instretcfg.SINH`<%- end -%> is set and the current privilege level is U

```
<%- end -%>
```

```
<%- if ext?(:H) -%>
```

- `mcyclecfg.VSINH` <%- if ext?(:Sccfg) -%>or its alias `instretcfg.SINH`<%- end -%> is set and the current privilege level is VS

- `mcyclecfg.VUINH` <%- if ext?(:Sccfg) -%>or its alias `instretcfg.SINH`<%- end -%> is set and the current privilege level is VU

```
<%- end -%>
```

```
<%- end -%>
```

Type:

RW-RH

Reset value:

UNDEFINED_LEGAL

C.40.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through `csrrw`), the following determines the written value:

```
COUNT = # since writes to this register may not be hart-local, it must be handled
# as a special case
if (xlen() == 32) {
    return sw_write_mcycle({read_mcycle()[63:31], csr_value.COUNT[31:0]});
} else {
    return sw_write_mcycle(csr_value.COUNT);
}
```

C.40.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return read_mcycle();
```

C.41. medeleg

Machine Exception Delegation

Controls exception delegation from M-mode to (H)S-mode <%- if ext?:(H) -%> or, in conjunction with [hedeleg](#), to VS-mode <%- end -%> .

An exception cause is delegated to (H)S-mode when all of the following hold:

- The corresponding field in [medeleg](#) is set.
- The current privilege level is not M-mode. <%- if ext?:(H) -%>
- The same field in [hedeleg](#) is clear. <%- end -%>

<%- if ext?:(H) -%> An exception cause is delegated to VS-mode when all of the following hold:

- The corresponding field in [medeleg](#) is set.
- The corresponding field in [hedeleg](#) is set.
- The current privilege level is not M-mode or HS-mode. <%- end -%>

Otherwise, an exception cause is handled by M-mode.

See [interrupt documentation](#) for more details.

C.41.1. Attributes

CSR Address	0x302
Defining extension	S
Length	64-bit
Privilege Mode	M

C.41.2. Format

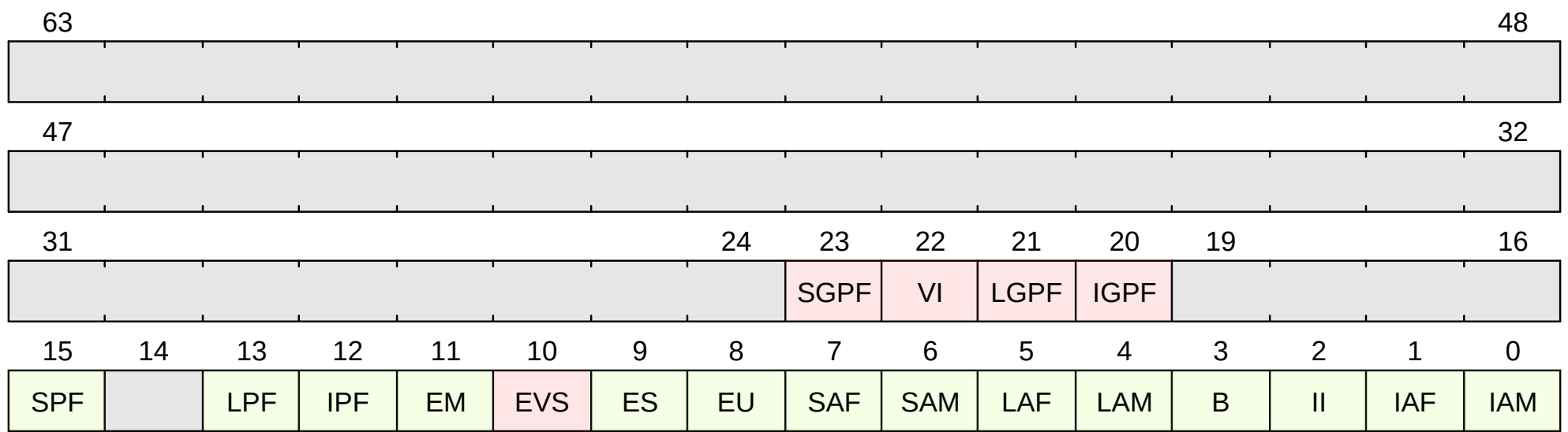


Figure 41. medeleg format

C.41.3. Field Summary

Nam e	Location	Type	Reset Value
medeleg.IAM	0	RW	UNDEFINED_LEGAL
medeleg.IAF	1	RW	UNDEFINED_LEGAL
medeleg.II	2	RW	UNDEFINED_LEGAL
medeleg.B	3	RW	UNDEFINED_LEGAL
medeleg.LAM	4	RW	UNDEFINED_LEGAL

Nam e	Location	Type	Reset Value
medeleg.LAF	5	RW	UNDEFINED_LEGAL
medeleg.SAM	6	RW	UNDEFINED_LEGAL
medeleg.SAF	7	RW	UNDEFINED_LEGAL
medeleg.EU	8	RW	UNDEFINED_LEGAL
medeleg.ES	9	RW	UNDEFINED_LEGAL
medeleg.EVS	10	RW	UNDEFINED_LEGAL
medeleg.EM	11	RO	0
medeleg.IPF	12	RW	UNDEFINED_LEGAL
medeleg.LPF	13	RW	UNDEFINED_LEGAL
medeleg.SPF	15	RW	UNDEFINED_LEGAL
medeleg.IGPF	20	RW	UNDEFINED_LEGAL
medeleg.LGPF	21	RW	UNDEFINED_LEGAL
medeleg.VI	22	RW	UNDEFINED_LEGAL
medeleg.SGPF	23	RW	UNDEFINED_LEGAL

C.41.4. Fields

[medeleg.IAM](#) Field

Location:

0

Description:

Instruction Address Misaligned

Delegates Instruction Address Misaligned exceptions to (H)S-mode.

<%- if ext?(:H) -%>

Instruction Address Misaligned exceptions may be further delegated to VS-mode if [hedeleg.IAM](#) is also set.

<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

<%- if ext?(:H) -%>

```
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.IAM .2+! hedeleg.IAM 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.IAM 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

medeleg.IAF Field

Location:

1

Description:

Instruction Access Fault

Delegates Instruction Access Fault exceptions to (H)S-mode.

<%- if ext?(:H) -%>

Instruction Access Fault exceptions may be further delegated to VS-mode if hedeleg.IAM is also set.

<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

The handling mode is determined as follows:

<%- if ext?(:H) -%>

```
[separator="!",%autowidth, %footer]
```

!===

.2+! medeleg.IAF .2+! hedeleg.IAF 4+^.>! Current Mode

>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M

! 0 ! 1 ! M ! M ! M ! M

! 1 ! 0 ! M ! HS ! HS ! HS

! 1 ! 1 ! M ! HS ! VS ! VS

!===

<%- else -%>

```
[separator="!",%autowidth, %footer]
```

!===

.2+! medeleg.IAF 2+^.>! Current Mode

>h! M-mode .>h! S-mode

! 0 ! M ! M

! 1 ! M ! S

!===

<%- end -%>

Type:

RW

Reset value:
UNDEFINED_LEGAL

medeleg.II Field

Location:
2

Description:
Illegal Instruction

Delegates Illegal Instruction exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Illegal Instruction exceptions may be further delegated to VS-mode if [hedeleg.II](#) is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.II .2+! hedeleg.II 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.II 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.B Field

Location:
3

Description:
Breakpoint

Delegates Breakpoint exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Breakpoint exceptions may be further delegated to VS-mode if [hedeleg.B](#) is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
```



```
!===
.2+! medeleg.B .2+! hedeleg.B 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.B 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.LAM Field

Location:
4

Description:
Load Address Misaligned

Delegates Load Address Misaligned exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Load Address Misaligned exceptions may be further delegated to VS-mode if hedeleg.LAM is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

[when,"MISALIGNED_LDST == true"]
Note that because this implementation supports misaligned loads, this exception will never occur.
However, the writable bit should be presented anyway.

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LAM .2+! hedeleg.LAM 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LAM 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.LAF Field

Location:
5

Description:
Load Access Fault

Delegates Load Access Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Load Access Fault exceptions may be further delegated to VS-mode if hedeleg.LAF is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LAF .2+! hedeleg.LAF 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LAF 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.SAM Field

Location:
6

Description:
Store/AMO Address Misaligned

Delegates Store/AMO Address Misaligned exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Store/AMO Address Misaligned exceptions may be further delegated to VS-mode if hedeleg.SAM is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

[when,"MISALIGNED_LDST == true && MISALIGNED_AMO == true"]

Note that because the implementation supports misaligned stores and misaligned AMOs (or no AMOs), this exception will never occur. Even so, the writable bit should be presented anyway.

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SAM .2+! hedeleg.SAM 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SAM 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

medeleg.SAF Field

Location:

7

Description:

Store/AMO Access Fault

Delegates Store/AMO Access Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Store/AMO Access Fault exceptions may be further delegated to VS-mode if hedeleg.SAM is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SAF .2+! hedeleg.SAF 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SAF 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
```

```
! 1 ! M ! S
!===
<%- end -%>
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

medeleg.EU Field

Location:

8

Description:

Environment Call from U-Mode

Delegates Environment Call from U-mode exceptions to (H)S-mode.

```
<%- if ext?(:H) -%>
Environment Call from U-mode exceptions may be further delegated to VS-mode if hedeleg.EU is also set.
<%- end -%>
```

Exceptions are never taken into a less-privileged mode, regardless of medeleg.

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.EU .2+! hedeleg.EU 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode
```

```
! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.EU 2+^.>! Current Mode
.>h! M-mode .>h! S-mode
```

```
! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

medeleg.ES Field

Location:

9

Description:

Environment Call from S-Mode

Delegates Environment Call from S-mode exceptions to (H)S-mode.

```
<%- if ext?(:H) -%>
Environment Call from S-mode exceptions cannot be delegated to VS-mode.
<%- end -%>
```

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.ES 2+^.>! Current Mode
.>h! M-mode .>h! \(H\)S-mode
```

```
! 0 ! M ! M
! 1 ! M ! (H)S
!===
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

[medeleg.EVS](#) Field

Location:
10

Description:
Environment Call from VS-Mode

Delegates Environment Call from VS-mode exceptions to (H)S-mode.

```
<%- if ext?(:H) -%>
Environment Call from S-mode exceptions cannot be delegated to VS-mode.
<%- end -%>
```

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.EVS 2+^.>! Current Mode
.>h! M-mode .>h! \(H\)S-mode
```

```
! 0 ! M ! M
! 1 ! M ! (H)S
!===
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

[medeleg.EM](#) Field

Location:
11

Description:
Environment Call from M-Mode

An Environment Call from M-mode cannot be delegated, so this is a read-only field.

All Environment Call from M-mode exceptions are taken by M-mode.

Type:
RO

Reset value:

0

medeleg.IPF Field

Location:

12

Description:

Instruction Page Fault

Delegates Instruction Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Instruction Page Fault exceptions may be further delegated to VS-mode if [hedeleg.IPF](#) is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.IPF .2+! hedeleg.IPF 4+^,>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.IPF 2+^,>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

medeleg.LPF Field

Location:

13

Description:

Load Page Fault

Delegates Load Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Load Page Fault exceptions may be further delegated to VS-mode if [hedeleg.LPF](#) is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
```

```
!===
.2+! medeleg.LPF .2+! hedeleg.LPF 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LPF 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.SPF Field

Location:
15

Description:
Store/AMO Page Fault

Delegates Store/AMO Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Store/AMO Page Fault exceptions may be further delegated to VS-mode if [hedeleg.SPF](#) is also set.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
<%- if ext?(:H) -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SPF .2+! hedeleg.SPF 4+^.>! Current Mode
.>h! M-mode .>h! HS-mode .>h! VS-mode .>h! VU-mode

! 0 ! 0 ! M ! M ! M ! M
! 0 ! 1 ! M ! M ! M ! M
! 1 ! 0 ! M ! HS ! HS ! HS
! 1 ! 1 ! M ! HS ! VS ! VS
!===
<%- else -%>
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.LPF 2+^.>! Current Mode
.>h! M-mode .>h! S-mode

! 0 ! M ! M
! 1 ! M ! S
!===
<%- end -%>
```

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.IGPF Field

Location:
20

Description:
Instruction Guest Page Fault

Delegates Instruction Guest Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Instruction Guest Page Fault exceptions *cannot be delegated to VS-mode*.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

[separator="!",%autowidth, %footer]
!===
.2+! [medeleg.IGPF](#) 2+^.>! Current Mode
>h! ~~M-mode~~ >h! (H)S-mode

! 0 ! M ! M
! 1 ! M ! HS
!===

Type:
RW

Reset value:
UNDEFINED_LEGAL

medeleg.LGPF Field

Location:
21

Description:
Load Guest Page Fault

Delegates Load Guest Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Load Guest Page Fault exceptions *cannot be delegated to VS-mode*.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

[separator="!",%autowidth, %footer]
!===
.2+! [medeleg.LGPF](#) 2+^.>! Current Mode
>h! ~~M-mode~~ >h! (H)S-mode

! 0 ! M ! M
! 1 ! M ! HS
!===

Type:
RW

Reset value:
UNDEFINED_LEGAL

Location:

22

Description:

Virtual Instruction

Delegates Virtual Instruction exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Virtual Instruction exceptions *cannot be delegated to VS-mode*.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.VI 2+^.>! Current Mode
.>h! M-mode .>h! (H)S-mode
```

```
! 0 ! M ! M
! 1 ! M ! HS
!===
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

Location:

23

Description:

Store/AMO Guest Page Fault

Delegates Store/AMO Guest Page Fault exceptions to (H)S-mode.
<%- if ext?(:H) -%>
Store/AMO Guest Page Fault exceptions *cannot be delegated to VS-mode*.
<%- end -%>

Exceptions are never taken into a less-privileged mode, regardless of [medeleg](#).

The handling mode is determined as follows:

```
[separator="!",%autowidth, %footer]
!===
.2+! medeleg.SGPF 2+^.>! Current Mode
.>h! M-mode .>h! (H)S-mode
```

```
! 0 ! M ! M
! 1 ! M ! HS
!===
```

Type:

RW

Reset value:

UNDEFINED_LEGAL

C.42. mepc

Machine Exception Program Counter

Written with the PC of an instruction on an exception or interrupt taken in M-mode.

Also controls where the hart jumps on an exception return from M-mode.

C.42.1. Attributes

CSR Address	0x341
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.42.2. Format

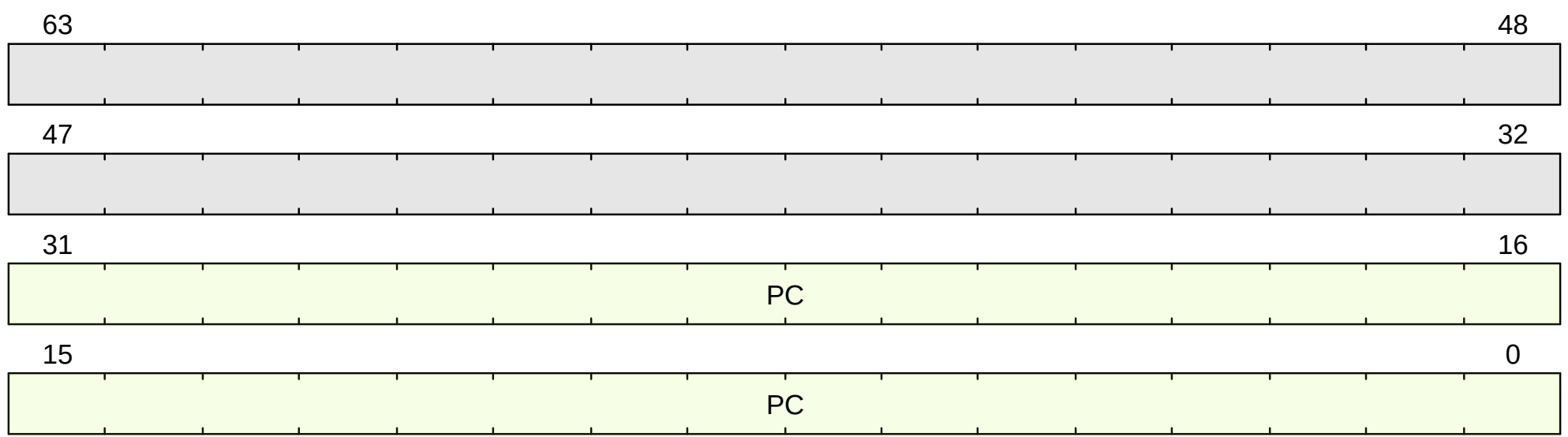


Figure 42. mepc format

C.42.3. Field Summary

Na me	Location	Type	Reset Value
mepc.PC	63:0	RW-RH	0

C.42.4. Fields

[mepc.PC](#) Field

Location:

63:0

Description:

When a trap is taken into M-mode, [mepc.PC](#) is written with the virtual address of the instruction that was interrupted or that encountered the exception. Otherwise, [mepc.PC](#) is never written by the implementation, though it may be explicitly written by software.

On an exception return from M-mode (from the MRET instruction), control transfers to the virtual address read out of [mepc.PC](#).

[when,"ext?:(C)"]
Because PCs are always halfword-aligned, bit 0 of [mepc.PC](#) is always read-only 0.

[when,"!ext?:(C)"]
Because PCs are always word-aligned, bits 1:0 of [mepc.PC](#) are always read-only 0.

[when,"ext?:(C) && MUTABLE_MISA_C == true"]
When [misa.C](#) is clear, bit 1 is masked to zero. Writes to bit 1 are still captured, and

may be visible on the next read with [misa.C](#) is set.

Type:

RW-RH

Reset value:

0

C.42.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
PC = return csr_value.PC & ~64'b1;
```

C.42.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (implemented?(ExtensionName::C) && CSR[misa].C == 1'b1) {  
    return CSR[mepc].PC & ~64'b1;  
} else {  
    return CSR[mepc].PC;  
}
```

C.43. mhartid

Machine Hart ID

Reports the unique hart-specific ID in the system.

C.43.1. Attributes

CSR Address	0xf14
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.43.2. Format

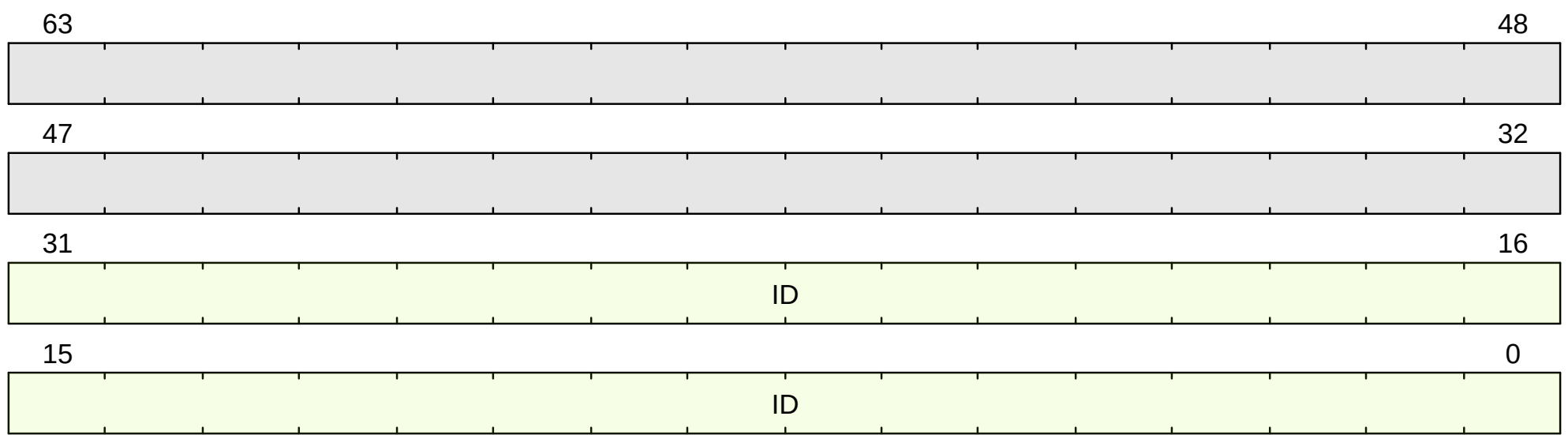


Figure 43. mhartid format

C.43.3. Field Summary

Na me	Location	Type	Reset Value
mhartid.ID	63:0	RO	UNDEFINED_LEGAL

C.43.4. Fields

[mhartid.ID](#) Field

Location:
63:0

Description:
hart-specific ID.

Type:
RO

Reset value:
UNDEFINED_LEGAL

C.43.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return hartid();
```

C.44. mie

Machine Interrupt Enable

mip.yaml#/description

C.44.1. Attributes

CSR Address	0x304
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.44.2. Format

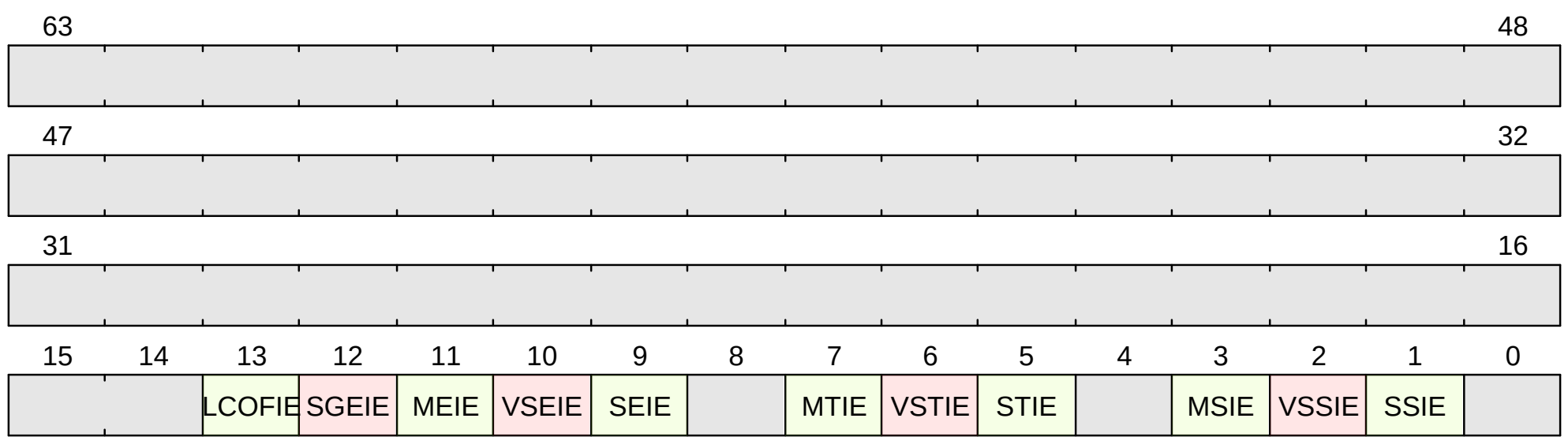


Figure 44. mie format

C.44.3. Field Summary

Nam e	Location	Type	Reset Value
mie. SSIE	1	RW	0
mie. VSSI E	2	RW	0
mie. MSI E	3	RW	0
mie. STIE	5	RW	0
mie. VSTI E	6	RW	0
mie. MTI E	7	RW	0
mie. SEIE	9	RW	0
mie. VSEI E	10	RW	0
mie. MEI E	11	RW	0
mie. SGEI E	12	RW	0

Name	Location	Type	Reset Value
mie.LCOFIE	13	RW	0

C.44.4. Fields

mie.SSIE Field

Location:

1

Description:

Enables Supervisor Software Interrupts.

Alias of **sie.SSIE** when **mideleg.SSI** is set. Otherwise, **sie.SSIE** is read-only 0.

Type:

RW

Reset value:

0

mie.VSSIE Field

Location:

2

Description:

Enables Virtual Supervisor Software Interrupts.

Alias of **hie.VSSIE**.

Alias of **vsie.SSIE** when **hideleg.VSSI** is set. Otherwise, **vseie.SSIE** is read-only 0.

Alias of **sie.SSIE** when **hideleg.VSSI** is set and the current mode is VS or VU
(Because **mie** is inaccessible in VS or VU mode, this alias can never be observed by software).

Type:

RW

Reset value:

0

mie.MSIE Field

Location:

3

Description:

Enables Machine Software Interrupts.

Type:

RW

Reset value:

0

mie.STIE Field

Location:

5

Description:

Enables Supervisor Timer Interrupts.

Alias of [sip](#) when [mideleg.STI](#) is set. Otherwise, [sip](#) is read-only 0.

Type:

RW

Reset value:

0

[mie.VSTIE](#) Field

Location:

6

Description:

Enables Virtual Supervisor Timer Interrupts.

Alias of [hie.VSTIE](#).

Alias of [vsie.STIE](#) when [hideleg.VSTI](#) is set. Otherwise, [vseie.STIE](#) is read-only 0.

Alias of [sie.STIE](#) when [hideleg.VSTI](#) is set and the current mode is VS or VU
(Because [mie](#) is inaccessible in VS or VU mode, this alias can never be observed by software).

Type:

RW

Reset value:

0

[mie.MTIE](#) Field

Location:

7

Description:

Enables Machine Timer Interrupts.

Type:

RW

Reset value:

0

[mie.SEIE](#) Field

Location:

9

Description:

Enables Supervisor External Interrupts.

Alias of [sie.SEIE](#) when [mideleg.SEI](#) is set. Otherwise, [sie.SEIE](#) is read-only 0.

Type:

RW

Reset value:

0

[mie.VSEIE](#) Field

Location:

10

Description:

Enables Virtual Supervisor External Interrupts.

Alias of `hie.VSEIE`.

Alias of `vsie.SEIE` when `hideleg.VSEI` is set. Otherwise, `vseie.SEIE` is read-only 0.

Alias of `sie.SEIE` when `hideleg.VSEI` is set and the current mode is VS or VU
(Because `mie` is inaccessible in VS or VU mode, this alias can never be observed by software).

Type:

RW

Reset value:

0

mie.MEIE Field

Location:

11

Description:

Enables Machine External Interrupts.

Type:

RW

Reset value:

0

mie.SGEIE Field

Location:

12

Description:

Enables Supervisor Guest External Interrupts

Alias of `hie.SGEIE`.

Type:

RW

Reset value:

0

mie.LCOFIE Field

Location:

13

Description:

Enables Local Counter Overflow Interrupts.

Alias of `sie.LCOFIE` when `mideleg.LCOFI` is set. Otherwise, `sie.LCOFIE` is an independent writable bit when `mvien.LCOFI` is set or is read-only 0.

Alias of `vsip.LCOFIE` when `hideleg.LCOFI` is set. Otherwise, `vsip.LCOFIE` is read-only 0.

Type:

RW

Reset value:

0

C.45. mimpid

Machine Implementation ID

Reports the vendor-specific implementation ID.

The [mimpid](#) CSR provides a unique encoding of the version of the processor implementation. This register must be readable in any implementation, but a value of 0 can be returned to indicate that the field is not implemented. The Implementation value should reflect the design of the RISC-V processor itself and not any surrounding system.



The format of this field is left to the provider of the architecture source code, but will often be printed by standard tools as a hexadecimal string without any leading or trailing zeros, so the Implementation value can be left-justified (i.e., filled in from most-significant nibble down) with subfields aligned on nibble boundaries to ease human readability.

C.45.1. Attributes

CSR Address	0xf13
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.45.2. Format



Figure 45. mimpid format

C.45.3. Field Summary

Name	Location	Type	Reset Value
mimpid.Implementation	63:0	RO	UNDEFINED_LEGAL

C.45.4. Fields

[mimpid.Implementation](#) Field

Location:

63:0

Description:

Vendor-specific implementation ID.

Type:

RO

Reset value:

UNDEFINED_LEGAL

C.46. minstret

Machine Instructions Retired Counter

Counts the number of instructions retired by this hart from some arbitrary start point in the past.



Instructions that cause synchronous exceptions, including [ecall](#) and [ebreak](#), are not considered to retire and hence do not increment the [minstret](#) CSR.

C.46.1. Attributes

CSR Address	0xb02
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.46.2. Format

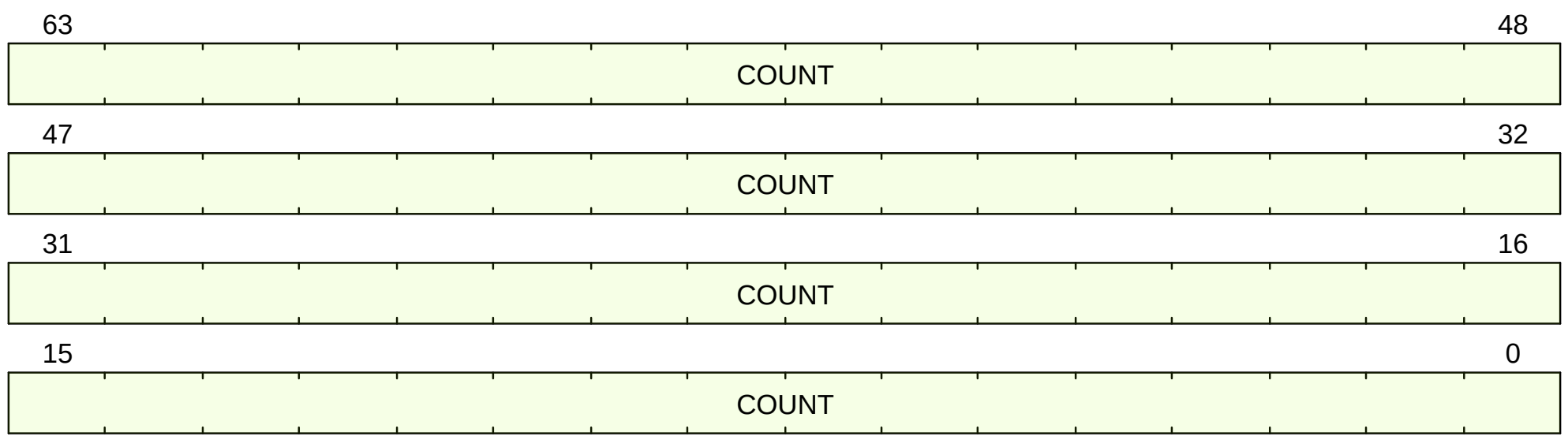


Figure 46. minstret format

C.46.3. Field Summary

Name	Location	Type	Reset Value
minstret.CO UNT	63:0	RW-H	UNDEFINED_LEGAL

C.46.4. Fields

[minstret.COUNT](#) Field

Location:
63:0

Description:
Instructions retired counter.

<%- if ext?(:Zicntr) -%>
Aliased as [instret.COUNT](#).
<%- end -%>

Increments every time an instruction retires unless:

- [mcountinhibit.IR](#) <%- if ext?(:Smcdeleg) -%>or its alias [scountinhibit.IR](#)<%- end -%> is set
<%- if ext?(:Smcntrpmf) -%>
- [minstretcfg.MINH](#) is set and the current privilege level is M
<%- if ext?(:S) -%>
- [minstretcfg.SINH](#) <%- if ext?(:Ssccfg) -%>or its alias [instretcfg.SINH](#)<%- end -%> is set and the current privilege level is (H)S
<%- end -%>
<%- if ext?(:U) -%>
- [minstretcfg.UINH](#) <%- if ext?(:Ssccfg) -%>or its alias [instretcfg.SINH](#)<%- end -%> is set and the current privilege level is U

<%- end -%>
<%- if ext?(:H) -%>

- [minstretcfg.VSINH](#) <%- if ext?(:Sccfg) -%>or its alias [instretcfg.SINH](#)<%- end -%> is set and the current privilege level is VS
 - [minstretcfg.VUINH](#) <%- if ext?(:Sccfg) -%>or its alias [instretcfg.SINH](#)<%- end -%> is set and the current privilege level is VU
- <%- end -%>
<%- end -%>

An instruction that causes an exception, notably including MRET/SRET,
does not retire and does not cause [minstret.COUNT](#) to increment.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

C.47. mip

Machine Interrupt Pending

The [mie](#) and [mip](#) CSRs are MXLEN-bit read/write registers used when the CLINT or PLIC interrupt controllers are present. Note that the CLINT refers to an interrupt controller used by some RISC-V implementations but isn’t a ratified RISC-V International standard.

The [mip](#) CSR contains information on pending interrupts, while [mie](#) is the corresponding CSR containing interrupt enable bits. Interrupt cause number *i* (as reported in the [mcause](#) CSR) corresponds to bit *i* in both [mip](#) and [mie](#). Bits 15:0 are allocated to standard interrupt causes only, while bits 16 and above are designated for platform use.



Interrupts designated for platform use may be designated for custom use at the platform’s discretion.

An interrupt *i* will trap to M-mode (causing the privilege mode to change to M-mode) if all of the following are true:

- either the current privilege mode is M and the MIE bit in the [mstatus](#) register is set, or the current privilege mode has less privilege than M-mode;
- bit *i* is set in both [mip](#) and [mie](#)
- if register [mideleg](#) exists, bit *i* is not set in [mideleg](#).

These conditions for an interrupt trap to occur must be evaluated in a bounded amount of time from when an interrupt becomes, or ceases to be, pending in [mip](#), and must also be evaluated immediately following the execution of an xRET instruction or an explicit write to a CSR on which these interrupt trap conditions expressly depend (including [mip](#), [mie](#), [mstatus](#), and [mideleg](#)).

Interrupts to M-mode take priority over any interrupts to lower privilege modes.

Each individual bit in register [mip](#) may be writable or may be read-only. When bit *i* in [mip](#) is writable, a pending interrupt *i* can be cleared by writing 0 to this bit. If interrupt *i* can become pending but bit *i* in [mip](#) is read-only, the implementation must provide some other mechanism for clearing the pending interrupt.

A bit in [mie](#) must be writable if the corresponding interrupt can ever become pending. Bits of [mie](#) that are not writable must be read-only zero.



The machine-level interrupt registers handle a few root interrupt sources which are assigned a fixed service priority for simplicity, while separate external interrupt controllers can implement a more complex prioritization scheme over a much larger set of interrupts that are then muxed into the machine-level interrupt sources.

The non-maskable interrupt is not made visible via the [mip](#) register as its presence is implicitly known when executing the NMI trap handler.

If supervisor mode is implemented, bits [mip](#).SEIP and [mie](#).SEIE are the interrupt-pending and interrupt-enable bits for supervisor-level external interrupts. SEIP is writable in [mip](#), and may be written by M-mode software to indicate to S-mode that an external interrupt is pending. Additionally, the platform-level interrupt controller may generate supervisor-level external interrupts. Supervisor-level external interrupts are made pending based on the logical-OR of the software-writable SEIP bit and the signal from the external interrupt controller. When [mip](#) is read with a CSR instruction, the value of the SEIP bit returned in the [rd](#) destination register is the logical-OR of the software-writable bit and the interrupt signal from the interrupt controller, but the signal from the interrupt controller is not used to calculate the value written to SEIP. Only the software-writable SEIP bit participates in the read-modify-write sequence of a CSRRS or CSRRC instruction.



For example, if we name the software-writable SEIP bit [B](#) and the signal from the external interrupt controller [E](#), then if [csrrs t0, mip, t1](#) is executed, [t0\[9\]](#) is written with [B || E](#), then [B](#) is written with [B || t1\[9\]](#). If [csrrw t0, mip, t1](#) is executed, then [t0\[9\]](#) is written with [B || E](#), and [B](#) is simply written with [t1\[9\]](#). In neither case does [B](#) depend upon [E](#).

The SEIP field behavior is designed to allow a higher privilege layer to mimic external interrupts cleanly, without losing any real external interrupts. The behavior of the CSR instructions is slightly modified from regular CSR accesses as a result.

If supervisor mode is implemented, bits [mip](#).STIP and [mie](#).STIE are the interrupt-pending and interrupt-enable bits for supervisor-level timer interrupts. STIP is writable in [mip](#), and may be written by M-mode software to deliver timer interrupts to S-mode.

If supervisor mode is implemented, bits [mip](#).SSIP and [mie](#).SSIE are the interrupt-pending and interrupt-enable bits for supervisor-level software interrupts. SSIP is writable in [mip](#) and may also be set to 1 by a platform-specific interrupt controller.

<% if ext?(:Sscofpmf) -%> bits [mip](#).LCOFIP and [mie](#).LCOFIE are the interrupt-pending and interrupt-enable bits for local counter-overflow interrupts. LCOFIP is read-write in [mip](#) and reflects the occurrence of a local counter-overflow overflow interrupt request resulting from any of the [mhpmevent n](#).OF bits being set. <% end -%>

Multiple simultaneous interrupts destined for M-mode are handled in the following decreasing priority order: MEI, MSI, MTI, SEI, SSI, STI, LCOFI.



The machine-level interrupt fixed-priority ordering rules were developed with the following rationale.

Interrupts for higher privilege modes must be serviced before interrupts for lower privilege modes to support preemption.

The platform-specific machine-level interrupt sources in bits 16 and above have platform-specific priority, but are typically chosen

to have the highest service priority to support very fast local vectored interrupts.

External interrupts are handled before internal (timer/software) interrupts as external interrupts are usually generated by devices that might require low interrupt service times.

Software interrupts are handled before internal timer interrupts, because internal timer interrupts are usually intended for time slicing, where time precision is less important, whereas software interrupts are used for inter-processor messaging. Software interrupts can be avoided when high-precision timing is required, or high-precision timer interrupts can be routed via a different interrupt path. Software interrupts are located in the lowest four bits of `mip` as these are often written by software, and this position allows the use of a single CSR instruction with a five-bit immediate.

Restricted views of the `mip` and `mie` registers appear as the `sip` and `sie` registers for supervisor level. If an interrupt is delegated to S-mode by setting a bit in the `mideleg` register, it becomes visible in the `sip` register and is maskable using the `sie` register. Otherwise, the corresponding bits in `sip` and `sie` are read-only zero.

C.47.1. Attributes

CSR Address	0x344
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.47.2. Format

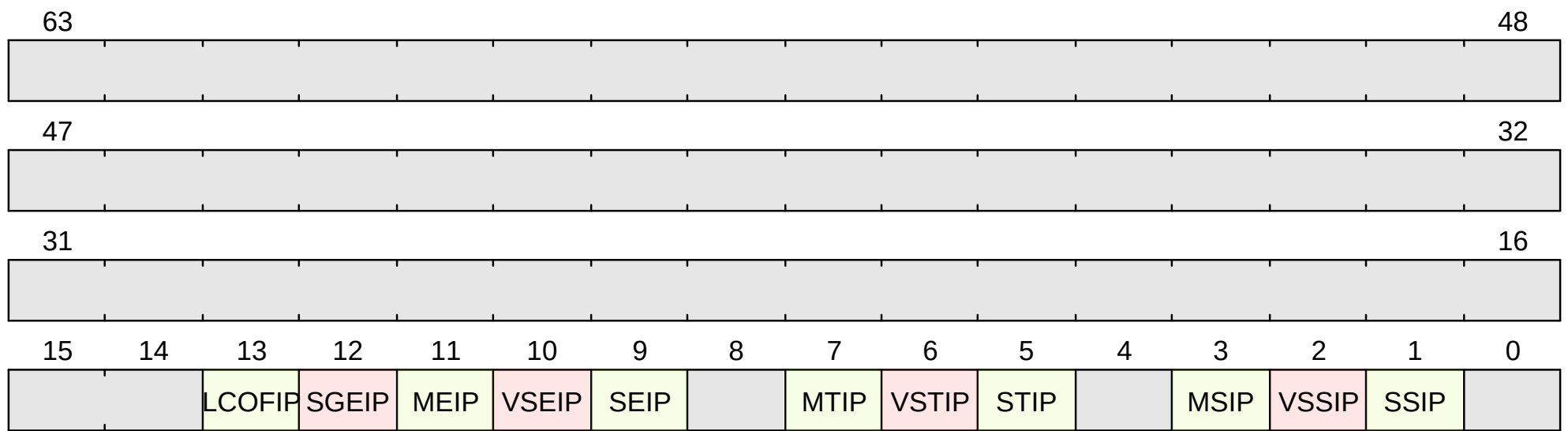


Figure 47. mip format

C.47.3. Field Summary

Nam e	Location	Type	Reset Value
mip. SSIP	1	RW	0
mip. VSSIP	2	RW	0
mip. MSIP	3	RO	0
mip. STIP	5	RW	0
mip. VSTIP	6	RO-H	0
mip. MTIP	7	RO-H	0
mip. SEIP	9	RW-H	0
mip. VSEIP	10	RO-H	0

Name	Location	Type	Reset Value
mip.MEIP	11	RO-H	0
mip.SGEIP	12	RO-H	0
mip.LCOFIP	13	RW-H	0

C.47.4. Fields

mip.SSIP Field

Location:

1

Description:

Supervisor Software Interrupt Pending

Reports the current pending state of an (H)S-mode software interrupt, which is generated by writing to this field.

<%- if ext?(:Smaia) -%>
When using AIA/IMSIC, IPIs are expected to be delivered as external interrupts and SSIP is not backed by any hardware update (aside from any aliasing effects). However, SSIP is still writable by M-mode software and, when written, can be used to generate an S-mode Software Interrupt.
<%- end -%>

<% if ext?(:Smaia) %>_Aliases_<% else %>_Alias_<% end %>:

- sip.SSIP when mideleg.SSI is set
<%- if ext?(:Smaia) -%>
- mvip.SSIP
<%- end -%>

Type:

RW

Reset value:

0

mip.VSSIP Field

Location:

2

Description:

Virtual Supervisor Software Interrupt Pending

Reports the current pending state of a VS-mode software interrupt, which is generated by writing to this field.

<%- if ext?(:Smaia) -%>
When using AIA/IMSIC, IPIs are expected to be delivered as external interrupts and VSSIP is not backed by any hardware update (aside from any aliased writes). However, VSSIP is still writable by M-mode software and, when written, can be used to generate a VS-mode Software Interrupt.
<%- end -%>

Aliases:

- hip.VSSIP

- `hvip.VSSIP`
- `vsip.SSIP` when `hideleg.VSSI` is set

Type:

RW

Reset value:

0

mip.MSIP Field

Location:

3

Description:

Machine Software Interrupt Pending

Unused field.

<%- if ext?(:Smaia) -%>

With AIA/IMSIC, IPIs are delivered as external interrupts. As a result, this bit is unused and hardwired to 0.

<%- end -%>

Type:

RO

Reset value:

0

mip.STIP Field

Location:

5

Description:

Supervisor Timer Interrupt Pending

Reports the current pending state of an (H)S-mode timer interrupt

<%- if ext?(:Sstc) -%>

, which is normally controlled by the `stimecmp` CSR.

<%- else -%>

, which is generated by software by writing to `mip.STIP`<% if ext?(:Smaia) %>or its alias `mvip.STIP`<% end %>.

<%- end -%>

<%-if ext?(:Sstc) -%>

When `menvcfg.STCE` is set, `mip.STIP` is RO-H, and is completely controlled by the timer interrupt device (using `stimecmp`).

When `menvcfg.STCE` is clear, `mip.STIP` is RW, and M-mode software may write the bit to inject a Supervisor Timer Interrupt.

<%- end -%>

<% if ext?(:Smaia) %>_Aliases_<% else %>_Alias_<% end %>:

- `sip.STIP` when `mideleg.STI` is set (though `sip.STIP` is a read-only view)
<%- if ext?(:Smaia) -%>
- `mvip.STIP` when when `menvcfg.STCE` is clear
<%- end -%>

Type:

RW

Reset value:

0

mip.VSTIP Field

Location:

6

Description:

Virtual Supervisor Timer Interrupt Pending

Reports the current pending state of a VS-mode timer interrupt

<%- if ext?(:Sstc) -%>

, which is normally controlled by the `vstimecmp` CSR, but can also be injected by the hypervisor through `hvip.VSTIP`.

<%- else -%>

, which is generated by M-mode and/or HS-mode software by writing to `hvip.VSTIP`.

<%- end -%>

<%-if ext?(:Sstc) -%>

When `menvcfg.STCE` is set (enabling the `Sstc` extension), `mip.VSTIP` is the logical OR of `hvip.VSTIP` and the VS-level interrupt signal generated by the timer device (controlled by the value of `vstimecmp`).

When `menvcfg.STCE` is clear (disabling the `Sstc` extension), `mip.VSTIP` is exactly the value of `hvip.VSTIP`.

<%- end -%>

`mip.VSTIP` is never writable. If VS-mode software wants to clear the bit, it must do so

<%- if ext?(:Sstc) -%>

by writing the `vstimecmp` register or

<%- end -%>

by calling into the hypervisor (which can then clear `hvip.VSTIP`).

Aliases:

- `hip.VSTIP`
- `vsip.STIP` when `hideleg.VSTI` is set
- `hvip.VSTIP` <% if ext?(:Sstc) %>when `menvcfg.STCE` is clear<% end %> (though `hvip.VSTIP` is writable)

Type:

RO-H

Reset value:

0

mip.MTIP Field

Location:

7

Description:

Machine Timer Interrupt Pending

Reports the current pending state of an M-mode timer interrupt.

Bit is controlled by the timer device (using `mtimecmp`), and is not writable.

Type:

RO-H

Reset value:

0

mip.SEIP Field

Location:

9

Description:

Supervisor External Interrupt Pending

Reports the current pending state of an (H)S-mode external interrupt.

This field has two parts: a software-writable shadow value and a wire from the interrupt controller.
The value presented to software in the bit on a CSR read is the logical OR of the software-writable value and the interrupt controller value.
When software writes this bit, only the shadow value is updated (the interrupt controller is not notified of the write).

<%- if ext?(:Smaia) -%>
The software-writable shadow value is aliased in `mvip.SEIP` (`Smaia` extension).
<%- end -%>

Alias:

- `sip.SEIP` when `mideleg.SEI` is set (though `sip.SEIP` is read-only)

Type:

RW-H

Reset value:

0

mip.VSEIP Field

Location:

10

Description:

Virtual Supervisor External Interrupt Pending

Reports the current pending state of a VS-mode external interrupt.

This field is the logical OR of `hvip.VSEIP` and the wire coming from the interrupt controller.

The field is not writable by software

<%- if ext?(:Smaia) -%>
(*i.e.*, unlike the behavior of `mip.SEIP`/`mvip.SEIP`, attempted writes to `mip.VSEIP` do not propagate to `hvip.VSEIP`)
<%- end -%>

1. +

Aliases:

- `hip.VSEIP`
- `vsip.SEIP` when `hideleg.VSEI` is set

Type:

RO-H

Reset value:

0

mip.MEIP Field

Location:

11

Description:

Machine External Interrupt Pending

Reports the current pending state of an M-mode external interrupt.

MEIP is controlled by the external interrupt controller <% if ext?(:Smaia) %>(AIA) <% end %>.
It is not writable by software.

Type:

RO-H

Reset value:

0

mip.SGEIP Field

Location:

12

Description:

Supervisor Guest External Interrupt Pending

Read-only summary of any pending Supervisor Guest External Interrupt Pending, i.e.: the logical-OR reduction of the hgeip register.

Alias:

- hip.SGEIP

Type:

RO-H

Reset value:

0

mip.LCOFIP Field

Location:

13

Description:

Local Counter Overflow Interrupt pending

<%- if ext?(:H) -%>
When hideleg.LCOFI is set,
vsip.LCOFIP, sip.LCOFIP, and mip.LCOFIP are all aliases.
<%- end -%>

When a counter overflow interrupt occurs, a hidden sticky bit is set.

Software writes 0 to mip.LCOFIP to clear the pending interrupt.

<% if ext?(:H) %>_Aliases_<% else %>_Alias_<% end %>:

- sip.LCOFIP when mideleg.LCOFI is set
<%- if ext?(:H) -%>
- vsip.LCOFIP when hideleg.LCOFI is set
<%- end -%>

Type:

RW-H

Reset value:

0

C.47.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return $bits(CSR[CSR[mip]]) | ((CSR[misa].S == 1'b1 && pending_smode_external_interrupt) ? 10'h200 : 0);
```

C.48. misa

Machine ISA Control

Reports the XLEN and "major" extensions supported by the ISA.

C.48.1. Attributes

CSR Address	0x301
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.48.2. Format

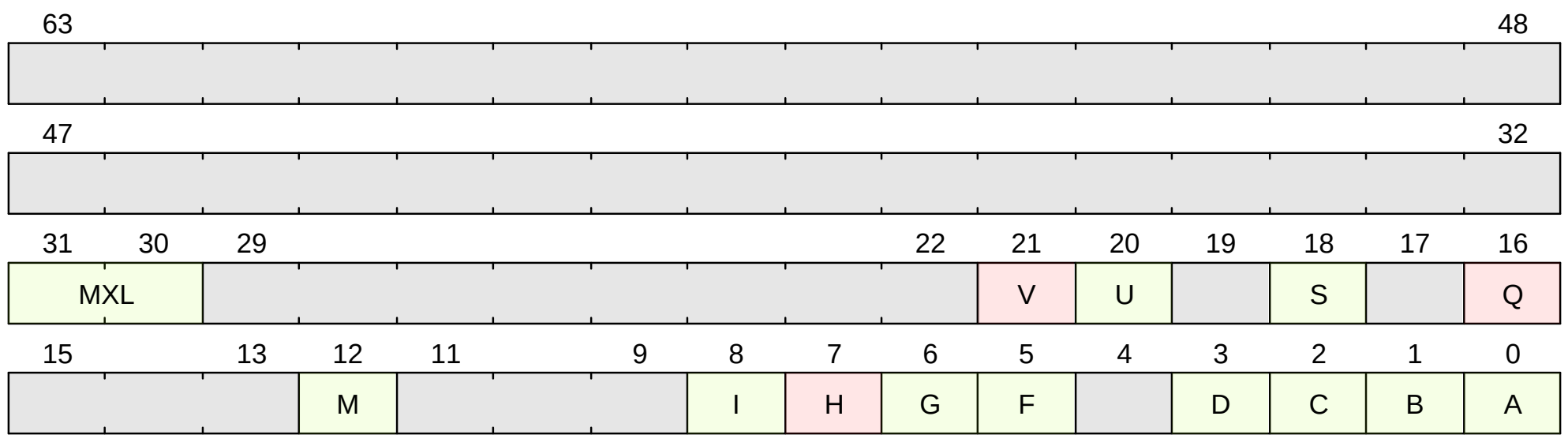


Figure 48. misa format

C.48.3. Field Summary

Na me	Location	Type	Reset Value
mis a.M XL	63:62	RO	2
mis a.A	0	RW	1
		RO	
mis a.B	1	RW	1
		RO	
mis a.C	2	RW	1
		RO	
mis a.D	3	RW	1
		RO	
mis a.F	5	RW	1
		RO	
mis a.G	6	RO-H	1
		RO	
mis a.H	7	RW	UNDEFINED_LEGAL
		RO	
mis a.I	8	RO	1
mis a.M	12	RW	1
		RO	

Na me	Location	Type	Reset Value
mis a.Q	16	RW	1
		RO	
mis a.S	18	RW	1
		RO	
mis a.U	20	RW	1
		RO	
mis a.V	21	RW	1
		RO	

C.48.4. Fields

[misa.MXL](#) Field

Location:
63:62

Description:
XLEN in M-mode.

Type:
RO

Reset value:
2

[misa.A](#) Field

Location:
0

Description:
Indicates support for the [A](#) (atomic) extension.

[when,"MUTABLE_MISA_A == true"]
Writing 0 to this field will cause all atomic instructions to raise an **IllegalInstruction** exception.

Type:

RW

RO

Reset value:
1

[misa.B](#) Field

Location:
1

Description:
Indicates support for the [B](#) (bitmanip) extension.

[when,"MUTABLE_MISA_B == true"]
Writing 0 to this field will cause all bitmanip instructions to raise an **IllegalInstruction** exception.

Type:

RW

RO

Reset value:

1

misa.C Field

Location:

2

Description:

Indicates support for the **C** (compressed) extension.

[when,"MUTABLE_MISA_C == true"]

Writing 0 to this field will cause all compressed instructions to raise an **IllegalInstruction** exception.

Additionally, IALIGN becomes 32.

Type:

RW

RO

Reset value:

1

misa.D Field

Location:

3

Description:

Indicates support for the **D** (double precision float) extension.

[when,"MUTABLE_MISA_D == true"] + — + Writing 0 to this field will cause all double-precision floating point instructions to raise an **IllegalInstruction** exception.

Additionally, the upper 32-bits of the f registers will read as zero. + — +

Type:

RW

RO

Reset value:

1

misa.F Field

Location:

5

Description:

Indicates support for the **F** (single precision float) extension.

[when,"MUTABLE_MISA_F == true"] + — + Writing 0 to this field will cause all floating point (single and double precision) instructions to raise an **IllegalInstruction** exception.

Writing 0 to this field with **misa.D** set will result in UNDEFINED behavior. + — +

Type:

RW

RO

Reset value:

1

misa.G Field

Location:

6

Description:

Indicates support for all of the following extensions: [I](#), [A](#), [M](#), [F](#), [D](#).

Type:

RO-H

RO

Reset value:

1

misa.H Field

Location:

7

Description:

Indicates support for the [H](#) (hypervisor) extension.

[when,"MUTABLE_MISA_H == true"]

Writing 0 to this field will cause all attempts to enter VS- or VU- mode, execute a hypervisor instruction, or access a hypervisor CSR to raise an **IllegalInstruction** fault.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

misa.I Field

Location:

8

Description:

Indicates support for the [I](#) (base) extension.

Type:

RO

Reset value:

1

misa.M Field

Location:

12

Description:

Indicates support for the [M](#) (integer multiply/divide) extension.

[when,"MUTABLE_MISA_M == true"]

Writing 0 to this field will cause all attempts to execute an integer multiply or divide instruction to raise an **IllegalInstruction** exception.

Type:

RW

RO

Reset value:

1

misa.Q Field

Location:

16

Description:

Indicates support for the [Q](#) (quad precision float) extension.

[when,"MUTABLE_MISA_Q == true"] +—+ Writing 0 to this field will cause all quad-precision floating point instructions to raise an [IllegalInstruction](#) exception. +—+

Type:

RW

RO

Reset value:

1

misa.S Field

Location:

18

Description:

Indicates support for the [S](#) (supervisor mode) extension.

[when,"MUTABLE_MISA_S == true"]
Writing 0 to this field will cause all attempts to enter S-mode or access S-mode state to raise an exception.

Type:

RW

RO

Reset value:

1

misa.U Field

Location:

20

Description:

Indicates support for the [U](#) (user mode) extension.

[when,"MUTABLE_MISA_U == true"]
Writing 0 to this field will cause all attempts to enter U-mode to raise an exception.

Type:

RW

RO

Reset value:

1

misa.V Field

Location:

21

Description:

Indicates support for the [V](#) (vector) extension.

[when,"MUTABLE_MISA_V == true"]

Writing 0 to this field will cause all attempts to execute a vector instruction to raise an [IllegalInstruction](#) trap.

Type:

RW

RO

Reset value:

1

C.48.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
MXL = csr_value.MXL
A = csr_value.A
B = csr_value.B
C = csr_value.C
D = csr_value.D
F = if (csr_value.F == 0 && csr_value.D == 1) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
}

# fall-through; write the intended value
return csr_value.F;

G = csr_value.G
H = csr_value.H
I = csr_value.I
M = csr_value.M
Q = if ((csr_value.F == 0 || csr_value.D == 0) && csr_value.Q == 1) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
}

# fall-through; write the intended value
return csr_value.Q;

S = csr_value.S
U = csr_value.U
V = csr_value.V
```

C.48.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
return CSR[misa].MXL `<< (xlen() - 2 | (CSR[misa].V `<< 21) | (CSR[misa].U `<< 20) | (CSR[misa].S `<< 18) | (CSR[misa].Q `<< 16) |
(CSR[misa].M `<< 12) | (CSR[misa].I `<< 7) | (CSR[misa].H `<< 6) | ((CSR[misa].A & CSR[misa].M & CSR[misa].F & CSR[misa].D) `<< 5)
| (CSR[misa].F `<< 4) | (CSR[misa].D `<< 3) | (CSR[misa].C `<< 2) | (CSR[misa].B `<< 1) | CSR[misa].A);
```

C.49. mscratch

Machine Scratch Register

Scratch register for software use. Bits are not interpreted by hardware.

C.49.1. Attributes

CSR Address	0x340
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.49.2. Format

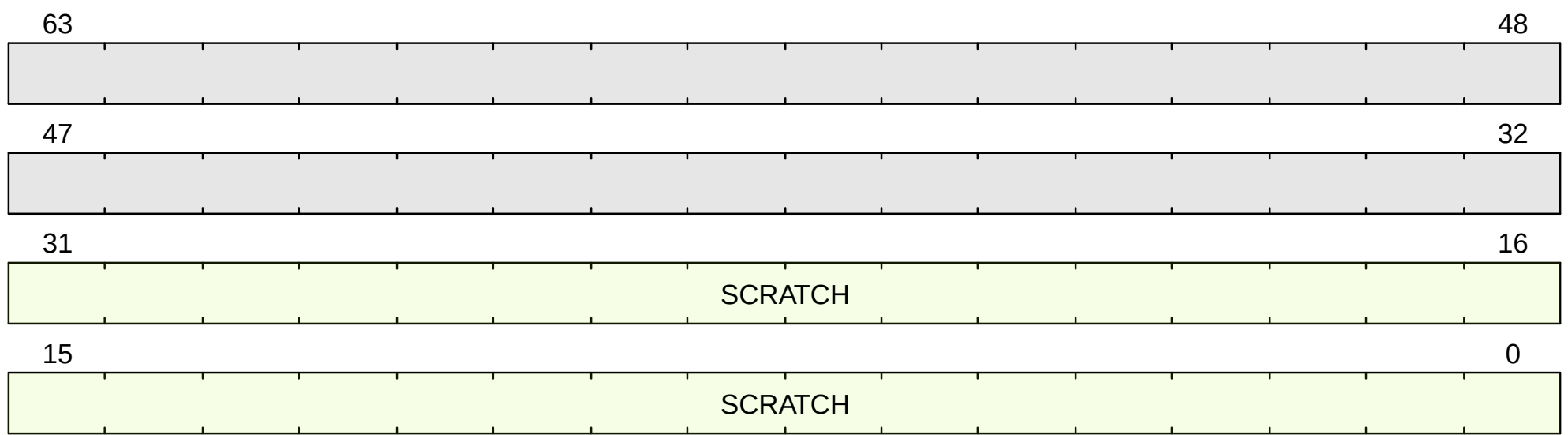


Figure 49. mscratch format

C.49.3. Field Summary

Name	Location	Type	Reset Value
mscratch.SCRATCH	63:0	RW	0

C.49.4. Fields

[mscratch.SCRATCH](#) Field

Location:

63:0

Description:

Scratch value

Type:

RW

Reset value:

0

C.50. mstatus

Machine Status

The mstatus register tracks and controls the hart’s current operating state.

C.50.1. Attributes

CSR Address	0x300
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.50.2. Format

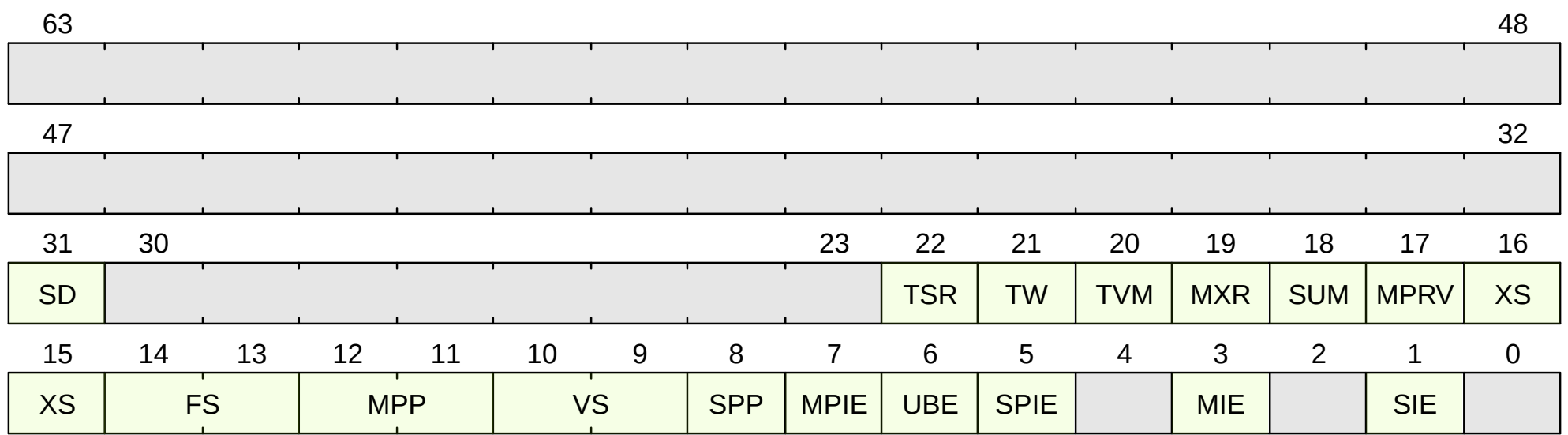


Figure 50. mstatus format

C.50.3. Field Summary

Nam e	Location	Type	Reset Value
mstatus.SD	63	RO-H RO-H RO	UNDEFINED_LEGAL
mstatus.MDT	42	RW-H	UNDEFINED_LEGAL
mstatus.MPV	39	RW-H	UNDEFINED_LEGAL
mstatus.GVA	38	RW-H	0
mstatus.MBE	37	RW RO	UNDEFINED_LEGAL
mstatus.SBE	36	RW RO	UNDEFINED_LEGAL
mstatus.SXL	35:34	RW RO	UNDEFINED_LEGAL
mstatus.UXL	33:32	RW RO	UNDEFINED_LEGAL
mstatus.TSR	22	RW	UNDEFINED_LEGAL

Name	Location	Type	Reset Value
mstatus.TW	21	RW	UNDEFINED_LEGAL
mstatus.TVM	20	RO RW	UNDEFINED_LEGAL
mstatus.MXR	19	RW	UNDEFINED_LEGAL
mstatus.SUM	18	RW RO	UNDEFINED_LEGAL
mstatus.MPRV	17	RW-H RO	0
mstatus.XS	16:15	RO	0
mstatus.FS	14:13	RW-H RO RO RW	UNDEFINED_LEGAL
mstatus.MPP	12:11	RW-H	3
mstatus.VS	10:9	RW-H RO RO RW	UNDEFINED_LEGAL
mstatus.SPP	8	RW-H	UNDEFINED_LEGAL
mstatus.MPIE	7	RW-H	UNDEFINED_LEGAL
mstatus.UBE	6	RW RO	UNDEFINED_LEGAL
mstatus.SPIE	5	RW-H RO	UNDEFINED_LEGAL
mstatus.MIE	3	RW-H	0
mstatus.SIE	1	RW-H RO	UNDEFINED_LEGAL

C.50.4. Fields

mstatus.SD Field

Location:

63

Description:

Read-only bit that summarizes whether either the FS, XS, or VS

fields signal the presence of some dirty state.

Type:

RO-H

RO-H

RO

Reset value:

UNDEFINED_LEGAL

mstatus.MDT Field



MDT is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

42

Description:

Written to 1 when entering M-mode from an exception/interrupt.
When returning via an MRET instruction, the bit is written to 0.
On reset is set to 1, and software should write it to 0 when boot sequence is done.
When mstatus.MDT=1, direct write by CSR instruction cannot set mstatus.MIE to 1, if not written together.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

mstatus.MPV Field



MPV is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

39

Description:

Written with the prior virtualization mode when entering M-mode from an exception/interrupt.
When returning via an MRET instruction, the virtualization mode becomes the value of MPV unless MPP=3, in which case the virtualization mode is always 0.
Can also be written by software.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

mstatus.GVA Field



GVA is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

38

Description:

When a trap is taken and a guest virtual address is written into mtval, GVA is set.
When a trap is taken and a guest virtual address is written into mtval, GVA is cleared.

Type:

RW-H

Reset value:

0

mstatus.MBE Field



MBE is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

37

Description:

Controls the endianness of data M-mode (0 = little, 1 = big).
Instructions are always little endian, regardless of the data setting.

[when,"M_MODE_ENDIANNESSESS == little"]
Since the CPU does not support big endian, this is hardwired to 0.

[when,"M_MODE_ENDIANNESSESS == big"]
Since the CPU does not support little endian, this is hardwired to 1.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mstatus.SBE Field



SBE is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

36

Description:

Controls the endianness of S-mode (0 = little, 1 = big).
Instructions are always little endian, regardless of the data setting.

[when,"S_MODE_ENDIANNESSESS == little"]
Since the CPU does not support big endian, this is hardwired to 0.

[when,"S_MODE_ENDIANNESSESS == big"]
Since the CPU does not support little endian, this is hardwired to 1.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mstatus.SXL Field



SXL is only defined in RV64 (`CSR[misa].MXL == 1`)

Location:

35:34

Description:

Sets the effective XLEN for S-mode (0 = 32-bit, 1 = 64-bit, 2 = 128-bit [reserved]).

[when,"SXLEN==32"]

Since the CPU only supports SXLEN==32, this is hardwired to 1.

[when,"SXLEN==64"]

Since the CPU only supports SXLEN==64, this is hardwired to 2.

[when,"SXLEN=3264"] + — + It is not valid to have SXLEN less than UXLEN.

It is UNDEFINED_LEGAL what will happen if a software sets [mstatus.SXL](#) to be greater than [mstatus.UXL](#).

It is UNDEFINED_LEGAL to set the MSB of SXL. + — +

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mstatus.UXL](#) Field



UXL is only defined in RV64 ([CSR\[misa\].MXL == 1](#))

Location:

33:32

Description:

U-mode XLEN.

Sets the effective XLEN for U-mode (1 = 32-bit, 2 = 64-bit, 3 = 128-bit [reserved]).

[when,"UXLEN == 32"]

Since the CPU only supports UXLEN==32, this is hardwired to 1.

[when,"UXLEN == 64"]

Since the CPU only supports UXLEN==64, this is hardwired to 2.

[when,"UXLEN == 3264"] + — + It is not valid to have SXLEN less than UXLEN.

It is UNDEFINED_LEGAL what will happen if a software sets [mstatus.SXL](#) to be greater than [mstatus.UXL](#).

It is UNDEFINED_LEGAL to set the MSB of UXL. + — +

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mstatus.TSR](#) Field

Location:

22

Description:

When 1, attempts to execute the [sret](#) instruction while executing in HS/S-mode will raise an Illegal Instruction exception.

[when,"ext?(:H)"]

Does not affect the behavior of [sret](#) in VS_mode (see [hstatus.VTSR](#)).

Type:

RW

Reset value:
UNDEFINED_LEGAL

mstatus.TW Field

Location:
21

Description:
When 1, the WFI instruction will raise an Illegal Instruction trap after an implementaion-defined wait period when executed in a mode other than M-mode.

When 0, the [wfi](#) instruction is permitted to wait forever in (H)S-mode but must trap after an implementation-defined wait period in U-mode.

Type:
RW

Reset value:
UNDEFINED_LEGAL

mstatus.TVM Field

Location:
20

Description:
When 1, an **Illegal Instruction** trap occurs when

- writing the [satp](#) CSR, executing an [sfence.vma](#), or executing an [sinval.vma](#) while in (H)S-mode (but not VS-mode)
- writing the [hgtap](#) CSR, executing an [hfence.gvma](#), or executing an [hinval.gvma](#) while in HS-mode

Notably, [mstatus.TVM](#) does **not** cause

[*hfence.vvma](#), [sfence.w.inval](#), or [sfence.inval.ir](#) to trap.

- Any additional traps in VS-mode (controlled via [hstatus.VTVM](#) instead).

Type:
RO

RW

Reset value:
UNDEFINED_LEGAL

mstatus.MXR Field

Location:
19

Description:
When 1, loads from pages marked readable **or executable** are allowed.
When 0, loads from pages marked executable raise a Page Fault exception.

Type:
RW

Reset value:
UNDEFINED_LEGAL

mstatus.SUM Field

Location:

18

Description:

When 0, an S-mode read or an M-mode read with mstatus.MPRV=1 and mstatus.MPP=01 to a 'U' (user) page will cause an ILLEGAL INSTRUCTION exception.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

mstatus.MPRV Field

Location:

17

Description:

When 1, loads and stores behave as if the current virtualization mode:privilege level was [mstatus.MPV:mstatus.MPP](#).

[mstatus.MPRV](#) is cleared on any exception return ([mret](#) or [sret](#) instruction, regardless of the trap handler privilege mode).

Type:

RW-H

RO

Reset value:

0

mstatus.XS Field

Location:

16:15

Description:

Summarizes the current state of any custom extension state.
Either 0 - Off, 1 - Initial, 2 - Clean, 3 - Dirty.
Since there are no custom extensions in the base spec, this field is read-only 0.

Type:

RO

Reset value:

0

mstatus.FS Field

Location:

14:13

Description:

When 0, floating point instructions (from F and D extensions) are disabled, and cause **ILLEGAL INSTRUCTION** exceptions.
When a floating point register, or the fCSR register is written, FS obtains the value 3.
Values 1 and 2 are valid write values for software, but are not interpreted by hardware other than to possibly enable a previously-disabled floating point unit.

Type:

RW-H

RO

RO

RW

Reset value:

UNDEFINED_LEGAL

mstatus.MPP Field

Location:

12:11

Description:

Written by hardware in two cases:

- Written with the prior nominal privilege level when entering M-mode from an exception/interrupt.
- Written with 0 when executing an [mret](#) instruction to return from an exception in M-mode.

Can also be written by software without immediate side-effect.

Affects execution in two cases:

- On a return from an exception from M-mode, the machine will enter the privilege level stored in MPP before clearing the field.
- When [mstatus.MPRV](#) is set, loads and stores behave as if the current privilege level were MPP.

Type:

RW-H

Reset value:

3

mstatus.VS Field

Location:

10:9

Description:

When 0, vector instructions (from the V extension) are disabled, and cause ILLEGAL INSTRUCTION exceptions. When a vector register or vector CSR is written, VS obtains the value 3. Values 1 and 2 are valid write values for software, but are not interpreted by hardware other than to possibly enable a previously-disabled vector unit.

Type:

RW-H

RO

RO

RW

Reset value:

UNDEFINED_LEGAL

mstatus.SPP Field

Location:

8

Description:

Written by hardware in two cases:

- Written with the prior nominal privilege level when entering (H)S-mode from an exception/interrupt.
- Written with 0 when executing an [sret](#) instruction to return from an exception in (H)S-mode or (unlikely) M-mode.

Can also be written by software without immediate side-effect.

Affects execution in one case:

- On a return from an exception using the [sret](#) instruction in (H)S-mode or (unlikely) M-mode, the machine will enter the privilege level stored in SPP before clearing the field.

Notably, [mstatus.SPP](#) does not affect exception return in VS-mode (see [vsstatus.SPP](#)).

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

[mstatus.MPIE](#) Field

Location:

7

Description:

Written by hardware in two cases:

- Written with prior value of [mstatus.MIE](#) when entering M-mode from an exception/interrupt.
- Written with the value 1 when returning from an exception in M-mode (via the [mret](#) instruction).

Can also be written by software without immediate side effect.

Other than serving as a record of nested traps as described above, [mstatus.MPIE](#) does not affect execution.

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

[mstatus.UBE](#) Field

Location:

6

Description:

Controls the endianness of U-mode (0 = little, 1 = big).
Instructions are always little endian, regardless of the data setting.

[when,"U_MODE_ENDIANNESSESS == 'little'"]
Since the CPU does not support big endian in U-mode, this is hardwired to 0.

[when,"U_MODE_ENDIANNESSESS == 'big'"]
Since the CPU does not support little endian in U-mode, this is hardwired to 1.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[mstatus.SPIE](#) Field

Location:

5

Description:

Written by hardware in two cases:

- Written with prior value of [mstatus.SIE](#) when entering (H)S-mode from an exception/interrupt.
- Written with the value 1 when returning from an exception via the [sret](#) instruction in (H)S-mode or (unlikely) M-mode.

Can also be written by software without immediate side effect.

Other than serving as a record of nested traps as described above, [mstatus.SPIE](#) does not affect execution.

Type:

RW-H

RO

Reset value:

UNDEFINED_LEGAL

[mstatus.MIE](#) Field

Location:

3

Description:

Written by hardware in two cases:

- Written with the value 0 when entering M-mode from an exception/interrupt.
- Written with the prior value of [mstatus.MPIE](#) when returning from an exception in M-mode (via [mret](#)).

Affects execution by:

- When 0, all interrupts are disabled when the current privilege level is M.
- When 1, interrupts that are not otherwise disabled with a field in [mie](#) are enabled.

Type:

RW-H

Reset value:

0

[mstatus.SIE](#) Field

Location:

1

Description:

Written by hardware in two cases:

- Written with the value 0 when entering (H)S-mode from an exception/interrupt.
- Written with the prior value of [mstatus.SPIE](#) when returning from an exception via [sret](#) in (H)S-mode or (unlikely) M-mode.

Affects execution by:

- When 0, all (H)S-mode interrupts are disabled when the current privilege level is (H)S (M-mode interrupts are still enabled).
- When 1, (H)S-mode interrupts that are not otherwise disabled with a field in [sie](#) are enabled.

Type:

RW-H

RO

Reset value:

UNDEFINED_LEGAL

C.50.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
SD = csr_value.SD
MDT = csr_value.MDT
MPV = csr_value.MPV
GVA = csr_value.GVA
MBE = csr_value.MBE
SBE = csr_value.SBE
SXL = if (csr_value.SXL < csr_value.UXL) {
    return CSR[mstatus].SXL;
} else if (csr_value.SXL < 1 || csr_value.SXL > 2) {
    # SXL != [1, 2] is not defined (3 reserved for RV128, but that isn't ratified)
    return CSR[mstatus].SXL;
} else {
    return csr_value.SXL;
}

UXL = if (csr_value.SXL < csr_value.UXL) {
    return CSR[mstatus].UXL;
} else if (csr_value.UXL < 1 || csr_value.UXL > 2) {
    # UXL != [1, 2] is not defined (3 reserved for RV128, but that isn't ratified)
    return CSR[mstatus].UXL;
} else {
    return csr_value.UXL;
}

TSR = csr_value.TSR
TW = csr_value.TW
TVM = if (CSR[misa].S == 1'b0) {
    return 0;
} else if (MSTATUS_TVM_IMPLEMENTED) {
    return csr_value.TVM;
} else {
    return 0;
}

MXR = csr_value.MXR
SUM = csr_value.SUM
MPRV = csr_value.MPRV
XS = csr_value.XS
FS = if (MISA_CSR_IMPLEMENTED && (CSR[misa].S == 1'b0) && (CSR[misa].F == 1'b0)) {
    # must be read-only-0
    return 0;
}
return $array_includes?(MSTATUS_FS_LEGAL_VALUES, csr_value.FS) ? csr_value.FS : UNDEFINED_LEGAL_DETERMINISTIC;

MPP = if (csr_value.MPP == 2'b01 && !implemented?(ExtensionName::S)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (csr_value.MPP == 2'b00 && !implemented?(ExtensionName::U)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (csr_value.MPP == 2'b10) {
    # never a valid value
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.MPP;
}

VS = if (implemented?(ExtensionName::V) && CSR[misa].V == 1'b1){
    return $array_includes?(MSTATUS_VS_LEGAL_VALUES, csr_value.VS) ? csr_value.VS : UNDEFINED_LEGAL_DETERMINISTIC;
} else if (!implemented?(ExtensionName::S) && !implemented?(ExtensionName::V)) {
    # must be read-only-0
    return 0;
} else {
    # there will be no hardware update in this case because we know the V extension isn't implemented
```

```
    return $array_includes?(MSTATUS_VS_LEGAL_VALUES, csr_value.VS) ? csr_value.VS : UNDEFINED_LEGAL_DETERMINISTIC;
}

SPP = if (csr_value.SPP == 2'b10) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.SPP;
}

MPIE = csr_value.MPIE
UBE = csr_value.UBE
SPIE = csr_value.SPIE
MIE = csr_value.MIE
SIE = csr_value.SIE
```

C.51. mtval

Machine Trap Value

Holds trap-specific information

C.51.1. Attributes

CSR Address	0x343
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.51.2. Format

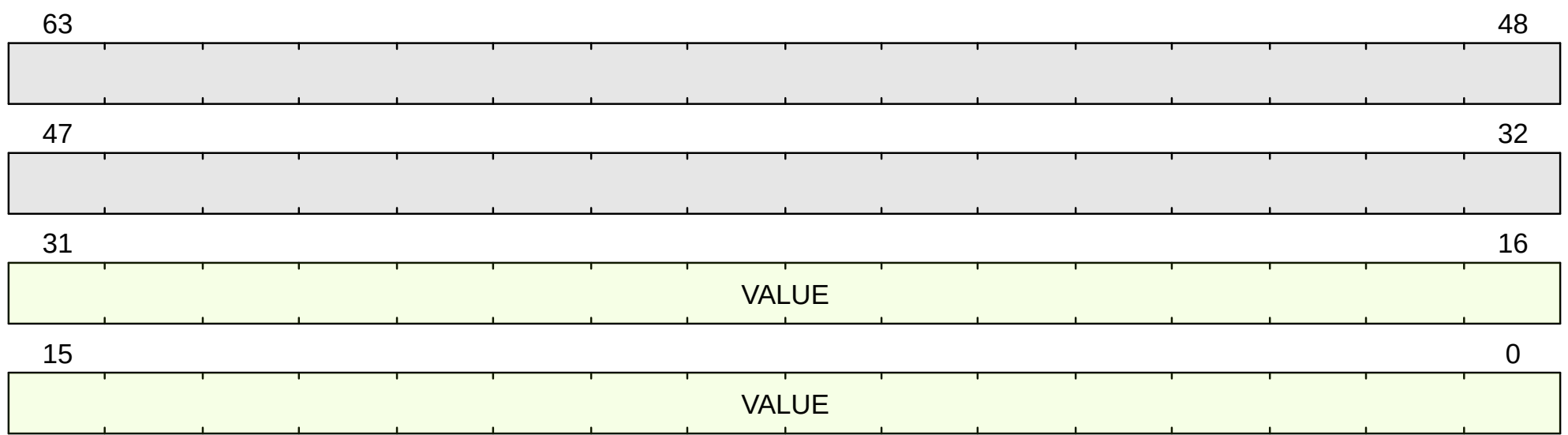


Figure 51. `mtval` format

C.51.3. Field Summary

Nam e	Location	Type	Reset Value
mtval . VALUE	63:0	RW-H	0

C.51.4. Fields

[mtval](#).[VALUE](#) Field

Location:
63:0

Description:
Written with trap-specific information when a trap is taken into M-mode.

The values are:

[separator="!"]
!===
! Exception type ! Value

! [0] Instruction address misaligned ! The misaligned virtual PC (same as the value written to [mepc](#)).
! [1] Instruction access fault ! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the access fault <%- unless ext?(:C) -%>(same as the value written to [mepc](#))<%- end -%>.
! [2] Illegal Instruction ! The encoding of the illegal instruction.
! [3] Breakpoint
! [when,"REPORT_VA_IN_MTVAL_ON_BREAKPOINT == true"]
When caused by an EBREAK instruction, the virtual PC of the breakpoint instruction.

[when,"REPORT_VA_IN_MTVAL_ON_BREAKPOINT == false"]
When caused by an EBREAK instruction, zero.

When caused by a data address (*i.e.*, watchpoint) breakpoint, the faulting virtual address.

When caused by an instruction address breakpoint, the faulting virtual PC.

! [4] Load address misaligned ! The misaligned virtual load address.

! [5] Load access fault

! The part of virtual load address causing in the access fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte load is equally split across a page and the fault occurs on the second page, address + 4 is reported).

(Even though the access fault arises on a physical address, the virtual address is reported)

! [6] Store/AMO address misaligned ! The misaligned virtual store/AMO address.

! [7] Store/AMO access fault

! The virtual store/AMO address causing the access fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte store is equally split across a page and the fault occurs on the second page, address + 4 is reported).

(Even though the access fault arises on a physical address, the virtual address is reported)

! [8] Environment call from U-mode <% if ext?(:H) %>or VU-mode<% end %> ! Zero

! [9] Environment call from (H)S-mode ! Zero

<%- if ext?(:H) -%>

! [10] Environment call from VS-mode ! Zero

<%- end -%>

! [11] Environment call from M-mode ! Zero

! [12] Instruction page fault

! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the page fault

<% unless ext?(:C) %>(same as the value written to [mepc](#))<% end %>.

! [13] Load page fault

! The part of the virtual load address causing in the page fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte load is equally split across a page and the fault occurs on the second page, address + 4 is reported).

! [15] Store/AMO page fault

! The virtual store/AMO address causing in the page fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte store is equally split across a page and the fault occurs on the second page, address + 4 is reported).

<%- if ext?(:H) -%>

! [20] Instruction guest-page fault

! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the fault <% unless ext?(:C) %>(same as the value written to [mepc](#))<% end %>.

The guest physical address is reported in [mtval2](#).

! [21] Load guest-page fault

! The part of the virtual address causing the fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte load is equally split across a page and the fault occurs on the second page, address + 4 is reported).

The guest physical address is reported in [mtval2](#).

! [22] Virtual instruction

! The encoding of the faulting virtual instruction.

! [23] Store/AMO guest-page fault

! The part of the virtual address causing the fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault (e.g., if an 8-byte store is equally split across a page and the fault occurs on the second page, address + 4 is reported).

The guest physical address is reported in [mtval2](#).

<%- end -%>

!===

Type:

RW-H

Reset value:

0

C.52. mtvec

Machine Trap Vector Control

Controls where traps jump.

C.52.1. Attributes

CSR Address	0x305
Defining extension	Sm
Length	64-bit
Privilege Mode	M

C.52.2. Format

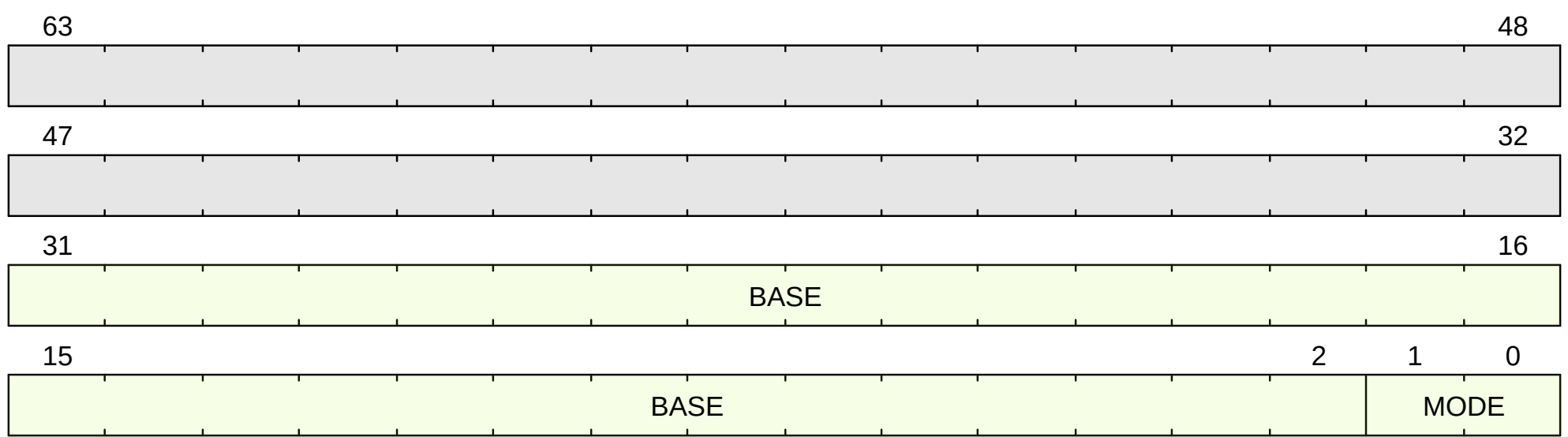


Figure 52. mtvec format

C.52.3. Field Summary

Nam e	Location	Type	Reset Value
mtvec.BA SE	63:2	RO	0
		RW-R	
mtvec.MO DE	1:0	RO	UNDEFINED_LEGAL
		RO	
		RW-R	

C.52.4. Fields

[mtvec.BASE](#) Field

Location:
63:2

Description:
Bits [MXLEN-1:2] of the exception vector physical address for any trap taken in M-mode.

The implementation physical memory map may resitRICT which values are legal in this field.

Type:

RO

RW-R

Reset value:
0

Location:

1:0

Description:

Vectoring mode for asynchronous interrupts.

0 - Direct, 1 - Vectored

When Direct, all synchronous exceptions and asynchronous interrupts jump to (mtvec.BASE << 2).

When Vectored, asynchronous interrupts jump to (mtvec.BASE << 2 + mcause*4) while synchronous exceptions continue to jump to (mtvec.BASE << 2).

Type:

RO

RO

RW-R

Reset value:

UNDEFINED_LEGAL

C.52.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through csrrw), the following determines the written value:

```
BASE = # Base spec says that BASE must be 4-byte aligned, which will always be the case
# implementations may put further constraints on BASE when MODE != Direct
# If that is the case, stvec should have an override for the implementation

if (csr_value.MODE == 0) {
  if ($array_includes?(MTVEC_MODES, 0)) {
    return csr_value.BASE;
  }
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
    return CSR[mtvec].BASE;
  }
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
    return UNDEFINED_LEGAL_DETERMINISTIC;
  }
  unreachable();
} else if (csr_value.MODE == 1) {
  if ($array_includes?(MTVEC_MODES, 1)) {
    return csr_value.BASE;
  }
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
    return CSR[mtvec].BASE;
  }
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
    return UNDEFINED_LEGAL_DETERMINISTIC;
  }
  unreachable();
} else {
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
    return CSR[mtvec].BASE;
  }
  if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
    return UNDEFINED_LEGAL_DETERMINISTIC;
  }
  unreachable();
}

MODE = if (csr_value.MODE == 0) {
  if ($array_includes?(MTVEC_MODES, 0)) {
    return csr_value.MODE;
  } else {
```



```

    if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
        return CSR[mtvec].MODE;
    } else if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
        return UNDEFINED_LEGAL_DETERMINISTIC;
    }
}
} else if (csr_value.MODE == 1) {
    if ($array_includes?(MTVEC_MODES, 1)) {
        return csr_value.MODE;
    } else {
        if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
            return CSR[mtvec].MODE;
        } else if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
            return UNDEFINED_LEGAL_DETERMINISTIC;
        }
    }
} else {
    if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "retain") {
        return CSR[mtvec].MODE;
    } else if (MTVEC_ILLEGAL_WRITE_BEHAVIOR == "custom") {
        return UNDEFINED_LEGAL_DETERMINISTIC;
    }
}
}
unreachable();

```

C.53. mvendorid

Machine Vendor ID

Reports the JEDEC manufacturer ID of the core.

C.53.1. Attributes

CSR Address	0xf11
Defining extension	Sm
Length	32-bit
Privilege Mode	M

C.53.2. Format

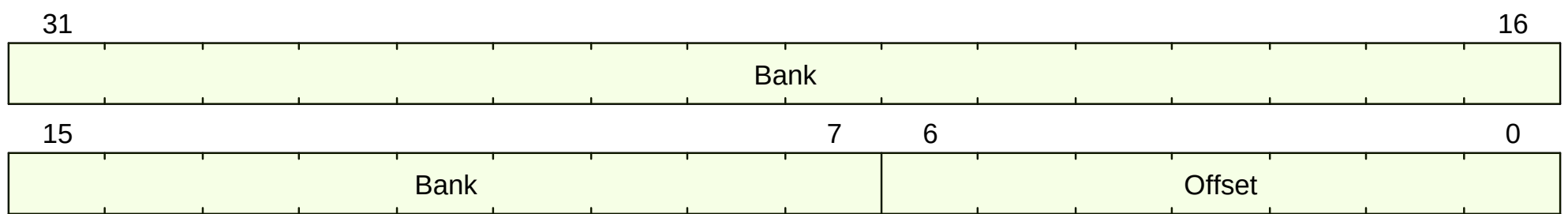


Figure 53. mvendorid format

C.53.3. Field Summary

Name	Location	Type	Reset Value
mvendorid.Bank	31:7	RO	UNDEFINED_LEGAL
mvendorid.Offset	6:0	RO	UNDEFINED_LEGAL

C.53.4. Fields

[mvendorid.Bank](#) Field

Location:
31:7

Description:
JEDEC manufacturer ID bank minus 1

Type:
RO

Reset value:
UNDEFINED_LEGAL

[mvendorid.Offset](#) Field

Location:
6:0

Description:
JEDEC manufacturer ID offset

Type:
RO

Reset value:
UNDEFINED_LEGAL

C.54. pmpaddr0

PMP Address 0

PMP entry address

C.54.1. Attributes

CSR Address	0x3b0
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.54.2. Format



Figure 54. pmpaddr0 format

C.54.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr0.ADDR	63:0	RW	0
		RO	

C.54.4. Fields

[pmpaddr0.ADDR](#) Field

Location:

63:0

Description:

Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 0 (or, if `pmp1cfg.A` == TOR, for PMP entry 1).

Type:

RW

RO

Reset value:

0

C.54.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 0) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.54.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp0cfg[4] == 1)) {
        return CSR[pmpaddr0].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp0cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr0].ADDR & ~mask;
    } else {
        return CSR[pmpaddr0].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp0cfg[4] == 1)) {
        return CSR[pmpaddr0].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp0cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr0].ADDR & ~mask;
    } else {
        return CSR[pmpaddr0].ADDR;
    }
}
}

```

C.55. pmpaddr1

PMP Address 1

PMP entry address

C.55.1. Attributes

CSR Address	0x3b1
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.55.2. Format



Figure 55. pmpaddr1 format

C.55.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr1.ADDR	63:0	RW	0
		RO	

C.55.4. Fields

[pmpaddr1.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 1 (or, if [pmp2cfg.A](#) == TOR, for PMP entry 2).

Type:

RW

RO

Reset value:
0

C.55.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 '<< (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 1) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.55.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp1cfg[4] == 1)) {
        return CSR[pmpaddr1].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp1cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr1].ADDR & ~mask;
    } else {
        return CSR[pmpaddr1].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp1cfg[4] == 1)) {
        return CSR[pmpaddr1].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp1cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr1].ADDR & ~mask;
    } else {
        return CSR[pmpaddr1].ADDR;
    }
}
}

```


C.56. pmpaddr10

PMP Address 10

PMP entry address

C.56.1. Attributes

CSR Address	0x3ba
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.56.2. Format



Figure 56. pmpaddr10 format

C.56.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr10.ADDR	63:0	RW	0
		RO	

C.56.4. Fields

[pmpaddr10.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 10 (or, if [pmp11cfg.A](#) == TOR, for PMP entry 11).

Type:

RW

RO

Reset value:
0

C.56.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 10) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.56.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp10cfg[4] == 1)) {
        return CSR[pmpaddr10].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp10cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr10].ADDR & ~mask;
    } else {
        return CSR[pmpaddr10].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp10cfg[4] == 1)) {
        return CSR[pmpaddr10].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp10cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr10].ADDR & ~mask;
    } else {
        return CSR[pmpaddr10].ADDR;
    }
}
}

```


C.57. pmpaddr11

PMP Address 11

PMP entry address

C.57.1. Attributes

CSR Address	0x3bb
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.57.2. Format



Figure 57. pmpaddr11 format

C.57.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr11.A	63:0	RW	0
pmpaddr11.DDR		RO	

C.57.4. Fields

[pmpaddr11.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 11 (or, if [pmp12cfg.A](#) == TOR, for PMP entry 12).

Type:

RW

RO

Reset value:
0

C.57.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 11) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.57.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp11cfg[4] == 1)) {
        return CSR[pmpaddr11].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp11cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr11].ADDR & ~mask;
    } else {
        return CSR[pmpaddr11].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp11cfg[4] == 1)) {
        return CSR[pmpaddr11].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp11cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr11].ADDR & ~mask;
    } else {
        return CSR[pmpaddr11].ADDR;
    }
}
}

```

C.58. pmpaddr12

PMP Address 12

PMP entry address

C.58.1. Attributes

CSR Address	0x3bc
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.58.2. Format



Figure 58. pmpaddr12 format

C.58.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr12.A	63:0	RW	0
DDR		RO	

C.58.4. Fields

[pmpaddr12.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 12 (or, if [pmp13cfg.A](#) == TOR, for PMP entry 13).

Type:

RW

RO

Reset value:
0

C.58.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 12) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.58.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg3].pmp12cfg[4] == 1)) {
        return CSR[pmpaddr12].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg3].pmp12cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr12].ADDR & ~mask;
    } else {
        return CSR[pmpaddr12].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp12cfg[4] == 1)) {
        return CSR[pmpaddr12].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp12cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr12].ADDR & ~mask;
    } else {
        return CSR[pmpaddr12].ADDR;
    }
}
}

```

C.59. pmpaddr13

PMP Address 13

PMP entry address

C.59.1. Attributes

CSR Address	0x3bd
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.59.2. Format



Figure 59. pmpaddr13 format

C.59.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr13.A	63:0	RW	0
DDR		RO	

C.59.4. Fields

[pmpaddr13.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 13 (or, if [pmp14cfg.A](#) == TOR, for PMP entry 14).

Type:

RW

RO

Reset value:
0

C.59.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 13) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.59.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg3].pmp13cfg[4] == 1)) {
        return CSR[pmpaddr13].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg3].pmp13cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr13].ADDR & ~mask;
    } else {
        return CSR[pmpaddr13].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp13cfg[4] == 1)) {
        return CSR[pmpaddr13].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp13cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr13].ADDR & ~mask;
    } else {
        return CSR[pmpaddr13].ADDR;
    }
}
}

```


C.60. pmpaddr14

PMP Address 14

PMP entry address

C.60.1. Attributes

CSR Address	0x3be
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.60.2. Format



Figure 60. pmpaddr14 format

C.60.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr14.A	63:0	RW	0
DDR		RO	

C.60.4. Fields

[pmpaddr14.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 14 (or, if [pmp15cfg.A](#) == TOR, for PMP entry 15).

Type:

RW

RO

Reset value:
0

C.60.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 14) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.60.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg3].pmp14cfg[4] == 1)) {
        return CSR[pmpaddr14].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg3].pmp14cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr14].ADDR & ~mask;
    } else {
        return CSR[pmpaddr14].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp14cfg[4] == 1)) {
        return CSR[pmpaddr14].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp14cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr14].ADDR & ~mask;
    } else {
        return CSR[pmpaddr14].ADDR;
    }
}
}

```


C.61. pmpaddr15

PMP Address 15

PMP entry address

C.61.1. Attributes

CSR Address	0x3bf
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.61.2. Format



Figure 61. pmpaddr15 format

C.61.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr15.A	63:0	RW	0
DDR		RO	

C.61.4. Fields

[pmpaddr15.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 15 (or, if [pmp16cfg.A](#) == TOR, for PMP entry 16).

Type:

RW

RO

Reset value:
0

C.61.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 15) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
return csr_value.ADDR;
}

```

C.61.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg3].pmp15cfg[4] == 1)) {
        return CSR[pmpaddr15].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg3].pmp15cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr15].ADDR & ~mask;
    } else {
        return CSR[pmpaddr15].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp15cfg[4] == 1)) {
        return CSR[pmpaddr15].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp15cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr15].ADDR & ~mask;
    } else {
        return CSR[pmpaddr15].ADDR;
    }
}
}

```

C.62. pmpaddr16

PMP Address 16

PMP entry address

C.62.1. Attributes

CSR Address	0x3c0
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.62.2. Format



Figure 62. pmpaddr16 format

C.62.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr16.ADDR	63:0	RW	0
		RO	

C.62.4. Fields

[pmpaddr16.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 16 (or, if [pmp17cfg.A](#) == TOR, for PMP entry 17).

Type:

RW

RO

Reset value:
0

C.62.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 16) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.62.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp16cfg[4] == 1)) {
        return CSR[pmpaddr16].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp16cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr16].ADDR & ~mask;
    } else {
        return CSR[pmpaddr16].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp16cfg[4] == 1)) {
        return CSR[pmpaddr16].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp16cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr16].ADDR & ~mask;
    } else {
        return CSR[pmpaddr16].ADDR;
    }
}
}

```

C.63. pmpaddr17

PMP Address 17

PMP entry address

C.63.1. Attributes

CSR Address	0x3c1
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.63.2. Format



Figure 63. pmpaddr17 format

C.63.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr17.A	63:0	RW	0
DDR		RO	

C.63.4. Fields

[pmpaddr17.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 17 (or, if [pmp18cfg.A](#) == TOR, for PMP entry 18).

Type:

RW

RO

Reset value:
0

C.63.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 17) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.63.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp17cfg[4] == 1)) {
        return CSR[pmpaddr17].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp17cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr17].ADDR & ~mask;
    } else {
        return CSR[pmpaddr17].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp17cfg[4] == 1)) {
        return CSR[pmpaddr17].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp17cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr17].ADDR & ~mask;
    } else {
        return CSR[pmpaddr17].ADDR;
    }
}
}

```


C.64. pmpaddr18

PMP Address 18

PMP entry address

C.64.1. Attributes

CSR Address	0x3c2
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.64.2. Format



Figure 64. pmpaddr18 format

C.64.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr18.A DDR	63:0	RW	0
		RO	

C.64.4. Fields

[pmpaddr18.ADDR](#) Field

Location:

63:0

Description:

Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 18 (or, if [pmp19cfg.A](#) == TOR, for PMP entry 19).

Type:

RW

RO

Reset value:

0

C.64.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 18) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.64.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp18cfg[4] == 1)) {
        return CSR[pmpaddr18].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp18cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr18].ADDR & ~mask;
    } else {
        return CSR[pmpaddr18].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp18cfg[4] == 1)) {
        return CSR[pmpaddr18].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp18cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr18].ADDR & ~mask;
    } else {
        return CSR[pmpaddr18].ADDR;
    }
}
}

```


C.65. pmpaddr19

PMP Address 19

PMP entry address

C.65.1. Attributes

CSR Address	0x3c3
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.65.2. Format



Figure 65. pmpaddr19 format

C.65.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr19.A DDR	63:0	RW	0
		RO	

C.65.4. Fields

[pmpaddr19.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 19 (or, if [pmp20cfg.A](#) == TOR, for PMP entry 20).

Type:

RW

RO

Reset value:
0

C.65.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 19) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.65.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp19cfg[4] == 1)) {
        return CSR[pmpaddr19].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp19cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr19].ADDR & ~mask;
    } else {
        return CSR[pmpaddr19].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp19cfg[4] == 1)) {
        return CSR[pmpaddr19].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp19cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr19].ADDR & ~mask;
    } else {
        return CSR[pmpaddr19].ADDR;
    }
}
}

```

C.66. pmpaddr2

PMP Address 2

PMP entry address

C.66.1. Attributes

CSR Address	0x3b2
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.66.2. Format



Figure 66. pmpaddr2 format

C.66.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr2.ADDR	63:0	RW	0
		RO	

C.66.4. Fields

[pmpaddr2.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 2 (or, if [pmp3cfg.A](#) == TOR, for PMP entry 3).

Type:

RW

RO

Reset value:
0

C.66.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 '<< (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 2) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.66.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp2cfg[4] == 1)) {
        return CSR[pmpaddr2].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp2cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr2].ADDR & ~mask;
    } else {
        return CSR[pmpaddr2].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp2cfg[4] == 1)) {
        return CSR[pmpaddr2].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp2cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr2].ADDR & ~mask;
    } else {
        return CSR[pmpaddr2].ADDR;
    }
}
}

```

C.67. pmpaddr20

PMP Address 20

PMP entry address

C.67.1. Attributes

CSR Address	0x3c4
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.67.2. Format



Figure 67. pmpaddr20 format

C.67.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr20.A	63:0	RW	0
pmpaddr20.DDR		RO	

C.67.4. Fields

[pmpaddr20.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 20 (or, if [pmp21cfg.A](#) == TOR, for PMP entry 21).

Type:

RW

RO

Reset value:
0

C.67.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 20) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.67.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg5].pmp20cfg[4] == 1)) {
        return CSR[pmpaddr20].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg5].pmp20cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr20].ADDR & ~mask;
    } else {
        return CSR[pmpaddr20].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp20cfg[4] == 1)) {
        return CSR[pmpaddr20].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp20cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr20].ADDR & ~mask;
    } else {
        return CSR[pmpaddr20].ADDR;
    }
}
}

```


C.68. pmpaddr21

PMP Address 21

PMP entry address

C.68.1. Attributes

CSR Address	0x3c5
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.68.2. Format

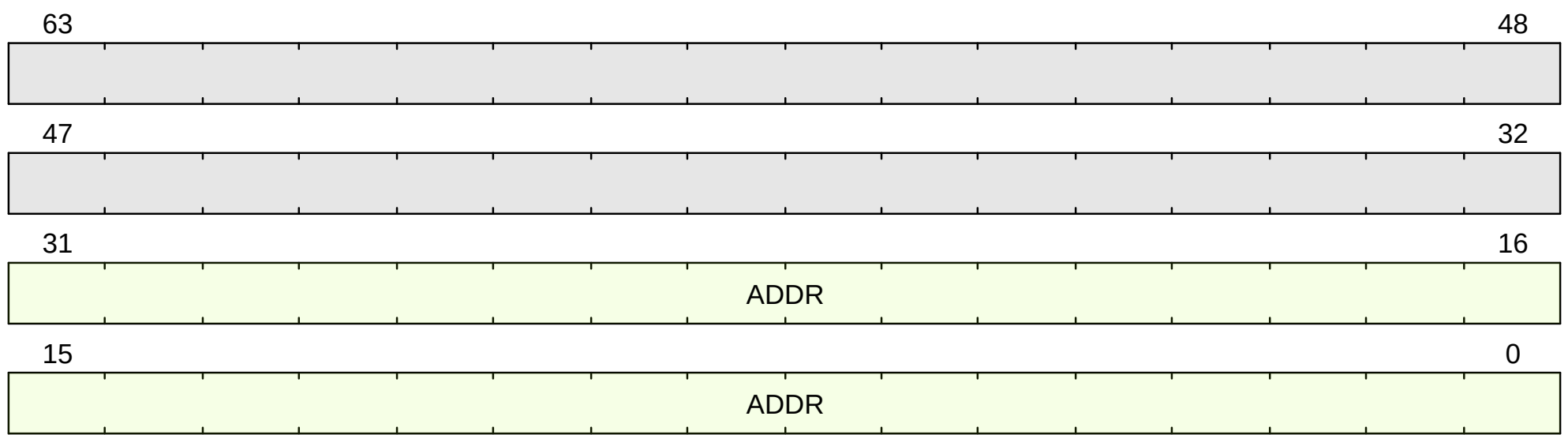


Figure 68. pmpaddr21 format

C.68.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr21.A	63:0	RW	0
DDR		RO	

C.68.4. Fields

[pmpaddr21.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 21 (or, if [pmp22cfg.A](#) == TOR, for PMP entry 22).

Type:

RW

RO

Reset value:
0

C.68.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 21) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.68.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg5].pmp21cfg[4] == 1)) {
        return CSR[pmpaddr21].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg5].pmp21cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr21].ADDR & ~mask;
    } else {
        return CSR[pmpaddr21].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp21cfg[4] == 1)) {
        return CSR[pmpaddr21].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp21cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr21].ADDR & ~mask;
    } else {
        return CSR[pmpaddr21].ADDR;
    }
}
}

```


C.69. pmpaddr22

PMP Address 22

PMP entry address

C.69.1. Attributes

CSR Address	0x3c6
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.69.2. Format



Figure 69. pmpaddr22 format

C.69.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr22.A	63:0	RW	0
DDR		RO	

C.69.4. Fields

[pmpaddr22.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 22 (or, if [pmp23cfg.A](#) == TOR, for PMP entry 23).

Type:

RW

RO

Reset value:
0

C.69.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 22) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.69.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg5].pmp22cfg[4] == 1)) {
        return CSR[pmpaddr22].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg5].pmp22cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr22].ADDR & ~mask;
    } else {
        return CSR[pmpaddr22].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp22cfg[4] == 1)) {
        return CSR[pmpaddr22].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp22cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr22].ADDR & ~mask;
    } else {
        return CSR[pmpaddr22].ADDR;
    }
}
}

```

C.70. pmpaddr23

PMP Address 23

PMP entry address

C.70.1. Attributes

CSR Address	0x3c7
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.70.2. Format



Figure 70. pmpaddr23 format

C.70.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr23.A	63:0	RW	0
pmpaddr23.DDR		RO	

C.70.4. Fields

[pmpaddr23.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 23 (or, if [pmp24cfg.A](#) == TOR, for PMP entry 24).

Type:

RW

RO

Reset value:
0

C.70.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 23) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.70.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg5].pmp23cfg[4] == 1)) {
        return CSR[pmpaddr23].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg5].pmp23cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr23].ADDR & ~mask;
    } else {
        return CSR[pmpaddr23].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg4].pmp23cfg[4] == 1)) {
        return CSR[pmpaddr23].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg4].pmp23cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr23].ADDR & ~mask;
    } else {
        return CSR[pmpaddr23].ADDR;
    }
}
}

```

C.71. pmpaddr24

PMP Address 24

PMP entry address

C.71.1. Attributes

CSR Address	0x3c8
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.71.2. Format



Figure 71. pmpaddr24 format

C.71.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr24.A	63:0	RW	0
pmpaddr24.DDR		RO	

C.71.4. Fields

[pmpaddr24.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 24 (or, if [pmp25cfg.A](#) == TOR, for PMP entry 25).

Type:

RW

RO

Reset value:
0

C.71.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 24) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.71.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp24cfg[4] == 1)) {
        return CSR[pmpaddr24].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp24cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr24].ADDR & ~mask;
    } else {
        return CSR[pmpaddr24].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp24cfg[4] == 1)) {
        return CSR[pmpaddr24].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp24cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr24].ADDR & ~mask;
    } else {
        return CSR[pmpaddr24].ADDR;
    }
}
}

```


C.72. pmpaddr25

PMP Address 25

PMP entry address

C.72.1. Attributes

CSR Address	0x3c9
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.72.2. Format



Figure 72. pmpaddr25 format

C.72.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr25.ADDR	63:0	RW	0
		RO	

C.72.4. Fields

[pmpaddr25.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 25 (or, if [pmp26cfg.A](#) == TOR, for PMP entry 26).

Type:

RW

RO

Reset value:
0

C.72.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 25) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.72.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp25cfg[4] == 1)) {
        return CSR[pmpaddr25].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp25cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr25].ADDR & ~mask;
    } else {
        return CSR[pmpaddr25].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp25cfg[4] == 1)) {
        return CSR[pmpaddr25].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp25cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr25].ADDR & ~mask;
    } else {
        return CSR[pmpaddr25].ADDR;
    }
}
}

```


C.73. pmpaddr26

PMP Address 26

PMP entry address

C.73.1. Attributes

CSR Address	0x3ca
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.73.2. Format



Figure 73. pmpaddr26 format

C.73.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr26.A	63:0	RW	0
DDR		RO	

C.73.4. Fields

[pmpaddr26.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 26 (or, if [pmp27cfg.A](#) == TOR, for PMP entry 27).

Type:

RW

RO

Reset value:
0

C.73.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 26) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.73.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp26cfg[4] == 1)) {
        return CSR[pmpaddr26].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp26cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr26].ADDR & ~mask;
    } else {
        return CSR[pmpaddr26].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp26cfg[4] == 1)) {
        return CSR[pmpaddr26].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp26cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr26].ADDR & ~mask;
    } else {
        return CSR[pmpaddr26].ADDR;
    }
}
}

```

C.74. pmpaddr27

PMP Address 27

PMP entry address

C.74.1. Attributes

CSR Address	0x3cb
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.74.2. Format



Figure 74. pmpaddr27 format

C.74.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr27.A	63:0	RW	0
pmpaddr27.DDR		RO	

C.74.4. Fields

[pmpaddr27.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 27 (or, if [pmp28cfg.A](#) == TOR, for PMP entry 28).

Type:

RW

RO

Reset value:
0

C.74.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 27) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.74.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp27cfg[4] == 1)) {
        return CSR[pmpaddr27].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp27cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr27].ADDR & ~mask;
    } else {
        return CSR[pmpaddr27].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp27cfg[4] == 1)) {
        return CSR[pmpaddr27].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp27cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr27].ADDR & ~mask;
    } else {
        return CSR[pmpaddr27].ADDR;
    }
}
}

```

C.75. pmpaddr28

PMP Address 28

PMP entry address

C.75.1. Attributes

CSR Address	0x3cc
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.75.2. Format



Figure 75. pmpaddr28 format

C.75.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr28.ADDR	63:0	RW	0
		RO	

C.75.4. Fields

[pmpaddr28.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 28 (or, if [pmp29cfg.A](#) == TOR, for PMP entry 29).

Type:

RW

RO

Reset value:
0

C.75.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 28) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.75.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg7].pmp28cfg[4] == 1)) {
        return CSR[pmpaddr28].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg7].pmp28cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr28].ADDR & ~mask;
    } else {
        return CSR[pmpaddr28].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp28cfg[4] == 1)) {
        return CSR[pmpaddr28].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp28cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr28].ADDR & ~mask;
    } else {
        return CSR[pmpaddr28].ADDR;
    }
}
}

```


C.76. pmpaddr29

PMP Address 29

PMP entry address

C.76.1. Attributes

CSR Address	0x3cd
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.76.2. Format



Figure 76. pmpaddr29 format

C.76.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr29.A	63:0	RW	0
DDR		RO	

C.76.4. Fields

[pmpaddr29.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 29
(or, if [pmp30cfg.A](#) == TOR, for PMP entry 30).

Type:

RW

RO

Reset value:
0

C.76.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 29) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.76.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg7].pmp29cfg[4] == 1)) {
        return CSR[pmpaddr29].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg7].pmp29cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr29].ADDR & ~mask;
    } else {
        return CSR[pmpaddr29].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp29cfg[4] == 1)) {
        return CSR[pmpaddr29].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp29cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr29].ADDR & ~mask;
    } else {
        return CSR[pmpaddr29].ADDR;
    }
}
}

```


C.77. pmpaddr3

PMP Address 3

PMP entry address

C.77.1. Attributes

CSR Address	0x3b3
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.77.2. Format



Figure 77. pmpaddr3 format

C.77.3. Field Summary

Name	Location	Type	Reset Value
pmpa ddr3. ADDR	63:0	RW RO	0

C.77.4. Fields

[pmpaddr3.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 3
(or, if [pmp4cfg.A](#) == TOR, for PMP entry 4).

Type:

RW

RO

Reset value:
0

C.77.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 '<< (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 3) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.77.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp3cfg[4] == 1)) {
        return CSR[pmpaddr3].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp3cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr3].ADDR & ~mask;
    } else {
        return CSR[pmpaddr3].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp3cfg[4] == 1)) {
        return CSR[pmpaddr3].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp3cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr3].ADDR & ~mask;
    } else {
        return CSR[pmpaddr3].ADDR;
    }
}
}

```

C.78. pmpaddr30

PMP Address 30

PMP entry address

C.78.1. Attributes

CSR Address	0x3ce
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.78.2. Format



Figure 78. pmpaddr30 format

C.78.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr30.A	63:0	RW	0
DDR		RO	

C.78.4. Fields

[pmpaddr30.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 30 (or, if [pmp31cfg.A](#) == TOR, for PMP entry 31).

Type:

RW

RO

Reset value:
0

C.78.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 `<< (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 30) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.78.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg7].pmp30cfg[4] == 1)) {
        return CSR[pmpaddr30].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg7].pmp30cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr30].ADDR & ~mask;
    } else {
        return CSR[pmpaddr30].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp30cfg[4] == 1)) {
        return CSR[pmpaddr30].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp30cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr30].ADDR & ~mask;
    } else {
        return CSR[pmpaddr30].ADDR;
    }
}
}

```

C.79. pmpaddr31

PMP Address 31

PMP entry address

C.79.1. Attributes

CSR Address	0x3cf
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.79.2. Format

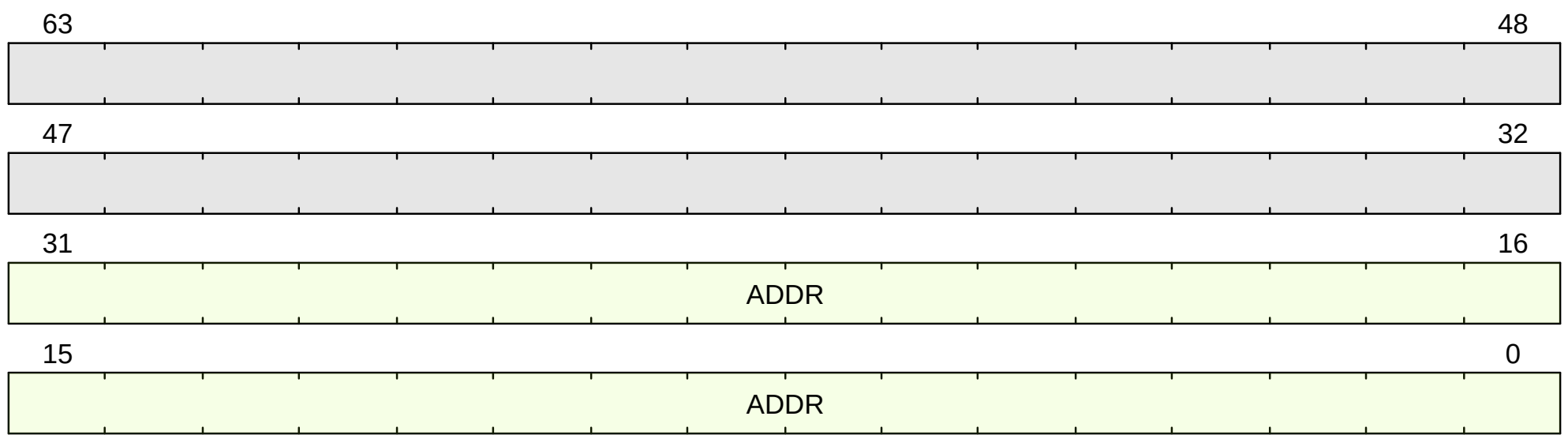


Figure 79. pmpaddr31 format

C.79.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr31.A	63:0	RW	0
DDR		RO	

C.79.4. Fields

[pmpaddr31.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 31 (or, if [pmp32cfg.A](#) == TOR, for PMP entry 32).

Type:

RW

RO

Reset value:
0

C.79.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 31) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.79.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg7].pmp31cfg[4] == 1)) {
        return CSR[pmpaddr31].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg7].pmp31cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr31].ADDR & ~mask;
    } else {
        return CSR[pmpaddr31].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg6].pmp31cfg[4] == 1)) {
        return CSR[pmpaddr31].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg6].pmp31cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr31].ADDR & ~mask;
    } else {
        return CSR[pmpaddr31].ADDR;
    }
}
}

```


C.80. pmpaddr32

PMP Address 32

PMP entry address

C.80.1. Attributes

CSR Address	0x3d0
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.80.2. Format



Figure 80. pmpaddr32 format

C.80.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr32.A	63:0	RW	0
DDR		RO	

C.80.4. Fields

[pmpaddr32.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 32 (or, if [pmp32cfg.A](#) == TOR, for PMP entry 33).

Type:

RW

RO

Reset value:
0

C.80.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 32) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.80.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp32cfg[4] == 1)) {
        return CSR[pmpaddr32].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp32cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr32].ADDR & ~mask;
    } else {
        return CSR[pmpaddr32].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp32cfg[4] == 1)) {
        return CSR[pmpaddr32].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp32cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr32].ADDR & ~mask;
    } else {
        return CSR[pmpaddr32].ADDR;
    }
}
}

```


C.81. pmpaddr33

PMP Address 33

PMP entry address

C.81.1. Attributes

CSR Address	0x3d1
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.81.2. Format



Figure 81. pmpaddr33 format

C.81.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr33.A	63:0	RW	0
DDR		RO	

C.81.4. Fields

[pmpaddr33.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 33 (or, if [pmp34cfg.A](#) == TOR, for PMP entry 34).

Type:

RW

RO

Reset value:
0

C.81.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 33) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.81.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp33cfg[4] == 1)) {
        return CSR[pmpaddr33].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp33cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr33].ADDR & ~mask;
    } else {
        return CSR[pmpaddr33].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp33cfg[4] == 1)) {
        return CSR[pmpaddr33].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp33cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr33].ADDR & ~mask;
    } else {
        return CSR[pmpaddr33].ADDR;
    }
}
}

```

C.82. pmpaddr34

PMP Address 34

PMP entry address

C.82.1. Attributes

CSR Address	0x3d2
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.82.2. Format



Figure 82. pmpaddr34 format

C.82.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr34.ADDR	63:0	RW	0
		RO	

C.82.4. Fields

[pmpaddr34.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 34 (or, if [pmp35cfg.A](#) == TOR, for PMP entry 35).

Type:

RW

RO

Reset value:
0

C.82.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 34) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.82.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp34cfg[4] == 1)) {
        return CSR[pmpaddr34].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp34cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr34].ADDR & ~mask;
    } else {
        return CSR[pmpaddr34].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp34cfg[4] == 1)) {
        return CSR[pmpaddr34].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp34cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr34].ADDR & ~mask;
    } else {
        return CSR[pmpaddr34].ADDR;
    }
}
}

```

C.83. pmpaddr35

PMP Address 35

PMP entry address

C.83.1. Attributes

CSR Address	0x3d3
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.83.2. Format

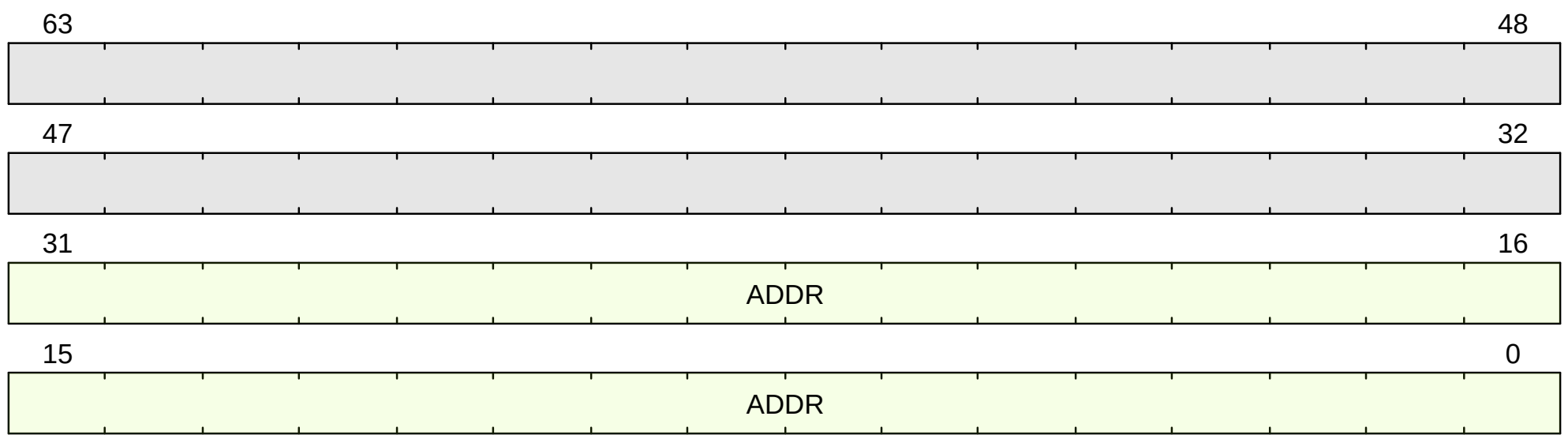


Figure 83. pmpaddr35 format

C.83.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr35.ADDR	63:0	RW	0
		RO	

C.83.4. Fields

[pmpaddr35.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 35 (or, if [pmp36cfg.A](#) == TOR, for PMP entry 36).

Type:

RW

RO

Reset value:
0

C.83.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 35) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.83.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp35cfg[4] == 1)) {
        return CSR[pmpaddr35].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp35cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr35].ADDR & ~mask;
    } else {
        return CSR[pmpaddr35].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp35cfg[4] == 1)) {
        return CSR[pmpaddr35].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp35cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr35].ADDR & ~mask;
    } else {
        return CSR[pmpaddr35].ADDR;
    }
}
}

```


C.84. pmpaddr36

PMP Address 36

PMP entry address

C.84.1. Attributes

CSR Address	0x3d4
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.84.2. Format



Figure 84. pmpaddr36 format

C.84.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr36.ADDR	63:0	RW	0
		RO	

C.84.4. Fields

[pmpaddr36.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 36 (or, if [pmp37cfg.A](#) == TOR, for PMP entry 37).

Type:

RW

RO

Reset value:
0

C.84.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 36) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.84.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg9].pmp36cfg[4] == 1)) {
        return CSR[pmpaddr36].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg9].pmp36cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr36].ADDR & ~mask;
    } else {
        return CSR[pmpaddr36].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp36cfg[4] == 1)) {
        return CSR[pmpaddr36].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp36cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr36].ADDR & ~mask;
    } else {
        return CSR[pmpaddr36].ADDR;
    }
}
}

```


C.85. pmpaddr37

PMP Address 37

PMP entry address

C.85.1. Attributes

CSR Address	0x3d5
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.85.2. Format



Figure 85. pmpaddr37 format

C.85.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr37.A	63:0	RW	0
DDR		RO	

C.85.4. Fields

[pmpaddr37.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 37 (or, if [pmp38cfg.A](#) == TOR, for PMP entry 38).

Type:

RW

RO

Reset value:
0

C.85.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 37) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.85.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg9].pmp37cfg[4] == 1)) {
        return CSR[pmpaddr37].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg9].pmp37cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr37].ADDR & ~mask;
    } else {
        return CSR[pmpaddr37].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp37cfg[4] == 1)) {
        return CSR[pmpaddr37].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp37cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr37].ADDR & ~mask;
    } else {
        return CSR[pmpaddr37].ADDR;
    }
}
}

```

C.86. pmpaddr38

PMP Address 38

PMP entry address

C.86.1. Attributes

CSR Address	0x3d6
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.86.2. Format



Figure 86. pmpaddr38 format

C.86.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr38.ADDR	63:0	RW	0
		RO	

C.86.4. Fields

[pmpaddr38.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 38 (or, if [pmp39cfg.A](#) == TOR, for PMP entry 39).

Type:

RW

RO

Reset value:
0

C.86.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 38) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.86.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg9].pmp38cfg[4] == 1)) {
        return CSR[pmpaddr38].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg9].pmp38cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr38].ADDR & ~mask;
    } else {
        return CSR[pmpaddr38].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp38cfg[4] == 1)) {
        return CSR[pmpaddr38].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp38cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr38].ADDR & ~mask;
    } else {
        return CSR[pmpaddr38].ADDR;
    }
}
}

```

C.87. pmpaddr39

PMP Address 39

PMP entry address

C.87.1. Attributes

CSR Address	0x3d7
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.87.2. Format



Figure 87. pmpaddr39 format

C.87.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr39.A	63:0	RW	0
DDR		RO	

C.87.4. Fields

[pmpaddr39.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 39 (or, if [pmp40cfg.A](#) == TOR, for PMP entry 40).

Type:

RW

RO

Reset value:
0

C.87.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 39) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
return csr_value.ADDR;
}

```

C.87.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg9].pmp39cfg[4] == 1)) {
        return CSR[pmpaddr39].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg9].pmp39cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr39].ADDR & ~mask;
    } else {
        return CSR[pmpaddr39].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg8].pmp39cfg[4] == 1)) {
        return CSR[pmpaddr39].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg8].pmp39cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr39].ADDR & ~mask;
    } else {
        return CSR[pmpaddr39].ADDR;
    }
}
}

```


C.88. pmpaddr4

PMP Address 4

PMP entry address

C.88.1. Attributes

CSR Address	0x3b4
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.88.2. Format



Figure 88. pmpaddr4 format

C.88.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr4.ADDR	63:0	RW	0
		RO	

C.88.4. Fields

[pmpaddr4.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 4 (or, if [pmp5cfg.A](#) == TOR, for PMP entry 5).

Type:

RW

RO

Reset value:
0

C.88.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 4) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.88.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg1].pmp4cfg[4] == 1)) {
        return CSR[pmpaddr4].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg1].pmp4cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr4].ADDR & ~mask;
    } else {
        return CSR[pmpaddr4].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp4cfg[4] == 1)) {
        return CSR[pmpaddr4].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp4cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr4].ADDR & ~mask;
    } else {
        return CSR[pmpaddr4].ADDR;
    }
}
}

```


C.89. pmpaddr40

PMP Address 40

PMP entry address

C.89.1. Attributes

CSR Address	0x3d8
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.89.2. Format



Figure 89. pmpaddr40 format

C.89.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr40.A	63:0	RW	0
DDR		RO	

C.89.4. Fields

[pmpaddr40.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 40 (or, if [pmp41cfg.A](#) == TOR, for PMP entry 41).

Type:

RW

RO

Reset value:
0

C.89.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 40) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.89.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp40cfg[4] == 1)) {
        return CSR[pmpaddr40].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp40cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr40].ADDR & ~mask;
    } else {
        return CSR[pmpaddr40].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp40cfg[4] == 1)) {
        return CSR[pmpaddr40].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp40cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr40].ADDR & ~mask;
    } else {
        return CSR[pmpaddr40].ADDR;
    }
}
}

```

C.90. pmpaddr41

PMP Address 41

PMP entry address

C.90.1. Attributes

CSR Address	0x3d9
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.90.2. Format



Figure 90. pmpaddr41 format

C.90.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr41.A	63:0	RW	0
DDR		RO	

C.90.4. Fields

[pmpaddr41.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 41 (or, if [pmp42cfg.A](#) == TOR, for PMP entry 42).

Type:

RW

RO

Reset value:
0

C.90.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 41) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.90.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp41cfg[4] == 1)) {
        return CSR[pmpaddr41].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp41cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr41].ADDR & ~mask;
    } else {
        return CSR[pmpaddr41].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp41cfg[4] == 1)) {
        return CSR[pmpaddr41].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp41cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr41].ADDR & ~mask;
    } else {
        return CSR[pmpaddr41].ADDR;
    }
}
}

```

C.91. pmpaddr42

PMP Address 42

PMP entry address

C.91.1. Attributes

CSR Address	0x3da
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.91.2. Format



Figure 91. pmpaddr42 format

C.91.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr42.A	63:0	RW	0
DDR		RO	

C.91.4. Fields

[pmpaddr42.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 42 (or, if [pmp43cfg.A](#) == TOR, for PMP entry 43).

Type:

RW

RO

Reset value:
0

C.91.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 42) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.91.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp42cfg[4] == 1)) {
        return CSR[pmpaddr42].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp42cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr42].ADDR & ~mask;
    } else {
        return CSR[pmpaddr42].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp42cfg[4] == 1)) {
        return CSR[pmpaddr42].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp42cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr42].ADDR & ~mask;
    } else {
        return CSR[pmpaddr42].ADDR;
    }
}
}

```


C.92. pmpaddr43

PMP Address 43

PMP entry address

C.92.1. Attributes

CSR Address	0x3db
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.92.2. Format



Figure 92. pmpaddr43 format

C.92.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr43.A	63:0	RW	0
DDR		RO	

C.92.4. Fields

[pmpaddr43.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 43 (or, if [pmp44cfg.A](#) == TOR, for PMP entry 44).

Type:

RW

RO

Reset value:
0

C.92.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 43) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.92.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp43cfg[4] == 1)) {
        return CSR[pmpaddr43].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp43cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr43].ADDR & ~mask;
    } else {
        return CSR[pmpaddr43].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp43cfg[4] == 1)) {
        return CSR[pmpaddr43].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp43cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr43].ADDR & ~mask;
    } else {
        return CSR[pmpaddr43].ADDR;
    }
}
}

```


C.93. pmpaddr44

PMP Address 44

PMP entry address

C.93.1. Attributes

CSR Address	0x3dc
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.93.2. Format



Figure 93. pmpaddr44 format

C.93.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr44.A	63:0	RW	0
DDR		RO	

C.93.4. Fields

[pmpaddr44.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 44 (or, if [pmp45cfg.A](#) == TOR, for PMP entry 45).

Type:

RW

RO

Reset value:
0

C.93.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 44) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.93.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg11].pmp44cfg[4] == 1)) {
        return CSR[pmpaddr44].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg11].pmp44cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr44].ADDR & ~mask;
    } else {
        return CSR[pmpaddr44].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp44cfg[4] == 1)) {
        return CSR[pmpaddr44].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp44cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr44].ADDR & ~mask;
    } else {
        return CSR[pmpaddr44].ADDR;
    }
}
}

```

C.94. pmpaddr45

PMP Address 45

PMP entry address

C.94.1. Attributes

CSR Address	0x3dd
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.94.2. Format



Figure 94. pmpaddr45 format

C.94.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr45.ADDR	63:0	RW	0
		RO	

C.94.4. Fields

[pmpaddr45.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 45 (or, if [pmp46cfg.A](#) == TOR, for PMP entry 46).

Type:

RW

RO

Reset value:
0

C.94.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 45) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.94.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg11].pmp45cfg[4] == 1)) {
        return CSR[pmpaddr45].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg11].pmp45cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr45].ADDR & ~mask;
    } else {
        return CSR[pmpaddr45].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp45cfg[4] == 1)) {
        return CSR[pmpaddr45].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp45cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr45].ADDR & ~mask;
    } else {
        return CSR[pmpaddr45].ADDR;
    }
}
}

```

C.95. pmpaddr46

PMP Address 46

PMP entry address

C.95.1. Attributes

CSR Address	0x3de
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.95.2. Format



Figure 95. pmpaddr46 format

C.95.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr46.A	63:0	RW	0
DDR		RO	

C.95.4. Fields

[pmpaddr46.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 46 (or, if [pmp47cfg.A](#) == TOR, for PMP entry 47).

Type:

RW

RO

Reset value:
0

C.95.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 46) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.95.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg11].pmp46cfg[4] == 1)) {
        return CSR[pmpaddr46].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg11].pmp46cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr46].ADDR & ~mask;
    } else {
        return CSR[pmpaddr46].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp46cfg[4] == 1)) {
        return CSR[pmpaddr46].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp46cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr46].ADDR & ~mask;
    } else {
        return CSR[pmpaddr46].ADDR;
    }
}
}

```


C.96. pmpaddr47

PMP Address 47

PMP entry address

C.96.1. Attributes

CSR Address	0x3df
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.96.2. Format

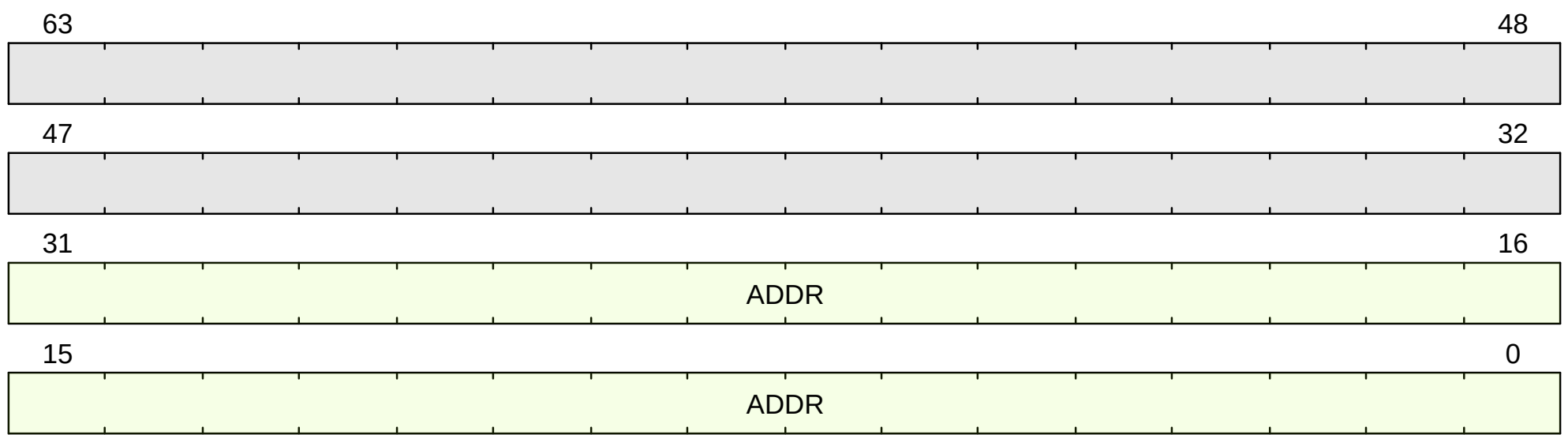


Figure 96. pmpaddr47 format

C.96.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr47.A	63:0	RW	0
DDR		RO	

C.96.4. Fields

[pmpaddr47.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 47 (or, if [pmp48cfg.A](#) == TOR, for PMP entry 48).

Type:

RW

RO

Reset value:
0

C.96.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 47) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.96.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg11].pmp47cfg[4] == 1)) {
        return CSR[pmpaddr47].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg11].pmp47cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr47].ADDR & ~mask;
    } else {
        return CSR[pmpaddr47].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg10].pmp47cfg[4] == 1)) {
        return CSR[pmpaddr47].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg10].pmp47cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr47].ADDR & ~mask;
    } else {
        return CSR[pmpaddr47].ADDR;
    }
}
}

```


C.97. pmpaddr48

PMP Address 48

PMP entry address

C.97.1. Attributes

CSR Address	0x3e0
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.97.2. Format



Figure 97. pmpaddr48 format

C.97.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr48.A	63:0	RW	0
DDR		RO	

C.97.4. Fields

[pmpaddr48.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 48 (or, if [pmp49cfg.A](#) == TOR, for PMP entry 49).

Type:

RW

RO

Reset value:
0

C.97.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 48) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.97.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp48cfg[4] == 1)) {
        return CSR[pmpaddr48].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp48cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr48].ADDR & ~mask;
    } else {
        return CSR[pmpaddr48].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp48cfg[4] == 1)) {
        return CSR[pmpaddr48].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp48cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr48].ADDR & ~mask;
    } else {
        return CSR[pmpaddr48].ADDR;
    }
}
}

```

C.98. pmpaddr49

PMP Address 49

PMP entry address

C.98.1. Attributes

CSR Address	0x3e1
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.98.2. Format



Figure 98. pmpaddr49 format

C.98.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr49.A	63:0	RW	0
DDR		RO	

C.98.4. Fields

[pmpaddr49.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 49 (or, if [pmp50cfg.A](#) == TOR, for PMP entry 50).

Type:

RW

RO

Reset value:
0

C.98.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 49) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.98.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp49cfg[4] == 1)) {
        return CSR[pmpaddr49].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp49cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr49].ADDR & ~mask;
    } else {
        return CSR[pmpaddr49].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp49cfg[4] == 1)) {
        return CSR[pmpaddr49].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp49cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr49].ADDR & ~mask;
    } else {
        return CSR[pmpaddr49].ADDR;
    }
}
}

```

C.99. pmpaddr5

PMP Address 5

PMP entry address

C.99.1. Attributes

CSR Address	0x3b5
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.99.2. Format

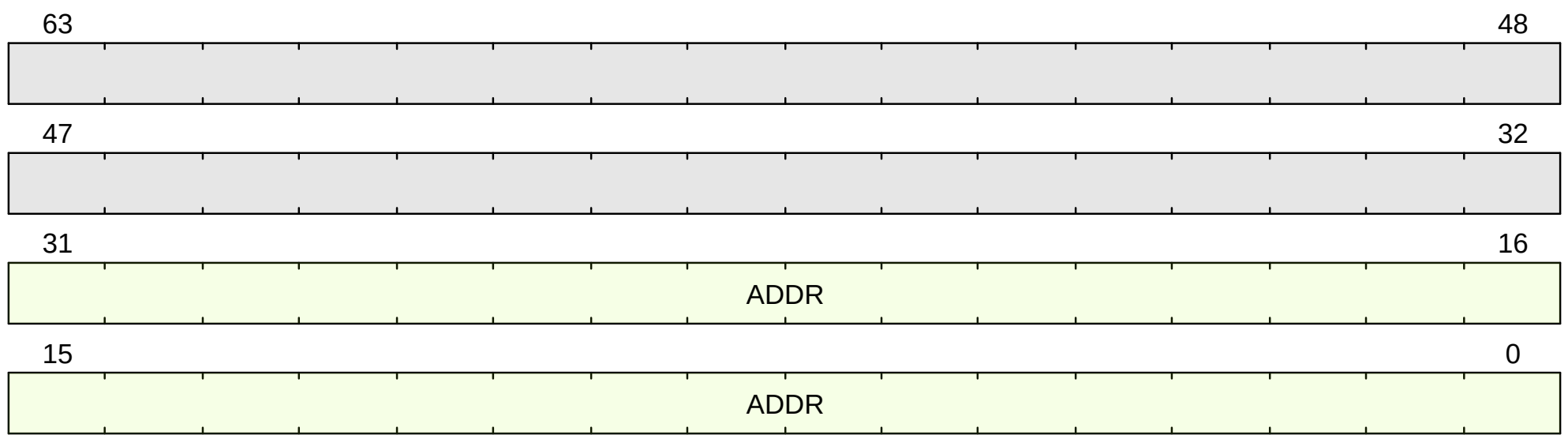


Figure 99. pmpaddr5 format

C.99.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr5.ADDR	63:0	RW	0
		RO	

C.99.4. Fields

[pmpaddr5.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 5 (or, if [pmp6cfg.A](#) == TOR, for PMP entry 6).

Type:

RW

RO

Reset value:
0

C.99.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 5) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.99.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg1].pmp5cfg[4] == 1)) {
        return CSR[pmpaddr5].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg1].pmp5cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr5].ADDR & ~mask;
    } else {
        return CSR[pmpaddr5].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp5cfg[4] == 1)) {
        return CSR[pmpaddr5].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp5cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr5].ADDR & ~mask;
    } else {
        return CSR[pmpaddr5].ADDR;
    }
}
}

```


C.100. pmpaddr50

PMP Address 50

PMP entry address

C.100.1. Attributes

CSR Address	0x3e2
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.100.2. Format

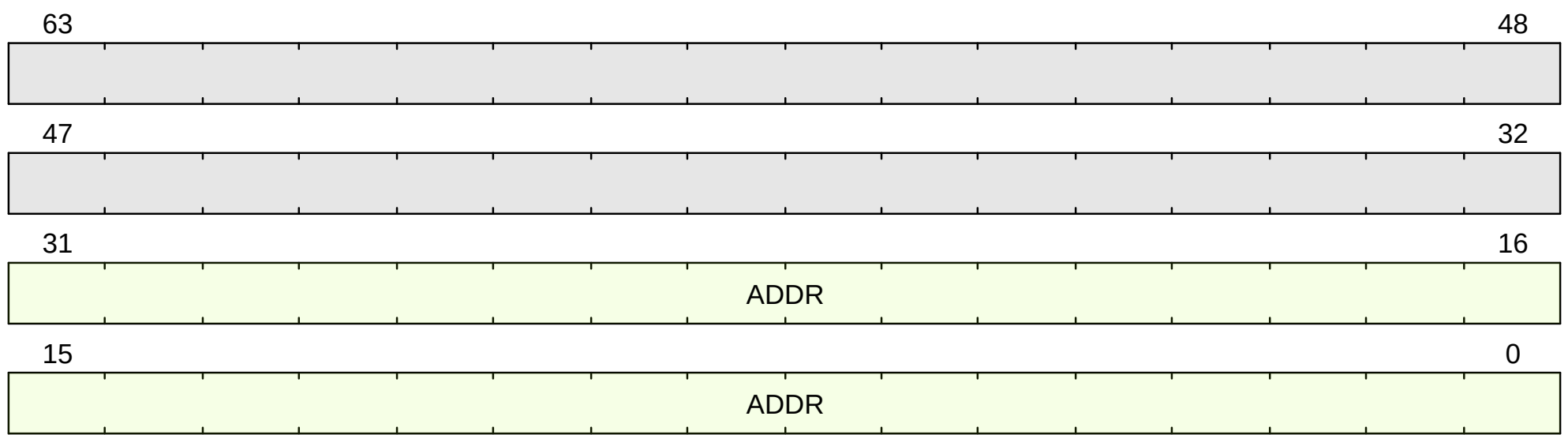


Figure 100. pmpaddr50 format

C.100.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr50.A	63:0	RW	0
DDR		RO	

C.100.4. Fields

[pmpaddr50.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 50 (or, if [pmp51cfg.A](#) == TOR, for PMP entry 51).

Type:

RW

RO

Reset value:
0

C.100.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 50) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.100.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp50cfg[4] == 1)) {
        return CSR[pmpaddr50].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp50cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr50].ADDR & ~mask;
    } else {
        return CSR[pmpaddr50].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp50cfg[4] == 1)) {
        return CSR[pmpaddr50].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp50cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr50].ADDR & ~mask;
    } else {
        return CSR[pmpaddr50].ADDR;
    }
}
}

```


C.101. pmpaddr51

PMP Address 51

PMP entry address

C.101.1. Attributes

CSR Address	0x3e3
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.101.2. Format

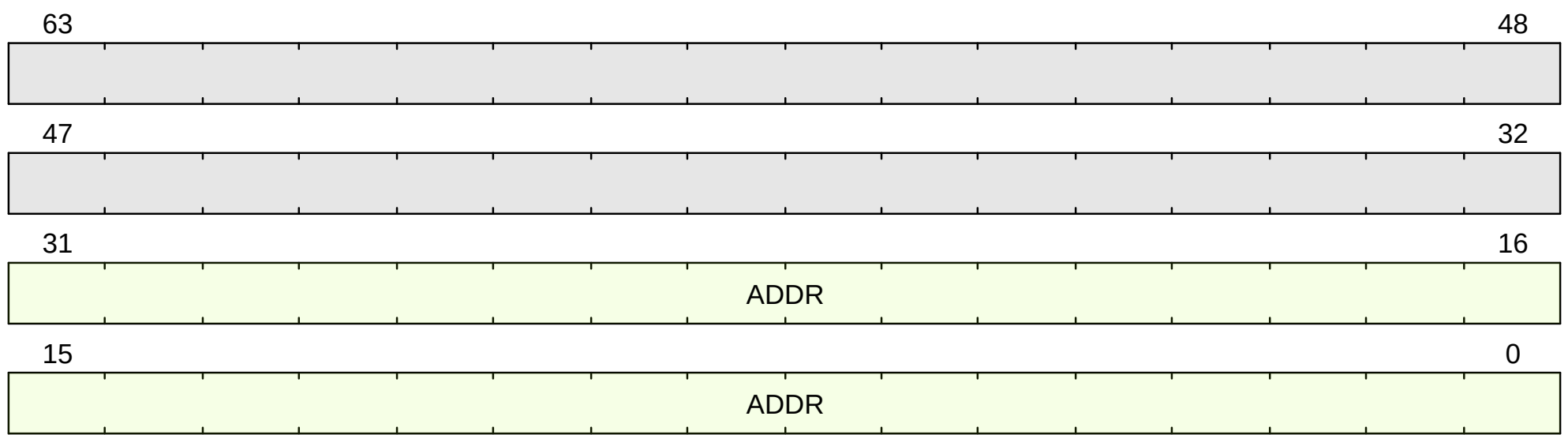


Figure 101. pmpaddr51 format

C.101.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr51.ADDR	63:0	RW	0
		RO	

C.101.4. Fields

[pmpaddr51.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 51 (or, if [pmp52cfg.A](#) == TOR, for PMP entry 52).

Type:

RW

RO

Reset value:
0

C.101.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 51) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.101.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp51cfg[4] == 1)) {
        return CSR[pmpaddr51].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp51cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr51].ADDR & ~mask;
    } else {
        return CSR[pmpaddr51].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp51cfg[4] == 1)) {
        return CSR[pmpaddr51].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp51cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr51].ADDR & ~mask;
    } else {
        return CSR[pmpaddr51].ADDR;
    }
}
}

```

C.102. pmpaddr52

PMP Address 52

PMP entry address

C.102.1. Attributes

CSR Address	0x3e4
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.102.2. Format



Figure 102. pmpaddr52 format

C.102.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr52.A	63:0	RW	0
DDR		RO	

C.102.4. Fields

[pmpaddr52.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 52 (or, if [pmp53cfg.A](#) == TOR, for PMP entry 53).

Type:

RW

RO

Reset value:
0

C.102.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 52) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.102.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg13].pmp52cfg[4] == 1)) {
        return CSR[pmpaddr52].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg13].pmp52cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr52].ADDR & ~mask;
    } else {
        return CSR[pmpaddr52].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp52cfg[4] == 1)) {
        return CSR[pmpaddr52].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp52cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr52].ADDR & ~mask;
    } else {
        return CSR[pmpaddr52].ADDR;
    }
}
}

```

C.103. pmpaddr53

PMP Address 53

PMP entry address

C.103.1. Attributes

CSR Address	0x3e5
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.103.2. Format

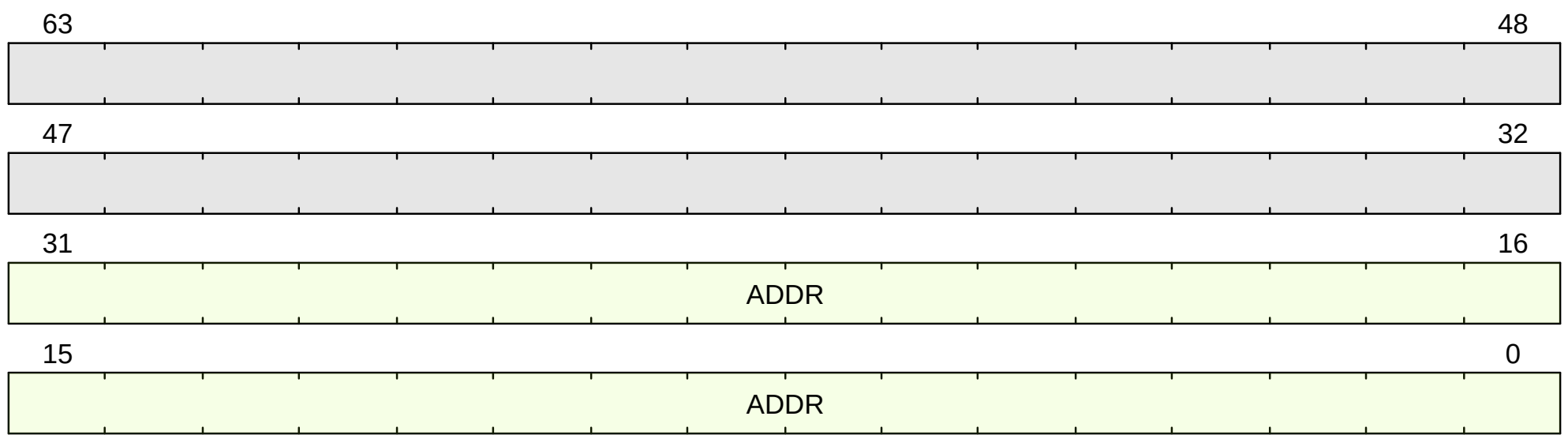


Figure 103. pmpaddr53 format

C.103.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr53.ADDR	63:0	RW	0
		RO	

C.103.4. Fields

[pmpaddr53.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 53 (or, if [pmp54cfg.A](#) == TOR, for PMP entry 54).

Type:

RW

RO

Reset value:
0

C.103.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 53) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.103.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg13].pmp53cfg[4] == 1)) {
        return CSR[pmpaddr53].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg13].pmp53cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr53].ADDR & ~mask;
    } else {
        return CSR[pmpaddr53].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp53cfg[4] == 1)) {
        return CSR[pmpaddr53].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp53cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr53].ADDR & ~mask;
    } else {
        return CSR[pmpaddr53].ADDR;
    }
}
}

```


C.104. pmpaddr54

PMP Address 54

PMP entry address

C.104.1. Attributes

CSR Address	0x3e6
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.104.2. Format

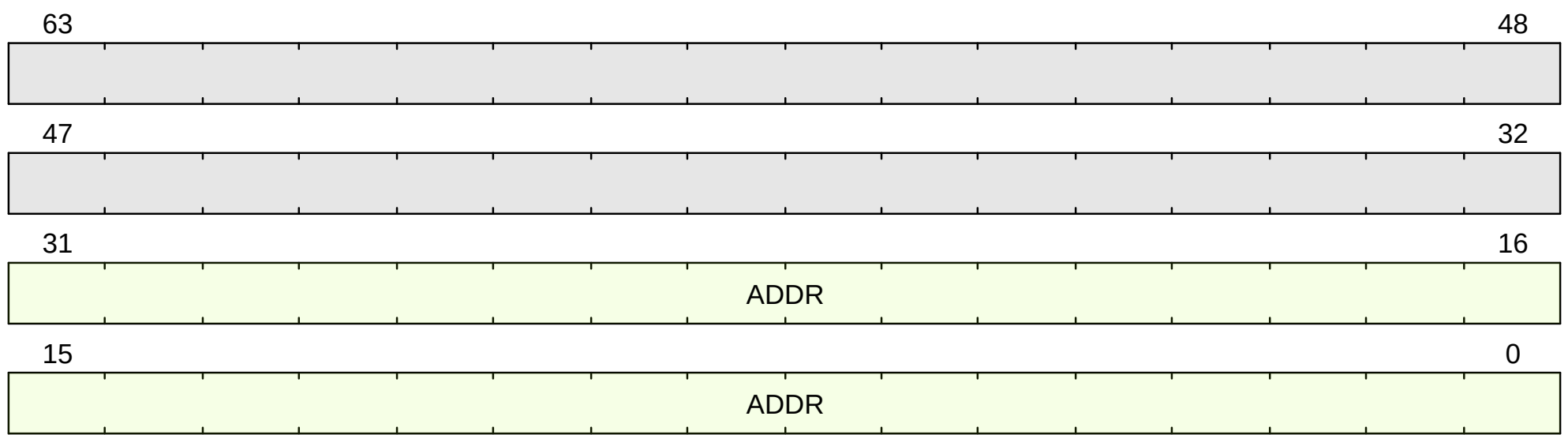


Figure 104. pmpaddr54 format

C.104.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr54.A	63:0	RW	0
DDR		RO	

C.104.4. Fields

[pmpaddr54.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 54 (or, if [pmp55cfg.A](#) == TOR, for PMP entry 55).

Type:

RW

RO

Reset value:
0

C.104.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 54) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.104.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg13].pmp54cfg[4] == 1)) {
        return CSR[pmpaddr54].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg13].pmp54cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr54].ADDR & ~mask;
    } else {
        return CSR[pmpaddr54].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp54cfg[4] == 1)) {
        return CSR[pmpaddr54].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp54cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr54].ADDR & ~mask;
    } else {
        return CSR[pmpaddr54].ADDR;
    }
}
}

```


C.105. pmpaddr55

PMP Address 55

PMP entry address

C.105.1. Attributes

CSR Address	0x3e7
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.105.2. Format

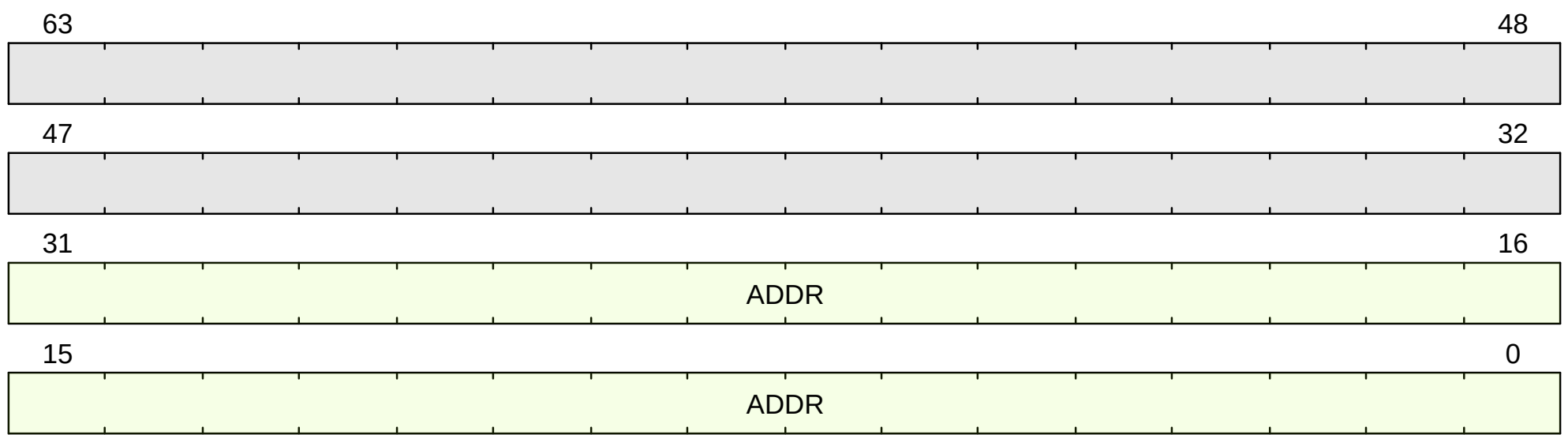


Figure 105. pmpaddr55 format

C.105.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr55.A	63:0	RW	0
DDR		RO	

C.105.4. Fields

[pmpaddr55.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 55 (or, if [pmp56cfg.A](#) == TOR, for PMP entry 56).

Type:

RW

RO

Reset value:
0

C.105.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 55) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.105.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg13].pmp55cfg[4] == 1)) {
        return CSR[pmpaddr55].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg13].pmp55cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr55].ADDR & ~mask;
    } else {
        return CSR[pmpaddr55].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg12].pmp55cfg[4] == 1)) {
        return CSR[pmpaddr55].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg12].pmp55cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr55].ADDR & ~mask;
    } else {
        return CSR[pmpaddr55].ADDR;
    }
}
}

```

C.106. pmpaddr56

PMP Address 56

PMP entry address

C.106.1. Attributes

CSR Address	0x3e8
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.106.2. Format



Figure 106. pmpaddr56 format

C.106.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr56.ADDR	63:0	RW	0
		RO	

C.106.4. Fields

[pmpaddr56.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 56 (or, if [pmp57cfg.A](#) == TOR, for PMP entry 57).

Type:

RW

RO

Reset value:
0

C.106.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 56) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.106.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp56cfg[4] == 1)) {
        return CSR[pmpaddr56].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp56cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr56].ADDR & ~mask;
    } else {
        return CSR[pmpaddr56].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp56cfg[4] == 1)) {
        return CSR[pmpaddr56].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp56cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr56].ADDR & ~mask;
    } else {
        return CSR[pmpaddr56].ADDR;
    }
}
}

```

C.107. pmpaddr57

PMP Address 57

PMP entry address

C.107.1. Attributes

CSR Address	0x3e9
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.107.2. Format

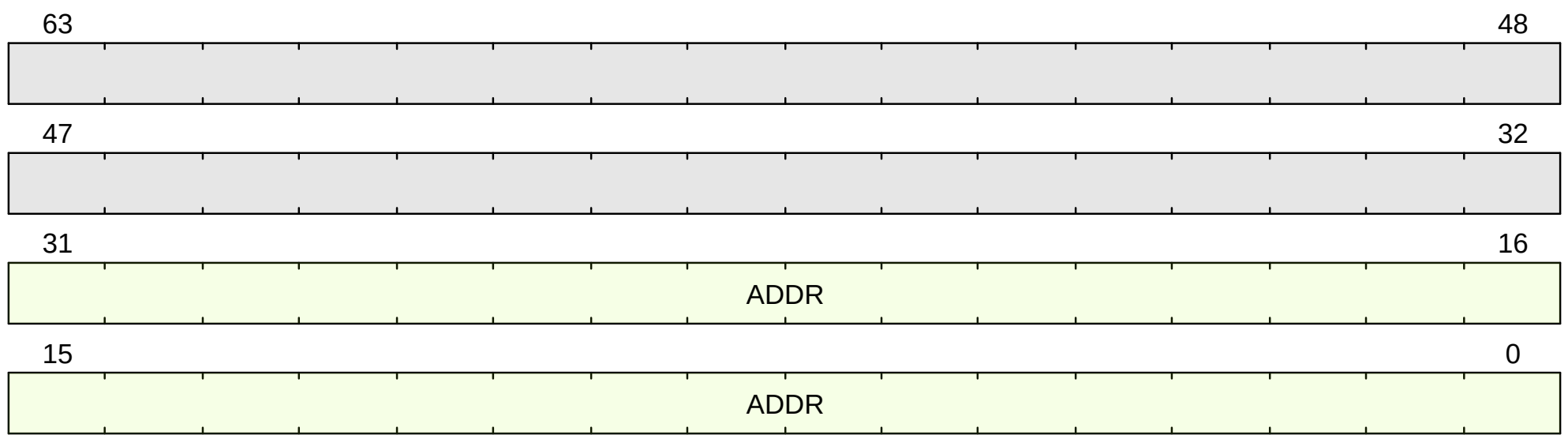


Figure 107. pmpaddr57 format

C.107.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr57.ADDR	63:0	RW	0
		RO	

C.107.4. Fields

[pmpaddr57.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 57 (or, if [pmp58cfg.A](#) == TOR, for PMP entry 58).

Type:

RW

RO

Reset value:
0

C.107.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 57) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.107.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp57cfg[4] == 1)) {
        return CSR[pmpaddr57].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp57cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr57].ADDR & ~mask;
    } else {
        return CSR[pmpaddr57].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp57cfg[4] == 1)) {
        return CSR[pmpaddr57].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp57cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr57].ADDR & ~mask;
    } else {
        return CSR[pmpaddr57].ADDR;
    }
}
}

```


C.108. pmpaddr58

PMP Address 58

PMP entry address

C.108.1. Attributes

CSR Address	0x3ea
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.108.2. Format

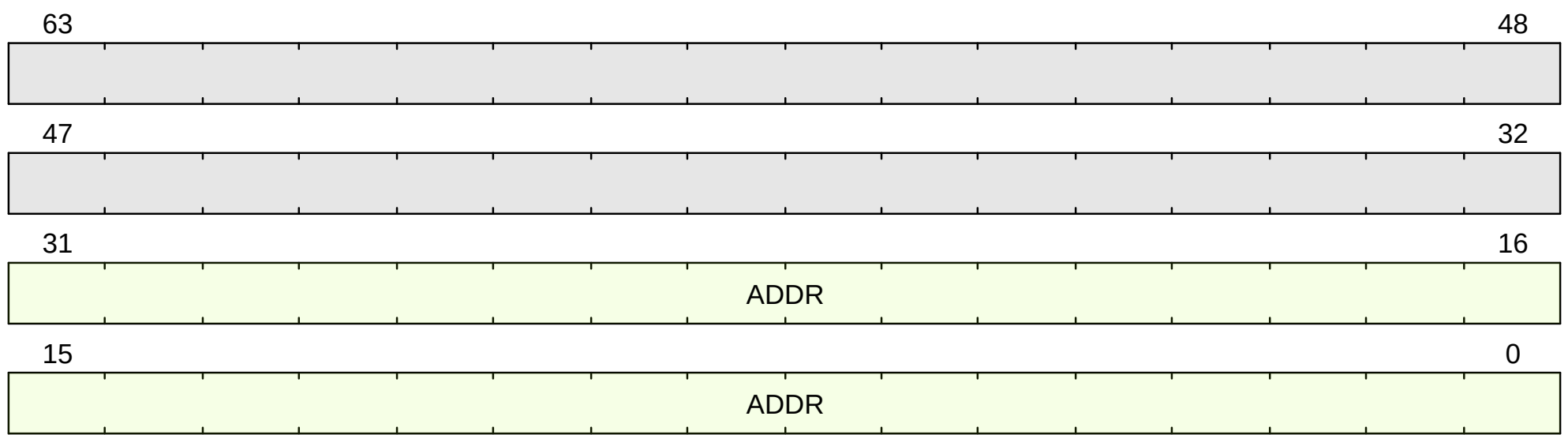


Figure 108. pmpaddr58 format

C.108.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr58.ADDR	63:0	RW	0
		RO	

C.108.4. Fields

[pmpaddr58.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 58 (or, if [pmp59cfg.A](#) == TOR, for PMP entry 59).

Type:

RW

RO

Reset value:
0

C.108.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 58) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.108.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp58cfg[4] == 1)) {
        return CSR[pmpaddr58].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp58cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr58].ADDR & ~mask;
    } else {
        return CSR[pmpaddr58].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp58cfg[4] == 1)) {
        return CSR[pmpaddr58].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp58cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr58].ADDR & ~mask;
    } else {
        return CSR[pmpaddr58].ADDR;
    }
}
}

```


C.109. pmpaddr59

PMP Address 59

PMP entry address

C.109.1. Attributes

CSR Address	0x3eb
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.109.2. Format

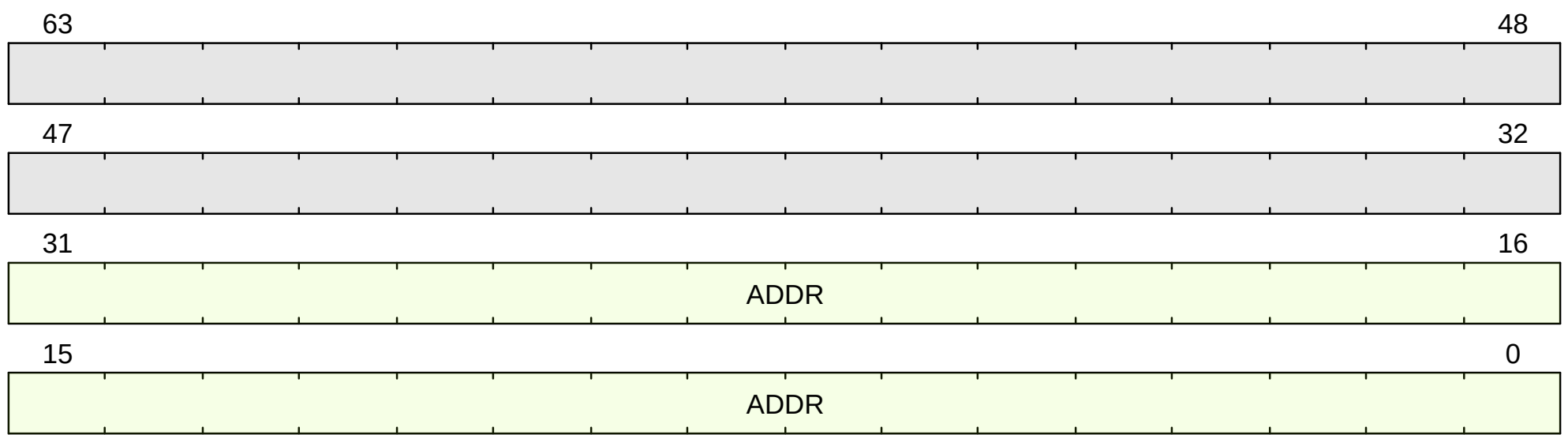


Figure 109. pmpaddr59 format

C.109.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr59.A	63:0	RW	0
DDR		RO	

C.109.4. Fields

[pmpaddr59.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 59 (or, if [pmp60cfg.A](#) == TOR, for PMP entry 60).

Type:

RW

RO

Reset value:
0

C.109.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 59) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.109.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp59cfg[4] == 1)) {
        return CSR[pmpaddr59].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp59cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr59].ADDR & ~mask;
    } else {
        return CSR[pmpaddr59].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp59cfg[4] == 1)) {
        return CSR[pmpaddr59].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp59cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr59].ADDR & ~mask;
    } else {
        return CSR[pmpaddr59].ADDR;
    }
}
}

```

C.110. pmpaddr6

PMP Address 6

PMP entry address

C.110.1. Attributes

CSR Address	0x3b6
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.110.2. Format

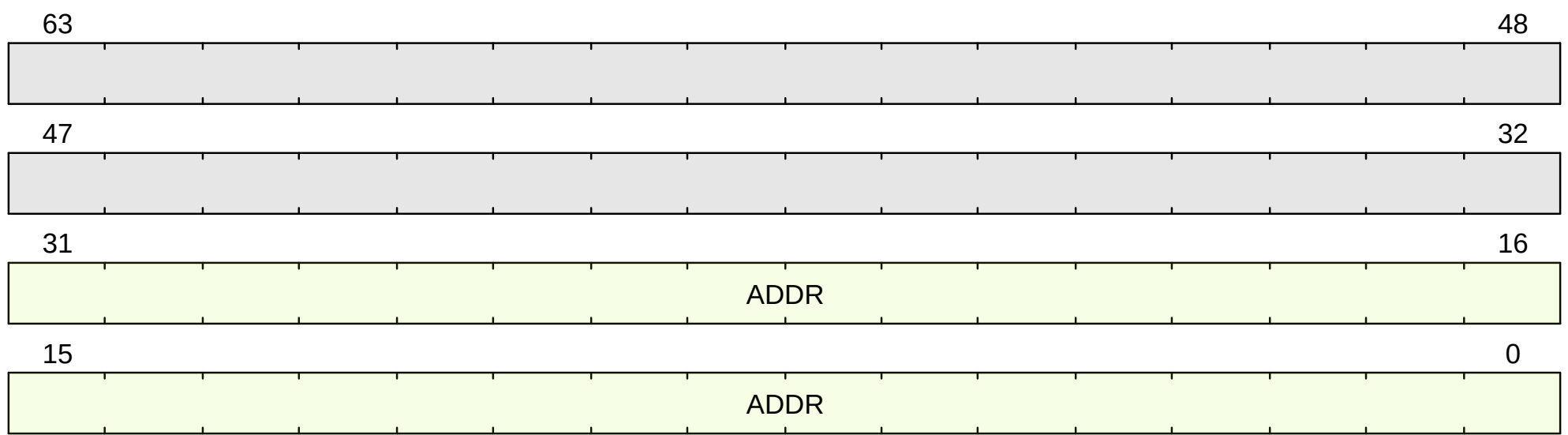


Figure 110. pmpaddr6 format

C.110.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr6.ADDR	63:0	RW	0
		RO	

C.110.4. Fields

[pmpaddr6.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 6 (or, if `pmp7cfg.A` == TOR, for PMP entry 7).

Type:

RW

RO

Reset value:
0

C.110.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 6) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.110.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg1].pmp6cfg[4] == 1)) {
        return CSR[pmpaddr6].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg1].pmp6cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr6].ADDR & ~mask;
    } else {
        return CSR[pmpaddr6].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp6cfg[4] == 1)) {
        return CSR[pmpaddr6].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp6cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr6].ADDR & ~mask;
    } else {
        return CSR[pmpaddr6].ADDR;
    }
}
}

```

C.111. pmpaddr60

PMP Address 60

PMP entry address

C.111.1. Attributes

CSR Address	0x3ec
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.111.2. Format

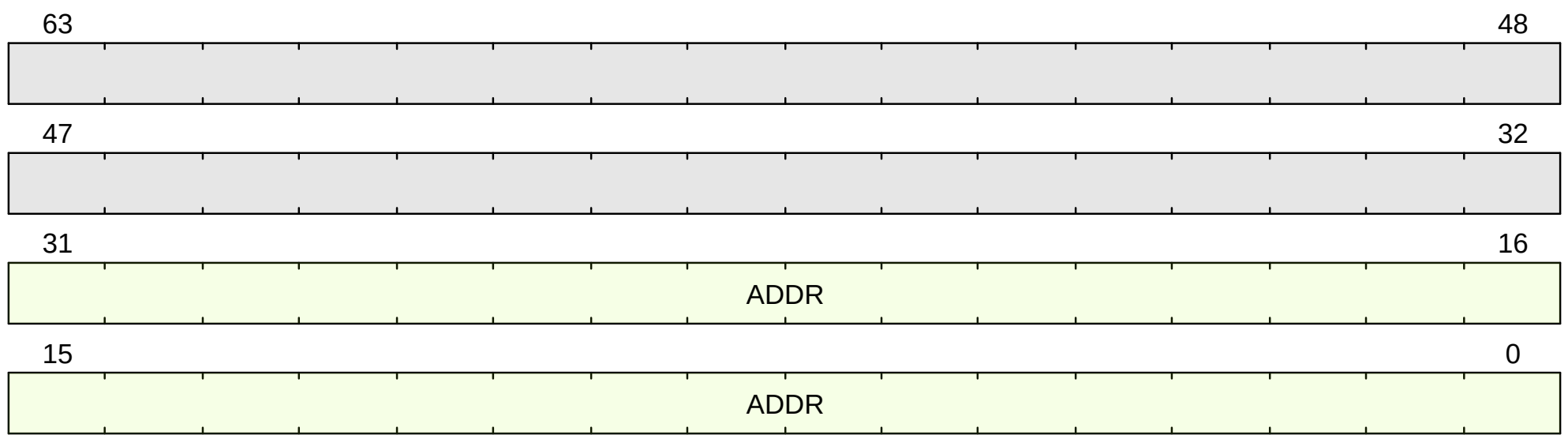


Figure 111. pmpaddr60 format

C.111.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr60.ADDR	63:0	RW	0
		RO	

C.111.4. Fields

[pmpaddr60.ADDR](#) Field

Location:

63:0

Description:

Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 60 (or, if [pmp61cfg.A](#) == TOR, for PMP entry 61).

Type:

RW

RO

Reset value:

0

C.111.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 60) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.111.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg15].pmp60cfg[4] == 1)) {
        return CSR[pmpaddr60].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg15].pmp60cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr60].ADDR & ~mask;
    } else {
        return CSR[pmpaddr60].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp60cfg[4] == 1)) {
        return CSR[pmpaddr60].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp60cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr60].ADDR & ~mask;
    } else {
        return CSR[pmpaddr60].ADDR;
    }
}
}

```


C.112. pmpaddr61

PMP Address 61

PMP entry address

C.112.1. Attributes

CSR Address	0x3ed
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.112.2. Format

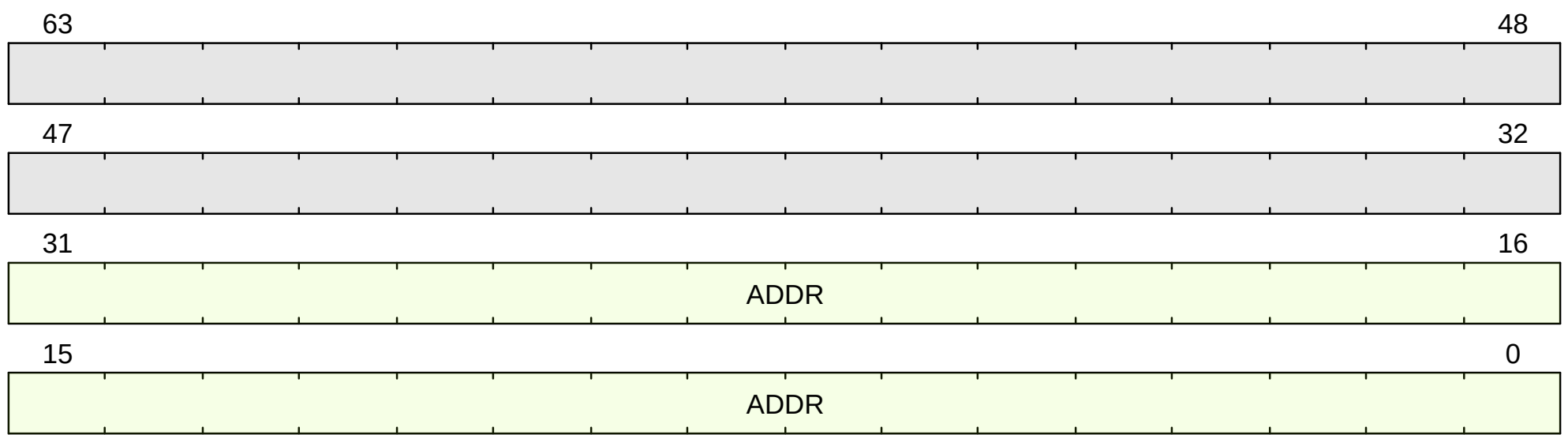


Figure 112. pmpaddr61 format

C.112.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr61.ADDR	63:0	RW	0
		RO	

C.112.4. Fields

[pmpaddr61.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 61 (or, if [pmp62cfg.A](#) == TOR, for PMP entry 62).

Type:

RW

RO

Reset value:
0

C.112.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 61) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.112.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg15].pmp61cfg[4] == 1)) {
        return CSR[pmpaddr61].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg15].pmp61cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr61].ADDR & ~mask;
    } else {
        return CSR[pmpaddr61].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp61cfg[4] == 1)) {
        return CSR[pmpaddr61].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp61cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr61].ADDR & ~mask;
    } else {
        return CSR[pmpaddr61].ADDR;
    }
}
}

```


C.113. pmpaddr62

PMP Address 62

PMP entry address

C.113.1. Attributes

CSR Address	0x3ee
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.113.2. Format

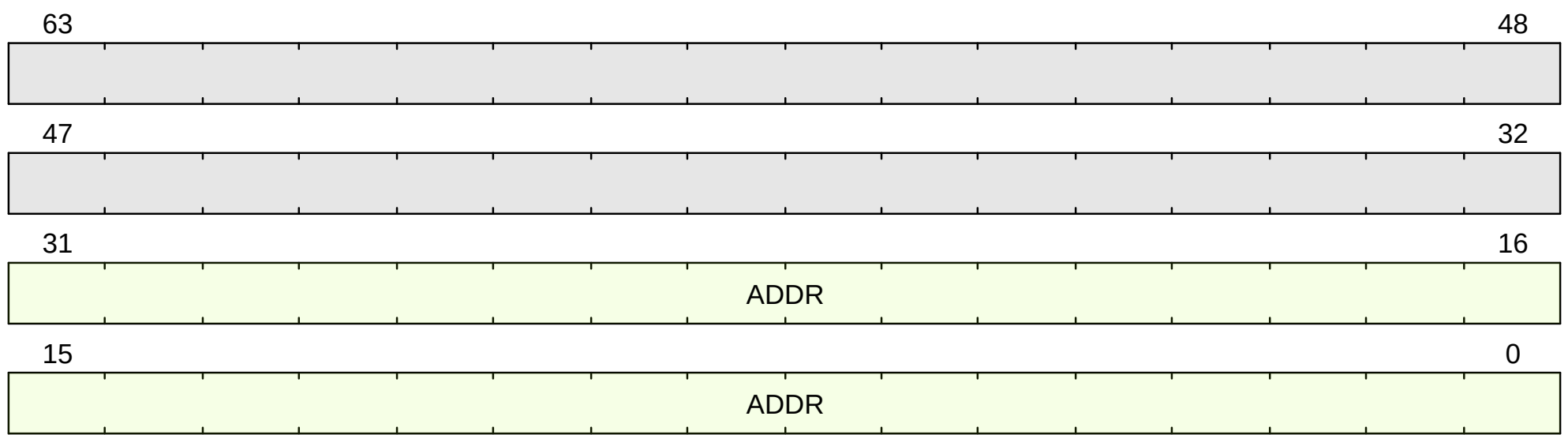


Figure 113. pmpaddr62 format

C.113.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr62.ADDR	63:0	RW	0
		RO	

C.113.4. Fields

[pmpaddr62.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 62 (or, if [pmp63cfg.A](#) == TOR, for PMP entry 63).

Type:

RW

RO

Reset value:
0

C.113.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 62) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
return csr_value.ADDR;
}

```

C.113.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg15].pmp62cfg[4] == 1)) {
        return CSR[pmpaddr62].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg15].pmp62cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr62].ADDR & ~mask;
    } else {
        return CSR[pmpaddr62].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp62cfg[4] == 1)) {
        return CSR[pmpaddr62].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp62cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr62].ADDR & ~mask;
    } else {
        return CSR[pmpaddr62].ADDR;
    }
}
}

```

C.114. pmpaddr63

PMP Address 63

PMP entry address

C.114.1. Attributes

CSR Address	0x3ef
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.114.2. Format

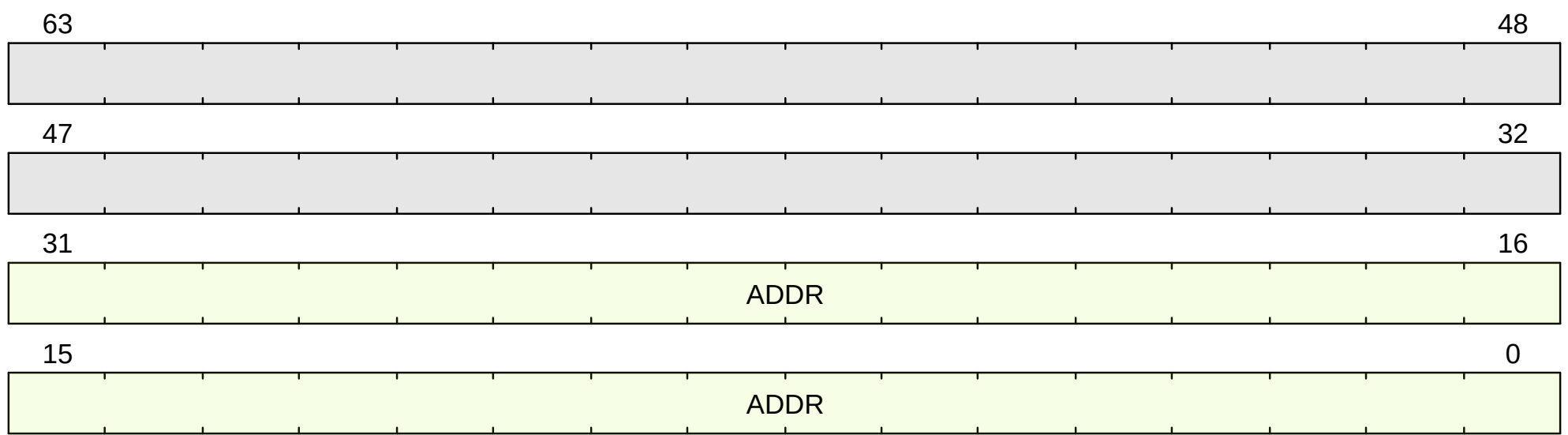


Figure 114. pmpaddr63 format

C.114.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr63.ADDR	63:0	RW	0
		RO	

C.114.4. Fields

[pmpaddr63.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 63 (or, if [pmp64cfg.A](#) == TOR, for PMP entry 64).

Type:

RW

RO

Reset value:
0

C.114.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 63) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.114.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg15].pmp63cfg[4] == 1)) {
        return CSR[pmpaddr63].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg15].pmp63cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr63].ADDR & ~mask;
    } else {
        return CSR[pmpaddr63].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg14].pmp63cfg[4] == 1)) {
        return CSR[pmpaddr63].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg14].pmp63cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr63].ADDR & ~mask;
    } else {
        return CSR[pmpaddr63].ADDR;
    }
}
}

```

C.115. pmpaddr7

PMP Address 7

PMP entry address

C.115.1. Attributes

CSR Address	0x3b7
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.115.2. Format

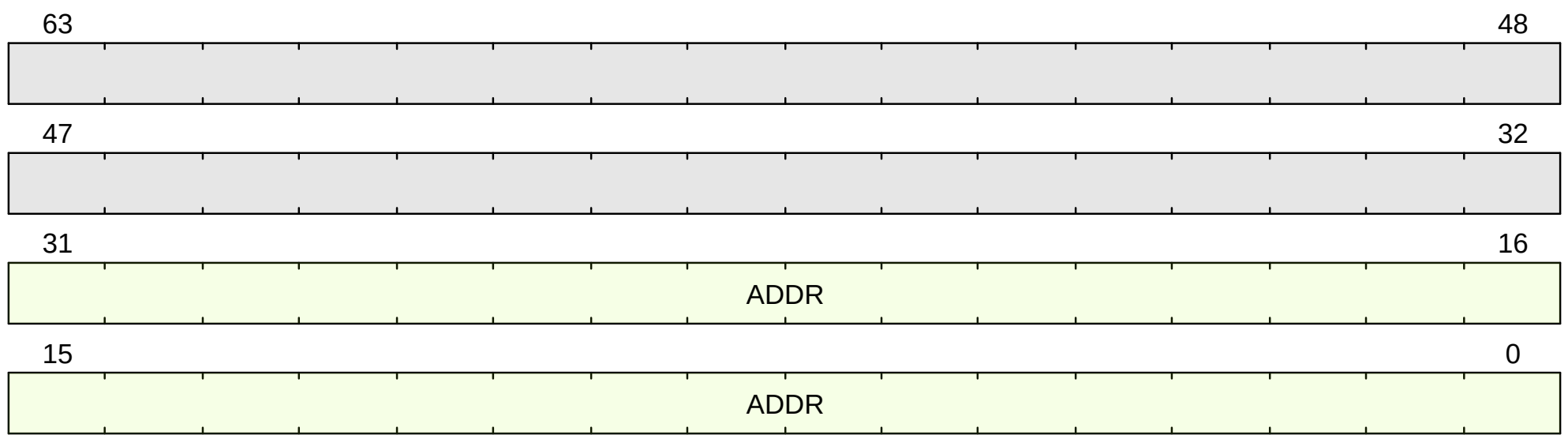


Figure 115. pmpaddr7 format

C.115.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr7.ADDR	63:0	RW	0
		RO	

C.115.4. Fields

[pmpaddr7.ADDR](#) Field

Location:

63:0

Description:

Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 7 (or, if [pmp8cfg.A](#) == TOR, for PMP entry 8).

Type:

RW

RO

Reset value:

0

C.115.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 7) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.115.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg1].pmp7cfg[4] == 1)) {
        return CSR[pmpaddr7].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg1].pmp7cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr7].ADDR & ~mask;
    } else {
        return CSR[pmpaddr7].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg0].pmp7cfg[4] == 1)) {
        return CSR[pmpaddr7].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg0].pmp7cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr7].ADDR & ~mask;
    } else {
        return CSR[pmpaddr7].ADDR;
    }
}
}

```


C.116. pmpaddr8

PMP Address 8

PMP entry address

C.116.1. Attributes

CSR Address	0x3b8
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.116.2. Format

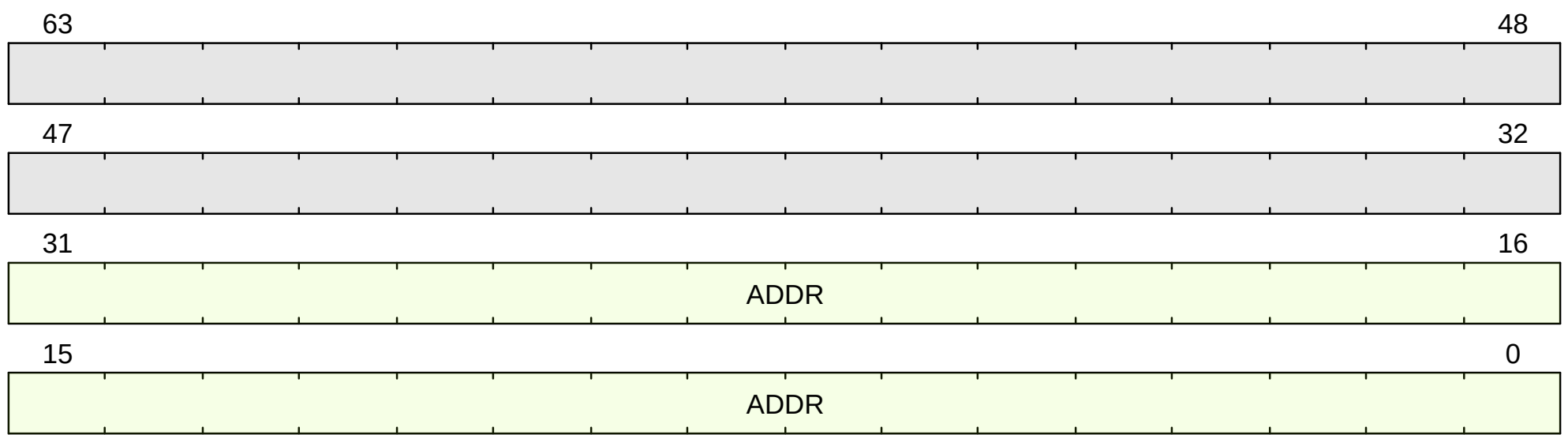


Figure 116. pmpaddr8 format

C.116.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr8.ADDR	63:0	RW	0
		RO	

C.116.4. Fields

[pmpaddr8.ADDR](#) Field

Location:
63:0

Description:
Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 8 (or, if `pmp9cfg.A` == TOR, for PMP entry 9).

Type:

RW

RO

Reset value:
0

C.116.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 '<< (PHYS_ADDR_WIDTH - 2)) - 1)) {  
    return UNDEFINED_LEGAL_DETERMINISTIC;  
} else if (NUM_PMP_ENTRIES <= 8) {
```

```

return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.116.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp8cfg[4] == 1)) {
        return CSR[pmpaddr8].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp8cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr8].ADDR & ~mask;
    } else {
        return CSR[pmpaddr8].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp8cfg[4] == 1)) {
        return CSR[pmpaddr8].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp8cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr8].ADDR & ~mask;
    } else {
        return CSR[pmpaddr8].ADDR;
    }
}
}

```


C.117. pmpaddr9

PMP Address 9

PMP entry address

C.117.1. Attributes

CSR Address	0x3b9
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.117.2. Format

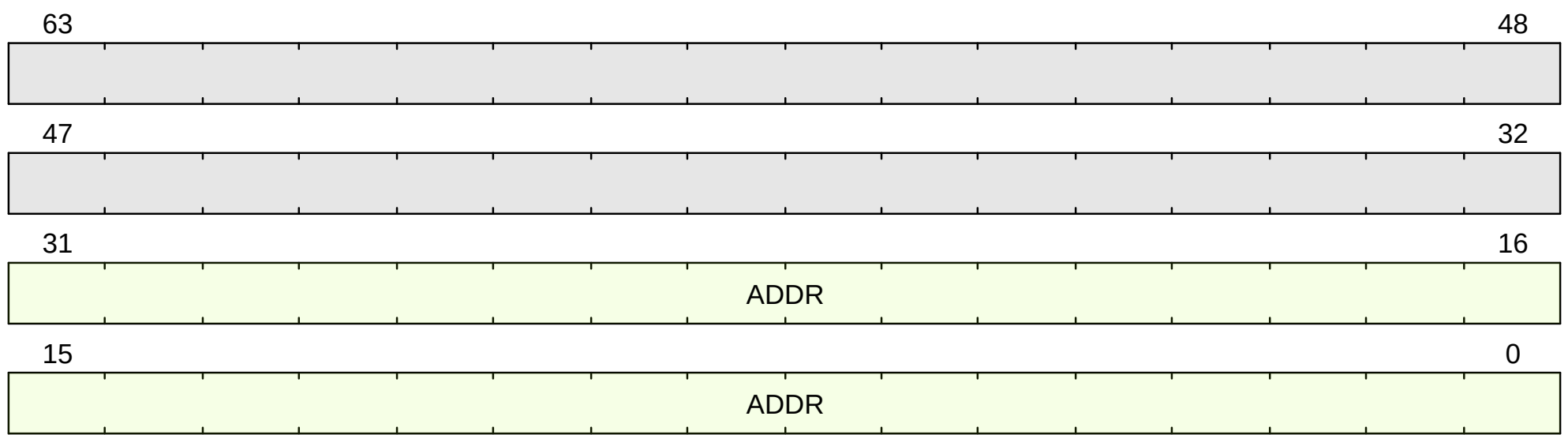


Figure 117. pmpaddr9 format

C.117.3. Field Summary

Name	Location	Type	Reset Value
pmpaddr9.ADDR	63:0	RW	0
		RO	

C.117.4. Fields

[pmpaddr9.ADDR](#) Field

Location:

63:0

Description:

Bits PHYS_ADDR_WIDTH-1:2 of the address specifier for PMP entry 9 (or, if [pmp10cfg.A](#) == TOR, for PMP entry 10).

Type:

RW

RO

Reset value:

0

C.117.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
ADDR = if (csr_value.ADDR >= ((1 << (PHYS_ADDR_WIDTH - 2)) - 1)) {
    return UNDEFINED_LEGAL_DETERMINISTIC;
} else if (NUM_PMP_ENTRIES <= 9) {
```

```

    return UNDEFINED_LEGAL_DETERMINISTIC;
} else {
    return csr_value.ADDR;
}

```

C.117.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```

if (MXLEN == 32) {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp9cfg[4] == 1)) {
        return CSR[pmpaddr9].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp9cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr9].ADDR & ~mask;
    } else {
        return CSR[pmpaddr9].ADDR;
    }
} else {
    if ((PMP_GRANULARITY >= 16) && (CSR[pmpcfg2].pmp9cfg[4] == 1)) {
        return CSR[pmpaddr9].ADDR | {PMP_GRANULARITY - 3{1'b1}};
    } else if ((PMP_GRANULARITY >= 8) && (CSR[pmpcfg2].pmp9cfg[4] == 0)) {
        Bits<PHYS_ADDR_WIDTH - 2> mask = {PMP_GRANULARITY - 2{1'b1}};
        return CSR[pmpaddr9].ADDR & ~mask;
    } else {
        return CSR[pmpaddr9].ADDR;
    }
}
}

```

C.118. pmpcfg0

PMP Configuration Register 0

PMP entry configuration

C.118.1. Attributes

CSR Address	0x3a0
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.118.2. Format

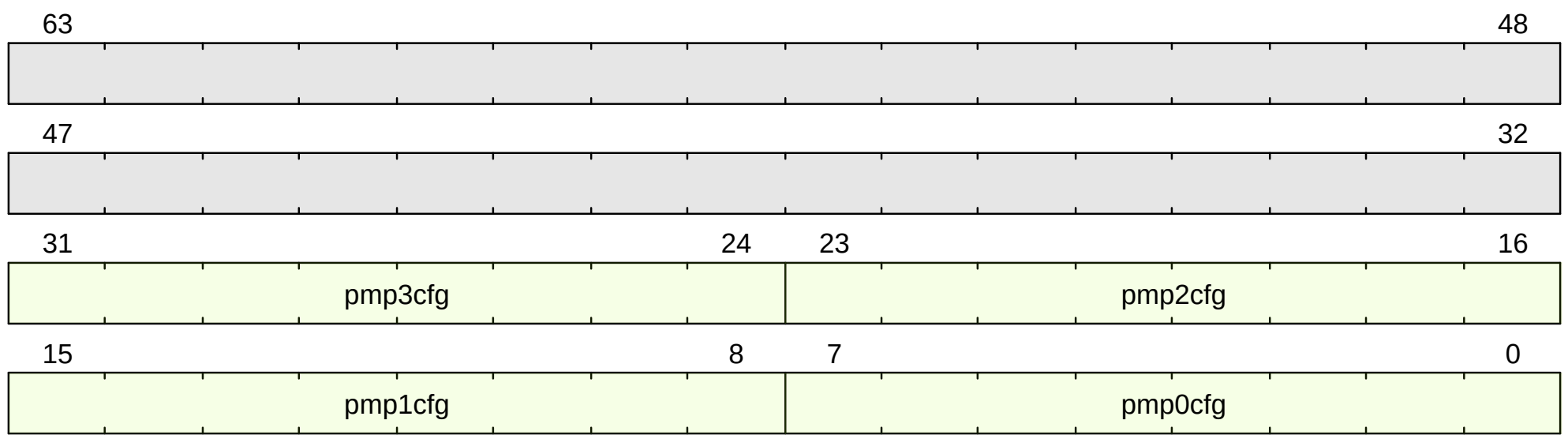


Figure 118. pmpcfg0 format

C.118.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg0.pmp0cfg	7:0	RW-R	0
		RO	
pmpcfg0.pmp1cfg	15:8	RW-R	0
		RO	
pmpcfg0.pmp2cfg	23:16	RW-R	0
		RO	
pmpcfg0.pmp3cfg	31:24	RW-R	0
		RO	
pmpcfg0.pmp4cfg	39:32	RW-R	0
		RO	
pmpcfg0.pmp5cfg	47:40	RW-R	0
		RO	
pmpcfg0.pmp6cfg	55:48	RW-R	0
		RO	
pmpcfg0.pmp7cfg	63:56	RW-R	0
		RO	

C.118.4. Fields

[pmpcfg0.pmp0cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 0

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcf0.pmp1cfg Field

Location:

15:8

Description:

PMP configuration for entry 1

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp2cfg Field

Location:

23:16

Description:

PMP configuration for entry 2

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp3cfg Field

Location:

31:24

Description:

PMP configuration for entry 3

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp4cfg Field



pmp4cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 4

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 38:37 ! *Reserved* Writes shall be ignored.
h! A ! 36:35
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp5cfg Field



pmp5cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 5

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 46:45 ! *Reserved* Writes shall be ignored.
h! A ! 44:43
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp6cfg Field



pmp6cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

55:48

Description:

PMP configuration for entry 6

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg0.pmp7cfg Field



pmp7cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

63:56

Description:

PMP configuration for entry 7

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.118.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp0cfg = if ((CSR[pmpcfg0].pmp0cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp0cfg & 0x1) == 0) && ((csr_value.pmp0cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp0cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp0cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp0cfg;

pmp1cfg = if ((CSR[pmpcfg0].pmp1cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp1cfg & 0x1) == 0) && ((csr_value.pmp1cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp1cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp1cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp1cfg;

pmp2cfg = if ((CSR[pmpcfg0].pmp2cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp2cfg & 0x1) == 0) && ((csr_value.pmp2cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp2cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp2cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp2cfg;

pmp3cfg = if ((CSR[pmpcfg0].pmp3cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp3cfg & 0x1) == 0) && ((csr_value.pmp3cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp3cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp3cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp3cfg;

pmp4cfg = if ((CSR[pmpcfg0].pmp4cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp4cfg & 0x1) == 0) && ((csr_value.pmp4cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp4cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp4cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp4cfg;

pmp5cfg = if ((xlen() == 64) && (CSR[pmpcfg0].pmp5cfg & 0x80) == 0) {
    # entry is not locked
```

```

    if (!(((csr_value.pmp5cfg & 0x1) == 0) && ((csr_value.pmp5cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp5cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp5cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp5cfg;

pmp6cfg = if ((xlen() == 64) && (CSR[pmpcfg0].pmp6cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp6cfg & 0x1) == 0) && ((csr_value.pmp6cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp6cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp6cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp6cfg;

pmp7cfg = if ((xlen() == 64) && (CSR[pmpcfg0].pmp7cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp7cfg & 0x1) == 0) && ((csr_value.pmp7cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp7cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp7cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg0].pmp7cfg;

```

C.119. pmpcfg10

PMP Configuration Register 10

PMP entry configuration

C.119.1. Attributes

CSR Address	0x3aa
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.119.2. Format

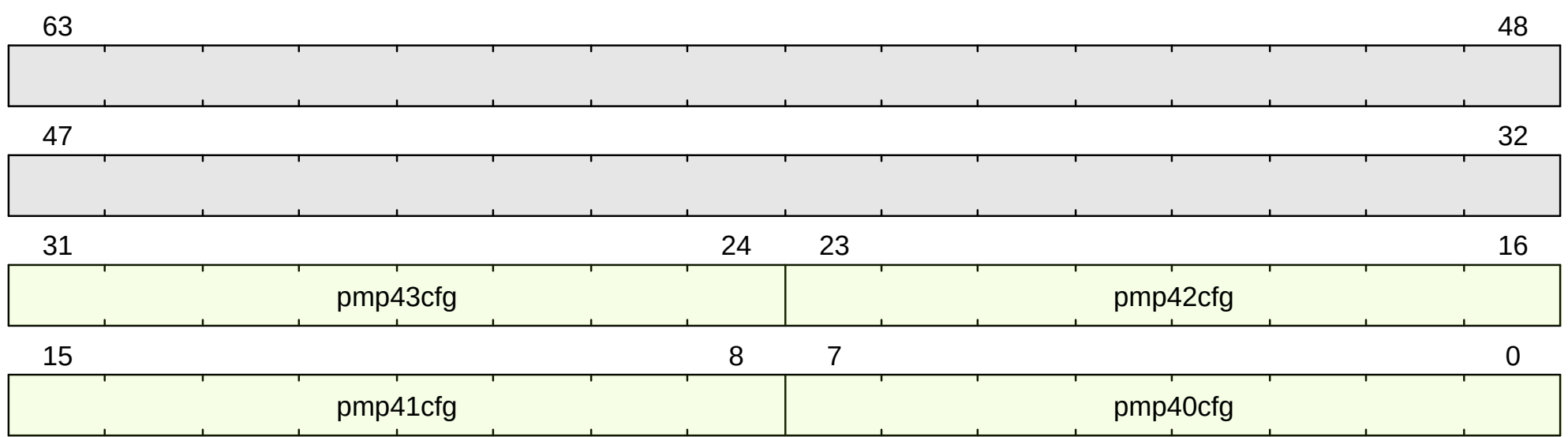


Figure 119. pmpcfg10 format

C.119.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg10.pmp40cfg	7:0	RW-R	0
		RO	
pmpcfg10.pmp41cfg	15:8	RW-R	0
		RO	
pmpcfg10.pmp42cfg	23:16	RW-R	0
		RO	
pmpcfg10.pmp43cfg	31:24	RW-R	0
		RO	
pmpcfg10.pmp44cfg	39:32	RW-R	0
		RO	
pmpcfg10.pmp45cfg	47:40	RW-R	0
		RO	
pmpcfg10.pmp46cfg	55:48	RW-R	0
		RO	
pmpcfg10.pmp47cfg	63:56	RW-R	0
		RO	

C.119.4. Fields

[pmpcfg10.pmp40cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 40

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp41cfg Field

Location:

15:8

Description:

PMP configuration for entry 41

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp42cfg Field

Location:

23:16

Description:

PMP configuration for entry 42

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp43cfg Field

Location:

31:24

Description:

PMP configuration for entry 43

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp44cfg Field



pmp44cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 44

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 38:37 ! *Reserved* Writes shall be ignored.

h! A ! 36:35

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp45cfg Field



pmp45cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 45

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 46:45 ! *Reserved* Writes shall be ignored.

h! A ! 44:43

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp46cfg Field



pmp46cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 46

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg10.pmp47cfg Field



pmp47cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 47

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.119.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp40cfg = if ((CSR[pmpcfg10].pmp40cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp40cfg & 0x1) == 0) && ((csr_value.pmp40cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp40cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp40cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp40cfg;

pmp41cfg = if ((CSR[pmpcfg10].pmp41cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp41cfg & 0x1) == 0) && ((csr_value.pmp41cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp41cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp41cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp41cfg;

pmp42cfg = if ((CSR[pmpcfg10].pmp42cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp42cfg & 0x1) == 0) && ((csr_value.pmp42cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp42cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp42cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp42cfg;

pmp43cfg = if ((CSR[pmpcfg10].pmp43cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp43cfg & 0x1) == 0) && ((csr_value.pmp43cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp43cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp43cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp43cfg;

pmp44cfg = if ((CSR[pmpcfg10].pmp44cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp44cfg & 0x1) == 0) && ((csr_value.pmp44cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp44cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp44cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp44cfg;

pmp45cfg = if ((xlen() == 64) && (CSR[pmpcfg10].pmp45cfg & 0x80) == 0) {
    # entry is not locked
```

```

    if (!(((csr_value.pmp45cfg & 0x1) == 0) && ((csr_value.pmp45cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp45cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp45cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp45cfg;

pmp46cfg = if ((xlen() == 64) && (CSR[pmpcfg10].pmp46cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp46cfg & 0x1) == 0) && ((csr_value.pmp46cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp46cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp46cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp46cfg;

pmp47cfg = if ((xlen() == 64) && (CSR[pmpcfg10].pmp47cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp47cfg & 0x1) == 0) && ((csr_value.pmp47cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp47cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp47cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg10].pmp47cfg;

```

C.120. pmpcfg12

PMP Configuration Register 12

PMP entry configuration

C.120.1. Attributes

CSR Address	0x3ac
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.120.2. Format

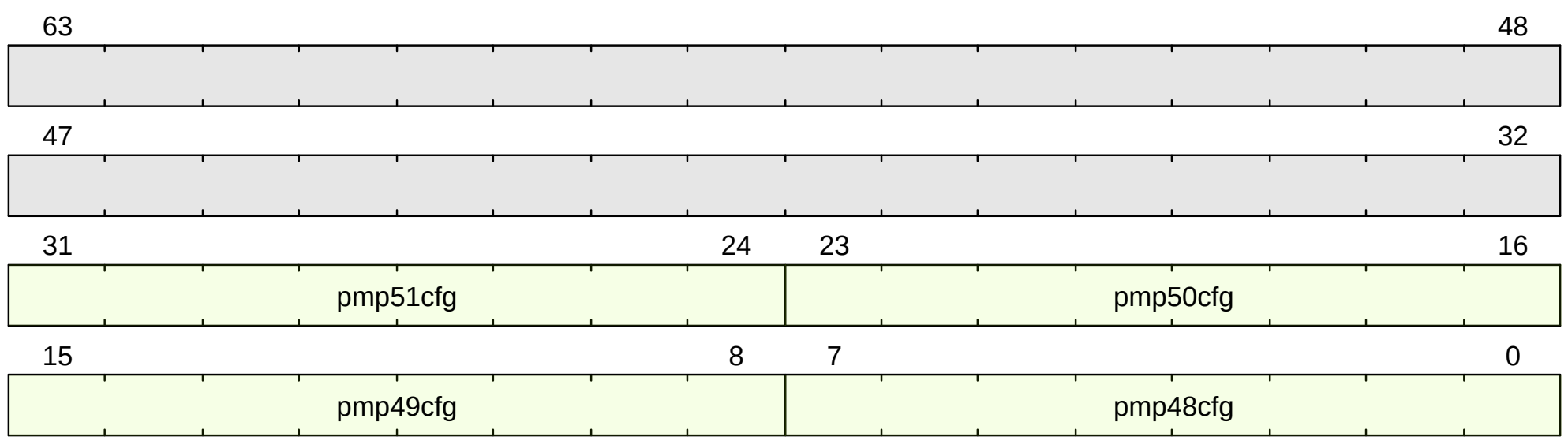


Figure 120. pmpcfg12 format

C.120.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg12.pmp48cfg	7:0	RW-R	0
		RO	
pmpcfg12.pmp49cfg	15:8	RW-R	0
		RO	
pmpcfg12.pmp50cfg	23:16	RW-R	0
		RO	
pmpcfg12.pmp51cfg	31:24	RW-R	0
		RO	
pmpcfg12.pmp52cfg	39:32	RW-R	0
		RO	
pmpcfg12.pmp53cfg	47:40	RW-R	0
		RO	
pmpcfg12.pmp54cfg	55:48	RW-R	0
		RO	
pmpcfg12.pmp55cfg	63:56	RW-R	0
		RO	

C.120.4. Fields

[pmpcfg12.pmp48cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 48

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp49cfg Field

Location:

15:8

Description:

PMP configuration for entry 49

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp50cfg Field

Location:

23:16

Description:

PMP configuration for entry 50

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp51cfg Field

Location:

31:24

Description:

PMP configuration for entry 51

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp52cfg Field



pmp52cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 52

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 38:37 ! *Reserved* Writes shall be ignored.

h! A ! 36:35

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp53cfg Field



pmp53cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 53

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 46:45 ! *Reserved* Writes shall be ignored.

h! A ! 44:43

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp54cfg Field



pmp54cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 54

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg12.pmp55cfg Field



pmp55cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 55

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.120.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp48cfg = if ((CSR[pmpcfg12].pmp48cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp48cfg & 0x1) == 0) && ((csr_value.pmp48cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp48cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp48cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp48cfg;

pmp49cfg = if ((CSR[pmpcfg12].pmp49cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp49cfg & 0x1) == 0) && ((csr_value.pmp49cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp49cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp49cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp49cfg;

pmp50cfg = if ((CSR[pmpcfg12].pmp50cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp50cfg & 0x1) == 0) && ((csr_value.pmp50cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp50cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp50cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp50cfg;

pmp51cfg = if ((CSR[pmpcfg12].pmp51cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp51cfg & 0x1) == 0) && ((csr_value.pmp51cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp51cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp51cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp51cfg;

pmp52cfg = if ((CSR[pmpcfg12].pmp52cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp52cfg & 0x1) == 0) && ((csr_value.pmp52cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp52cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp52cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp52cfg;

pmp53cfg = if ((xlen() == 64) && (CSR[pmpcfg12].pmp53cfg & 0x80) == 0) {
    # entry is not locked
```

```

if (!(((csr_value.pmp53cfg & 0x1) == 0) && ((csr_value.pmp53cfg & 0x2) == 0x2))) {
    # not R = 0, W =1, which is reserved
    if ((PMP_GRANULARITY < 2) ||
        ((csr_value.pmp53cfg & 0x18) != 0x10)) {
        # NA4 is not allowed when PMP granularity is larger than 4 bytes
        return csr_value.pmp53cfg;
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp53cfg;

pmp54cfg = if ((xlen() == 64) && (CSR[pmpcfg12].pmp54cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp54cfg & 0x1) == 0) && ((csr_value.pmp54cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp54cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp54cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp54cfg;

pmp55cfg = if ((xlen() == 64) && (CSR[pmpcfg12].pmp55cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp55cfg & 0x1) == 0) && ((csr_value.pmp55cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp55cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp55cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg12].pmp55cfg;

```

C.121. pmpcfg14

PMP Configuration Register 14

PMP entry configuration

C.121.1. Attributes

CSR Address	0x3ae
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.121.2. Format

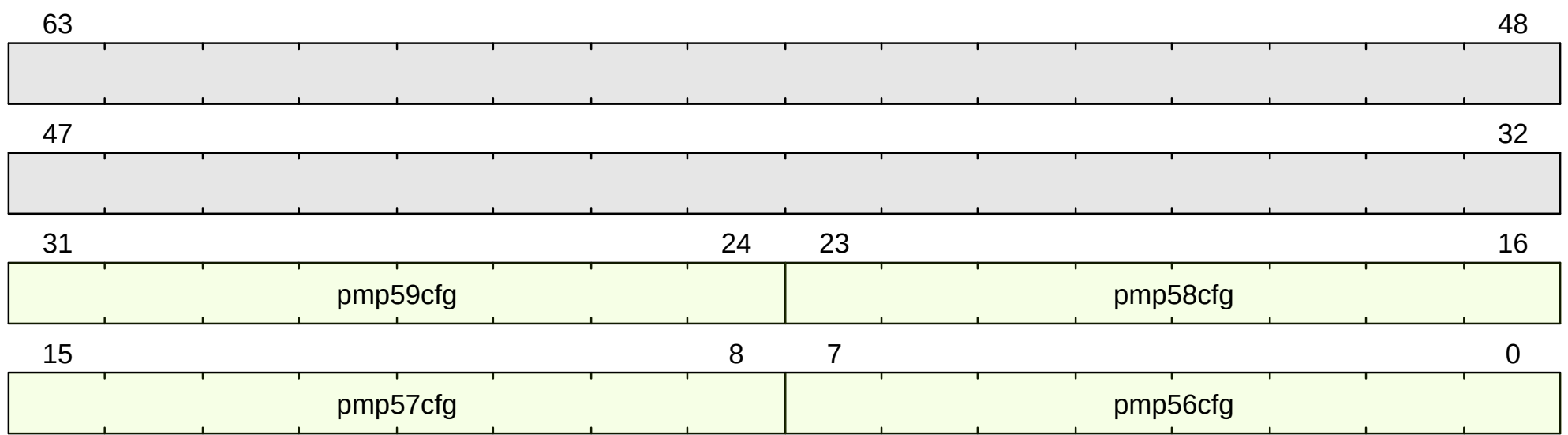


Figure 121. pmpcfg14 format

C.121.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg14.pmp56cfg	7:0	RW-R	0
		RO	
pmpcfg14.pmp57cfg	15:8	RW-R	0
		RO	
pmpcfg14.pmp58cfg	23:16	RW-R	0
		RO	
pmpcfg14.pmp59cfg	31:24	RW-R	0
		RO	
pmpcfg14.pmp60cfg	39:32	RW-R	0
		RO	
pmpcfg14.pmp61cfg	47:40	RW-R	0
		RO	
pmpcfg14.pmp62cfg	55:48	RW-R	0
		RO	
pmpcfg14.pmp63cfg	63:56	RW-R	0
		RO	

C.121.4. Fields

[pmpcfg14.pmp56cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 56

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp57cfg Field

Location:

15:8

Description:

PMP configuration for entry 57

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp58cfg Field

Location:

23:16

Description:

PMP configuration for entry 58

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp59cfg Field

Location:

31:24

Description:

PMP configuration for entry 59

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp60cfg Field



pmp60cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 60

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 38:37 ! *Reserved* Writes shall be ignored.
h! A ! 36:35
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp61cfg Field



pmp61cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 61

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 46:45 ! *Reserved* Writes shall be ignored.
h! A ! 44:43
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp62cfg Field



pmp62cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 62

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg14.pmp63cfg Field



pmp63cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 63

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.121.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp56cfg = if ((CSR[pmpcfg14].pmp56cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp56cfg & 0x1) == 0) && ((csr_value.pmp56cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp56cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp56cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp56cfg;

pmp57cfg = if ((CSR[pmpcfg14].pmp57cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp57cfg & 0x1) == 0) && ((csr_value.pmp57cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp57cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp57cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp57cfg;

pmp58cfg = if ((CSR[pmpcfg14].pmp58cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp58cfg & 0x1) == 0) && ((csr_value.pmp58cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp58cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp58cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp58cfg;

pmp59cfg = if ((CSR[pmpcfg14].pmp59cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp59cfg & 0x1) == 0) && ((csr_value.pmp59cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp59cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp59cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp59cfg;

pmp60cfg = if ((CSR[pmpcfg14].pmp60cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp60cfg & 0x1) == 0) && ((csr_value.pmp60cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp60cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp60cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp60cfg;

pmp61cfg = if ((xlen() == 64) && (CSR[pmpcfg14].pmp61cfg & 0x80) == 0) {
    # entry is not locked
```

```

    if (!(((csr_value.pmp61cfg & 0x1) == 0) && ((csr_value.pmp61cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp61cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp61cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp61cfg;

pmp62cfg = if ((xlen() == 64) && (CSR[pmpcfg14].pmp62cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp62cfg & 0x1) == 0) && ((csr_value.pmp62cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp62cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp62cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp62cfg;

pmp63cfg = if ((xlen() == 64) && (CSR[pmpcfg14].pmp63cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp63cfg & 0x1) == 0) && ((csr_value.pmp63cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp63cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp63cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg14].pmp63cfg;

```


C.122. pmpcfg2

PMP Configuration Register 2

PMP entry configuration

C.122.1. Attributes

CSR Address	0x3a2
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.122.2. Format

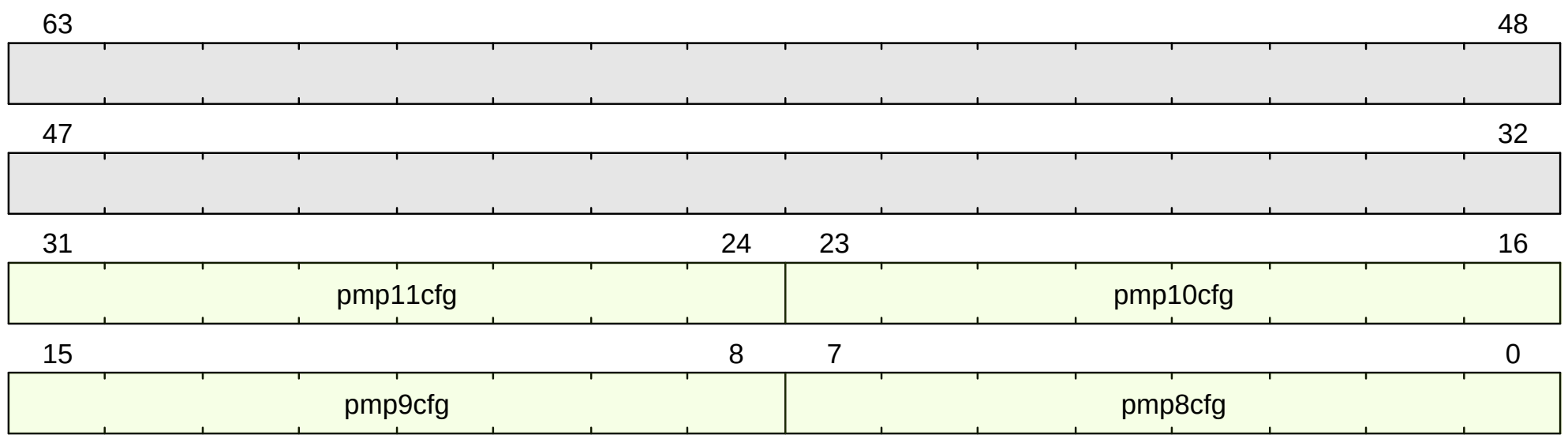


Figure 122. pmpcfg2 format

C.122.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg2.pmp8cfg	7:0	RW-R	0
		RO	
pmpcfg2.pmp9cfg	15:8	RW-R	0
		RO	
pmpcfg2.pmp10cfg	23:16	RW-R	0
		RO	
pmpcfg2.pmp11cfg	31:24	RW-R	0
		RO	
pmpcfg2.pmp12cfg	39:32	RW-R	0
		RO	
pmpcfg2.pmp13cfg	47:40	RW-R	0
		RO	
pmpcfg2.pmp14cfg	55:48	RW-R	0
		RO	
pmpcfg2.pmp15cfg	63:56	RW-R	0
		RO	

C.122.4. Fields

[pmpcfg2.pmp8cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 8

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp9cfg Field

Location:

15:8

Description:

PMP configuration for entry 9

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp10cfg Field

Location:

23:16

Description:

PMP configuration for entry 10

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp11cfg Field

Location:

31:24

Description:

PMP configuration for entry 11

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp12cfg Field



pmp12cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 12

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 38:37 ! *Reserved* Writes shall be ignored.

h! A ! 36:35

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp13cfg Field



pmp13cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 13

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 46:45 ! *Reserved* Writes shall be ignored.

h! A ! 44:43

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp14cfg Field



pmp14cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 14

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg2.pmp15cfg Field



pmp15cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

63:56

Description:

PMP configuration for entry 15

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.122.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp8cfg = if ((CSR[pmpcfg2].pmp8cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp8cfg & 0x1) == 0) && ((csr_value.pmp8cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp8cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp8cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp8cfg;

pmp9cfg = if ((CSR[pmpcfg2].pmp9cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp9cfg & 0x1) == 0) && ((csr_value.pmp9cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp9cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp9cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp9cfg;

pmp10cfg = if ((CSR[pmpcfg2].pmp10cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp10cfg & 0x1) == 0) && ((csr_value.pmp10cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp10cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp10cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp10cfg;

pmp11cfg = if ((CSR[pmpcfg2].pmp11cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp11cfg & 0x1) == 0) && ((csr_value.pmp11cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp11cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp11cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp11cfg;

pmp12cfg = if ((CSR[pmpcfg2].pmp12cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp12cfg & 0x1) == 0) && ((csr_value.pmp12cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp12cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp12cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp12cfg;

pmp13cfg = if ((xlen() == 64) && (CSR[pmpcfg2].pmp13cfg & 0x80) == 0) {
    # entry is not locked
```



```

    if (!(((csr_value.pmp13cfg & 0x1) == 0) && ((csr_value.pmp13cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp13cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp13cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp13cfg;

pmp14cfg = if ((xlen() == 64) && (CSR[pmpcfg2].pmp14cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp14cfg & 0x1) == 0) && ((csr_value.pmp14cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp14cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp14cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp14cfg;

pmp15cfg = if ((xlen() == 64) && (CSR[pmpcfg2].pmp15cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp15cfg & 0x1) == 0) && ((csr_value.pmp15cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp15cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp15cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg2].pmp15cfg;

```

C.123. pmpcfg4

PMP Configuration Register 4

PMP entry configuration

C.123.1. Attributes

CSR Address	0x3a4
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.123.2. Format

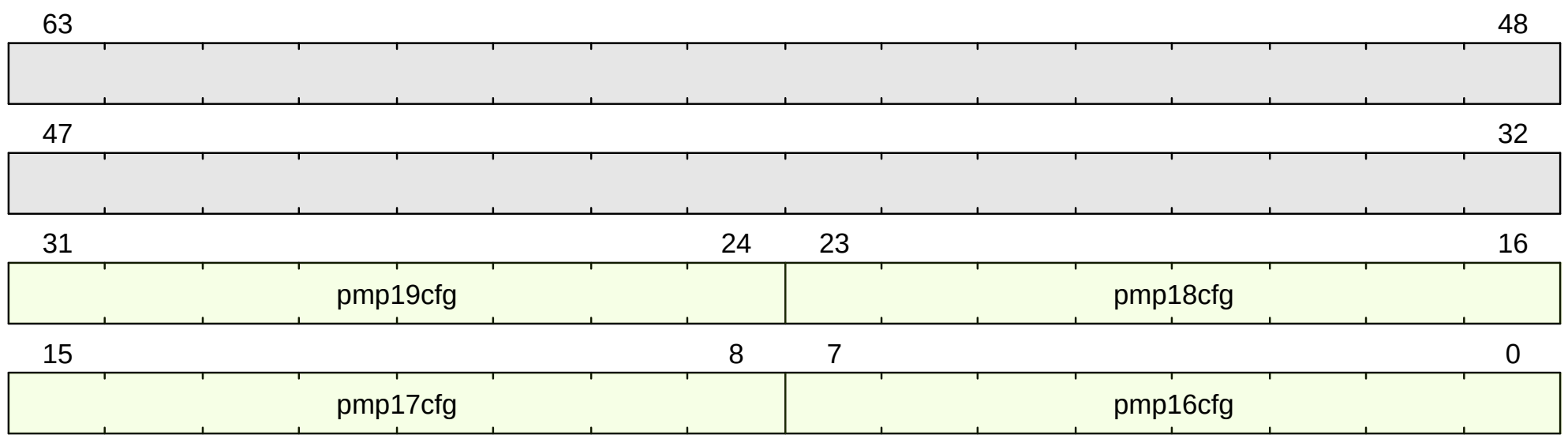


Figure 123. pmpcfg4 format

C.123.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg4.pmp16cfg	7:0	RW-R	0
		RO	
pmpcfg4.pmp17cfg	15:8	RW-R	0
		RO	
pmpcfg4.pmp18cfg	23:16	RW-R	0
		RO	
pmpcfg4.pmp19cfg	31:24	RW-R	0
		RO	
pmpcfg4.pmp20cfg	39:32	RW-R	0
		RO	
pmpcfg4.pmp21cfg	47:40	RW-R	0
		RO	
pmpcfg4.pmp22cfg	55:48	RW-R	0
		RO	
pmpcfg4.pmp23cfg	63:56	RW-R	0
		RO	

C.123.4. Fields

[pmpcfg4.pmp16cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 16

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp17cfg Field

Location:

15:8

Description:

PMP configuration for entry 17

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp18cfg Field

Location:

23:16

Description:

PMP configuration for entry 18

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp19cfg Field

Location:

31:24

Description:

PMP configuration for entry 19

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp20cfg Field



pmp20cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 20

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 38:37 ! *Reserved* Writes shall be ignored.
h! A ! 36:35
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp21cfg Field



pmp21cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 21

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 46:45 ! *Reserved* Writes shall be ignored.
h! A ! 44:43
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp22cfg Field



pmp22cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 22

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg4.pmp23cfg Field



pmp23cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 23

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.123.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp16cfg = if ((CSR[pmpcfg4].pmp16cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp16cfg & 0x1) == 0) && ((csr_value.pmp16cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp16cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp16cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp16cfg;

pmp17cfg = if ((CSR[pmpcfg4].pmp17cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp17cfg & 0x1) == 0) && ((csr_value.pmp17cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp17cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp17cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp17cfg;

pmp18cfg = if ((CSR[pmpcfg4].pmp18cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp18cfg & 0x1) == 0) && ((csr_value.pmp18cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp18cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp18cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp18cfg;

pmp19cfg = if ((CSR[pmpcfg4].pmp19cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp19cfg & 0x1) == 0) && ((csr_value.pmp19cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp19cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp19cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp19cfg;

pmp20cfg = if ((CSR[pmpcfg4].pmp20cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp20cfg & 0x1) == 0) && ((csr_value.pmp20cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp20cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp20cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp20cfg;

pmp21cfg = if ((xlen() == 64) && (CSR[pmpcfg4].pmp21cfg & 0x80) == 0) {
    # entry is not locked
```

```

    if (!(((csr_value.pmp21cfg & 0x1) == 0) && ((csr_value.pmp21cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp21cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp21cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp21cfg;

pmp22cfg = if ((xlen() == 64) && (CSR[pmpcfg4].pmp22cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp22cfg & 0x1) == 0) && ((csr_value.pmp22cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp22cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp22cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp22cfg;

pmp23cfg = if ((xlen() == 64) && (CSR[pmpcfg4].pmp23cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp23cfg & 0x1) == 0) && ((csr_value.pmp23cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp23cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp23cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg4].pmp23cfg;

```


C.124. pmpcfg6

PMP Configuration Register 6

PMP entry configuration

C.124.1. Attributes

CSR Address	0x3a6
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.124.2. Format

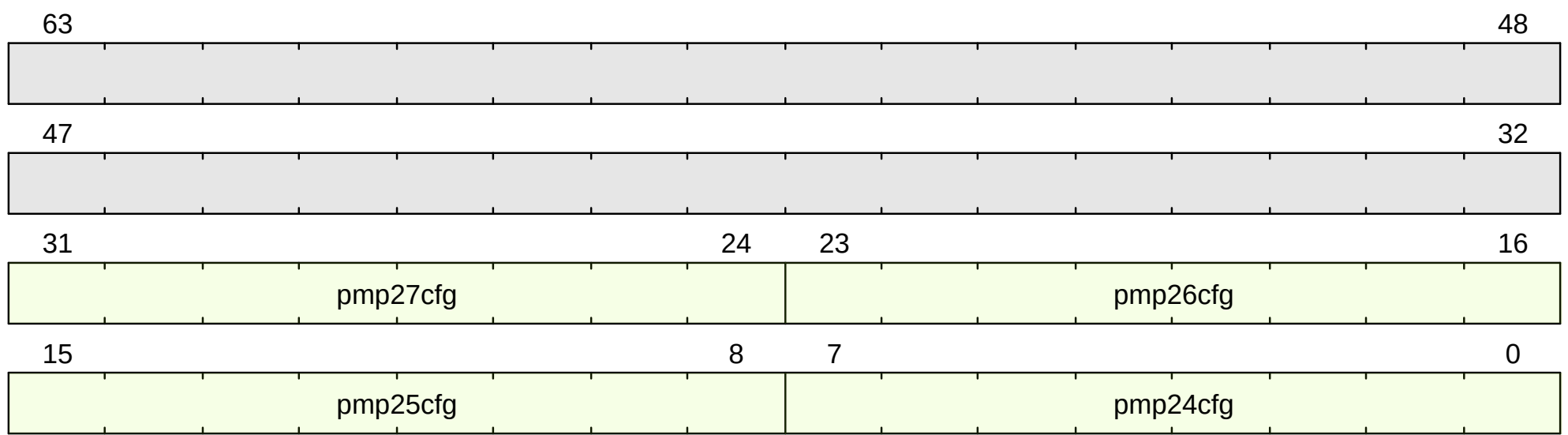


Figure 124. pmpcfg6 format

C.124.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg6.pmp24cfg	7:0	RW-R	0
		RO	
pmpcfg6.pmp25cfg	15:8	RW-R	0
		RO	
pmpcfg6.pmp26cfg	23:16	RW-R	0
		RO	
pmpcfg6.pmp27cfg	31:24	RW-R	0
		RO	
pmpcfg6.pmp28cfg	39:32	RW-R	0
		RO	
pmpcfg6.pmp29cfg	47:40	RW-R	0
		RO	
pmpcfg6.pmp30cfg	55:48	RW-R	0
		RO	
pmpcfg6.pmp31cfg	63:56	RW-R	0
		RO	

C.124.4. Fields

[pmpcfg6.pmp24cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 24

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 6:5 ! *Reserved* Writes shall be ignored.
h! A ! 4:3
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp25cfg Field

Location:

15:8

Description:

PMP configuration for entry 25

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 14:13 ! *Reserved* Writes shall be ignored.
h! A ! 12:11
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp26cfg Field

Location:

23:16

Description:

PMP configuration for entry 26

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp27cfg Field

Location:

31:24

Description:

PMP configuration for entry 27

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp28cfg Field



pmp28cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 28

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 38:37 ! *Reserved* Writes shall be ignored.
h! A ! 36:35
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp29cfg Field



pmp29cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 29

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 46:45 ! *Reserved* Writes shall be ignored.
h! A ! 44:43
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp30cfg Field



pmp30cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 30

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg6.pmp31cfg Field



pmp31cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 31

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.124.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp24cfg = if ((CSR[pmpcfg6].pmp24cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp24cfg & 0x1) == 0) && ((csr_value.pmp24cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp24cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp24cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp24cfg;

pmp25cfg = if ((CSR[pmpcfg6].pmp25cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp25cfg & 0x1) == 0) && ((csr_value.pmp25cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp25cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp25cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp25cfg;

pmp26cfg = if ((CSR[pmpcfg6].pmp26cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp26cfg & 0x1) == 0) && ((csr_value.pmp26cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp26cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp26cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp26cfg;

pmp27cfg = if ((CSR[pmpcfg6].pmp27cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp27cfg & 0x1) == 0) && ((csr_value.pmp27cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp27cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp27cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp27cfg;

pmp28cfg = if ((CSR[pmpcfg6].pmp28cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp28cfg & 0x1) == 0) && ((csr_value.pmp28cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp28cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp28cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp28cfg;

pmp29cfg = if ((xlen() == 64) && (CSR[pmpcfg6].pmp29cfg & 0x80) == 0) {
    # entry is not locked
```



```

    if (!(((csr_value.pmp29cfg & 0x1) == 0) && ((csr_value.pmp29cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp29cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp29cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp29cfg;

pmp30cfg = if ((xlen() == 64) && (CSR[pmpcfg6].pmp30cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp30cfg & 0x1) == 0) && ((csr_value.pmp30cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp30cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp30cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp30cfg;

pmp31cfg = if ((xlen() == 64) && (CSR[pmpcfg6].pmp31cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp31cfg & 0x1) == 0) && ((csr_value.pmp31cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp31cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp31cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg6].pmp31cfg;

```

C.125. pmpcfg8

PMP Configuration Register 8

PMP entry configuration

C.125.1. Attributes

CSR Address	0x3a8
Defining extension	Smpmp
Length	64-bit
Privilege Mode	M

C.125.2. Format

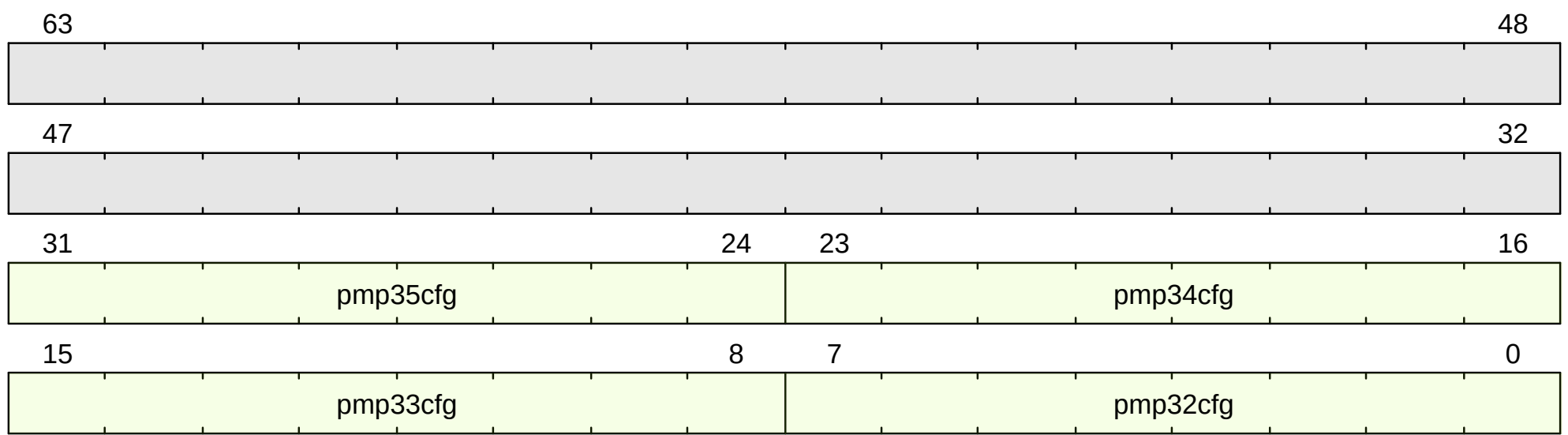


Figure 125. pmpcfg8 format

C.125.3. Field Summary

Name	Location	Type	Reset Value
pmpcfg8.pmp32cfg	7:0	RW-R	0
		RO	
pmpcfg8.pmp33cfg	15:8	RW-R	0
		RO	
pmpcfg8.pmp34cfg	23:16	RW-R	0
		RO	
pmpcfg8.pmp35cfg	31:24	RW-R	0
		RO	
pmpcfg8.pmp36cfg	39:32	RW-R	0
		RO	
pmpcfg8.pmp37cfg	47:40	RW-R	0
		RO	
pmpcfg8.pmp38cfg	55:48	RW-R	0
		RO	
pmpcfg8.pmp39cfg	63:56	RW-R	0
		RO	

C.125.4. Fields

[pmpcfg8.pmp32cfg](#) Field

Location:

7:0

Description:

PMP configuration for entry 32

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 7 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 6:5 ! *Reserved* Writes shall be ignored.

h! A ! 4:3

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 2 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 1 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 0 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp33cfg Field

Location:

15:8

Description:

PMP configuration for entry 33

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 15 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 14:13 ! *Reserved* Writes shall be ignored.

h! A ! 12:11

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 10 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 9 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 8 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp34cfg Field

Location:

23:16

Description:

PMP configuration for entry 34

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 23 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 22:21 ! *Reserved* Writes shall be ignored.
h! A ! 20:19
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 18 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 17 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 16 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp35cfg Field

Location:

31:24

Description:

PMP configuration for entry 35

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 31 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.

h! - ! 30:29 ! *Reserved* Writes shall be ignored.

h! A ! 28:27

a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 26 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.

h! W ! 25 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 24 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.

!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp36cfg Field



pmp36cfg is only defined in RV64 (**CSR[misa].MXL == 1**)

Location:

39:32

Description:

PMP configuration for entry 36

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 39 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 38:37 ! *Reserved* Writes shall be ignored.
h! A ! 36:35
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 34 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 33 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 32 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp37cfg Field



pmp37cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

47:40

Description:

PMP configuration for entry 37

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 47 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 46:45 ! *Reserved* Writes shall be ignored.
h! A ! 44:43
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 42 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 41 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 40 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp38cfg Field



pmp38cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

55:48

Description:

PMP configuration for entry 38

The bits are as follows:

[separator="!",%autowidth]
!===
! Name ! Location ! Description

h! L ! 55 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 54:53 ! *Reserved* Writes shall be ignored.
h! A ! 52:51
a! Address matching mode. One of:

- [when="PMP_GRANULARITY < 2"]
- **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NA4** (2) - Naturally aligned four-byte region
 - **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
 - **OFF** (0) - Null region (disabled)
 - **TOR** (1) - Top of range
 - **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]
Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 50 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 49 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.

h! R ! 48 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

pmpcfg8.pmp39cfg Field



pmp39cfg is only defined in RV64 (CSR[misa].MXL == 1)

Location:

63:56

Description:

PMP configuration for entry 39

The bits are as follows:

[separator="!",%autowidth]

!===

! Name ! Location ! Description

h! L ! 63 ! Locks the entry from further modification. Additionally, when set, PMP checks also apply to M-mode for the entry.
h! - ! 62:61 ! *Reserved* Writes shall be ignored.
h! A ! 60:59
a! Address matching mode. One of:

[when="PMP_GRANULARITY < 2"]

- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NA4** (2) - Naturally aligned four-byte region
- **NAPOT** (3) - Naturally aligned power of two
+ [when="PMP_GRANULARITY >= 2"]
- **OFF** (0) - Null region (disabled)
- **TOR** (1) - Top of range
- **NAPOT** (3) - Naturally aligned power of two

[when="PMP_GRANULARITY >= 2"]

Naturally aligned four-byte region, **NA4** (2), is not valid (not needed when the PMP granularity is larger than 4 bytes).

h! X ! 58 ! When clear, instruction fetches cause an **Access Fault** for the matching region and privilege mode.
h! W ! 57 ! When clear, stores and AMOs cause an **Access Fault** for the matching region and privilege mode.
h! R ! 56 ! When clear, loads cause an **Access Fault** for the matching region and privilege mode.
!===

The combination of R = 0, W = 1 is reserved.

Type:

RW-R

RO

Reset value:

0

C.125.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (e.g., through [csrrw](#)), the following determines the written value:

```
pmp32cfg = if ((CSR[pmpcfg8].pmp32cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp32cfg & 0x1) == 0) && ((csr_value.pmp32cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp32cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp32cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp32cfg;

pmp33cfg = if ((CSR[pmpcfg8].pmp33cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp33cfg & 0x1) == 0) && ((csr_value.pmp33cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp33cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp33cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp33cfg;

pmp34cfg = if ((CSR[pmpcfg8].pmp34cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp34cfg & 0x1) == 0) && ((csr_value.pmp34cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp34cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp34cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp34cfg;

pmp35cfg = if ((CSR[pmpcfg8].pmp35cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp35cfg & 0x1) == 0) && ((csr_value.pmp35cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp35cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp35cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp35cfg;

pmp36cfg = if ((CSR[pmpcfg8].pmp36cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp36cfg & 0x1) == 0) && ((csr_value.pmp36cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp36cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp36cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp36cfg;

pmp37cfg = if ((xlen() == 64) && (CSR[pmpcfg8].pmp37cfg & 0x80) == 0) {
    # entry is not locked
```

```

if (!(((csr_value.pmp37cfg & 0x1) == 0) && ((csr_value.pmp37cfg & 0x2) == 0x2))) {
    # not R = 0, W =1, which is reserved
    if ((PMP_GRANULARITY < 2) ||
        ((csr_value.pmp37cfg & 0x18) != 0x10)) {
        # NA4 is not allowed when PMP granularity is larger than 4 bytes
        return csr_value.pmp37cfg;
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp37cfg;

pmp38cfg = if ((xlen() == 64) && (CSR[pmpcfg8].pmp38cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp38cfg & 0x1) == 0) && ((csr_value.pmp38cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp38cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp38cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp38cfg;

pmp39cfg = if ((xlen() == 64) && (CSR[pmpcfg8].pmp39cfg & 0x80) == 0) {
    # entry is not locked
    if (!(((csr_value.pmp39cfg & 0x1) == 0) && ((csr_value.pmp39cfg & 0x2) == 0x2))) {
        # not R = 0, W =1, which is reserved
        if ((PMP_GRANULARITY < 2) ||
            ((csr_value.pmp39cfg & 0x18) != 0x10)) {
            # NA4 is not allowed when PMP granularity is larger than 4 bytes
            return csr_value.pmp39cfg;
        }
    }
}
# fall through: keep old value
return CSR[pmpcfg8].pmp39cfg;

```

C.126. satp

Supervisor Address Translation and Protection

Controls the translation mode in (H)S-mode and U-mode, and holds the current ASID and page table base pointer.

C.126.1. Attributes

CSR Address	0x180
Defining extension	S
Length	* 32 when CSR[mstatus].SXL == 0 * 64 when CSR[mstatus].SXL == 1
Privilege Mode	S

C.126.2. Format

This CSR format changes dynamically with XLEN.

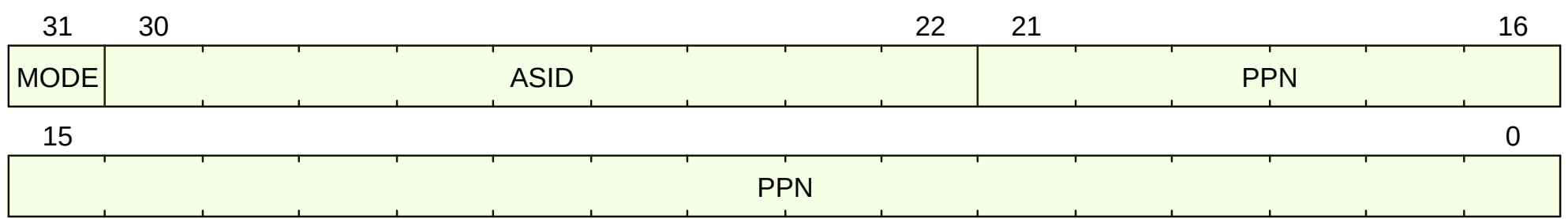


Figure 126. satp Format when CSR[mstatus].SXL == 0

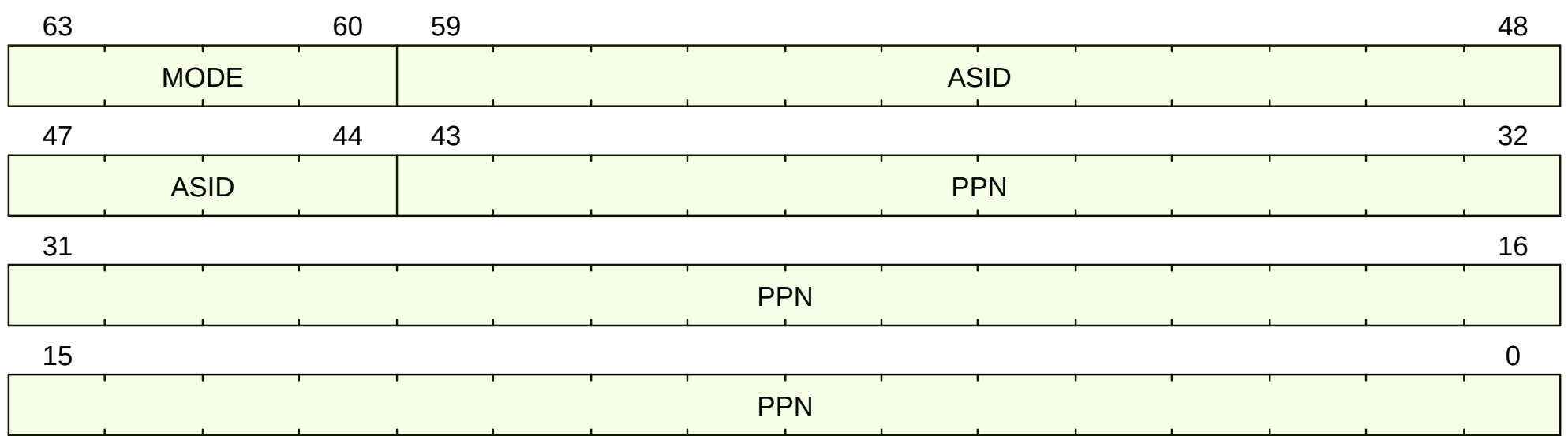


Figure 127. satp Format when CSR[mstatus].SXL == 1

C.126.3. Field Summary

Na me	Location	Type	Reset Value
satp.MODE	31	RW-R	0
satp.ASID	63:60		
	30:22	RW-R	UNDEFINED_LEGAL
	59:44		
satp.PPN	21:0	RW-R	UNDEFINED_LEGAL
	43:0		

C.126.4. Fields

satp.MODE Field

Location:

- 31 when CSR[mstatus].SXL == 0
- 63:60 when CSR[mstatus].SXL == 1

Description:

Translation Mode

Controls the current translation mode according to the table below.

```
[separator="!",%autowidth]
!===
! Value ! Name ! Description

! 0 ! Bare a! No translation → virtual address == physical address
<%- if ext?(:Sv39) -%>
! 8 ! Sv39 ! 39-bit virtual address translation
<%- end -%>
<%- if ext?(:Sv48) -%>
! 9 ! Sv48 ! 48-bit virtual address translation
<%- end -%>
<%- if ext?(:Sv57) -%>
! 10 ! Sv57 ! 57-bit virtual address translation
<%- end -%>
!===
```

Any other value shall be ignored on a write.

Type:

RW-R

Reset value:

0

satp.ASID Field

Location:

- 30:22 when CSR[mstatus].SXL == 0
- 59:44 when CSR[mstatus].SXL == 1

Description:

Address Space ID

Type:

RW-R

Reset value:

UNDEFINED_LEGAL

satp.PPN Field

Location:

- 21:0 when CSR[mstatus].SXL == 0
- 43:0 when CSR[mstatus].SXL == 1

Description:

Physical Page Number

The physical address of the active root page table is PPN << 12.

Can only hold values that correspond to a valid page table base, which will be implementation-dependent.

Type:

RW-R

Reset value:

UNDEFINED_LEGAL

C.126.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```

MODE = if (SATP_MODE_BARE && (csr_value.MODE == 0)) {
    # In Bare, ASID and PPN must be zero, else the entire write is ignored
    if (csr_value.ASID == 0 && csr_value.PPN == 0) {
        if (CSR[satp].MODE != 0) {
            # changes *to* Bare mode take effect immediately without needing sfence.vma
            # thus, an implicit sfence.vma occurs now
            VmaOrderType order_type;
            order_type.global = true;
            order_pgtbl_writes_before_vmafence(order_type);

            invalidate_translations(order_type);

            order_pgtbl_reads_after_vmafence(order_type);
        }
        return csr_value.MODE;
    } else {
        return UNDEFINED_LEGAL_DETERMINISTIC;
    }
}
else if (implemented?(ExtensionName::Sv32) && csr_value.MODE == 1) {
    if (CSR[satp].MODE == 0) {
        # changes *from* Bare mode take effect immediately without needing sfence.vma
        # thus, an implicit sfence.vma occurs now
        VmaOrderType order_type;
        order_type.global = true;
        order_pgtbl_writes_before_vmafence(order_type);

        invalidate_translations(order_type);

        order_pgtbl_reads_after_vmafence(order_type);
    }
    return csr_value.MODE;
} else if (implemented?(ExtensionName::Sv39) && csr_value.MODE == 8) {
    if (CSR[satp].MODE == 0) {
        # changes *from* Bare mode take effect immediately without needing sfence.vma
        # thus, an implicit sfence.vma occurs now
        VmaOrderType order_type;
        order_type.global = true;
        order_pgtbl_writes_before_vmafence(order_type);

        invalidate_translations(order_type);

        order_pgtbl_reads_after_vmafence(order_type);
    }
    return csr_value.MODE;
}
else if (implemented?(ExtensionName::Sv48) && csr_value.MODE == 9) {
    if (CSR[satp].MODE == 0) {
        # changes *from* Bare mode take effect immediately without needing sfence.vma
        # thus, an implicit sfence.vma occurs now
        VmaOrderType order_type;
        order_type.global = true;
        order_pgtbl_writes_before_vmafence(order_type);

        invalidate_translations(order_type);

        order_pgtbl_reads_after_vmafence(order_type);
    }

    return csr_value.MODE;
}
else if (implemented?(ExtensionName::Sv57) && csr_value.MODE == 10) {
    if (CSR[satp].MODE == 0) {
        # changes *from* Bare mode take effect immediately without needing sfence.vma
        # thus, an implicit sfence.vma occurs now
        VmaOrderType order_type;
        order_type.global = true;
        order_pgtbl_writes_before_vmafence(order_type);

        invalidate_translations(order_type);

        order_pgtbl_reads_after_vmafence(order_type);
    }
}

```

```

    return csr_value.MODE;
}
else {
    return UNDEFINED_LEGAL_DETERMINISTIC;
}

ASID = if (csr_value.MODE == 0) {
    # when MODE == Bare, PPN and ASID must be zero
    if (csr_value.ASID == 0 && csr_value.PPN == 0) {
        return csr_value.ASID;
    } else {
        return UNDEFINED_LEGAL_DETERMINISTIC;
    }
} else {
    XReg shamt = (xlen() == 32 || (CSR[mstatus].SXL == $bits(XRegWidth::XLEN32))) ? 9 : 16;
    XReg all_ones = ((MXLEN'1 << shamt) - 1);
    XReg largest_allowed_asid = (MXLEN'1 << shamt) - 1;

    if (csr_value.ASID == all_ones) {
        # the specification states that if all 1's are written to the ASID field, then
        # you must return the largest asid
        return largest_allowed_asid;
    } else if (csr_value.ASID > largest_allowed_asid) {
        # ... but is silent on what happens on any other illegal value
        return UNDEFINED_LEGAL_DETERMINISTIC;
    } else {
        # unrestricted
        return csr_value.ASID;
    }
}

PPN = if (csr_value.MODE == 0) {
    # when MODE == Bare, PPN and ASID must be zero
    if (csr_value.ASID == 0 && csr_value.PPN == 0) {
        return csr_value.PPN;
    } else {
        return UNDEFINED_LEGAL_DETERMINISTIC;
    }
} else {
    # unrestricted
    return csr_value.PPN;
}

```


C.127. scause

Supervisor Cause

Reports the cause of the latest exception.

C.127.1. Attributes

CSR Address	0x142
Defining extension	S
Length	* 32 when CSR[mstatus].SXL == 0 * 64 when CSR[mstatus].SXL == 1
Privilege Mode	S

C.127.2. Format

This CSR format changes dynamically with XLEN.

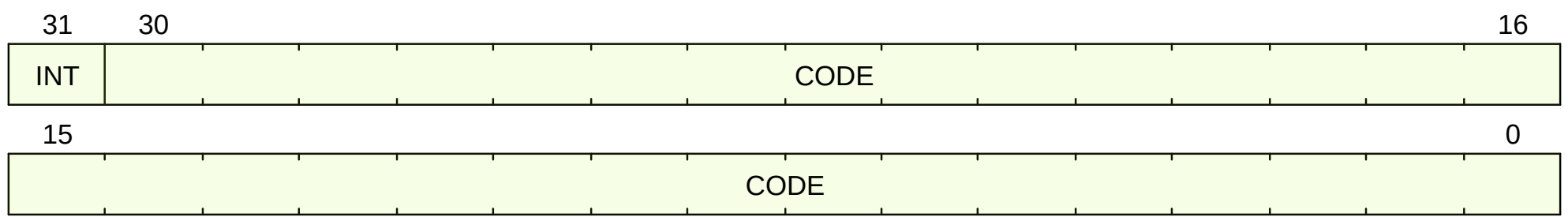


Figure 128. scause Format when CSR[mstatus].SXL == 0

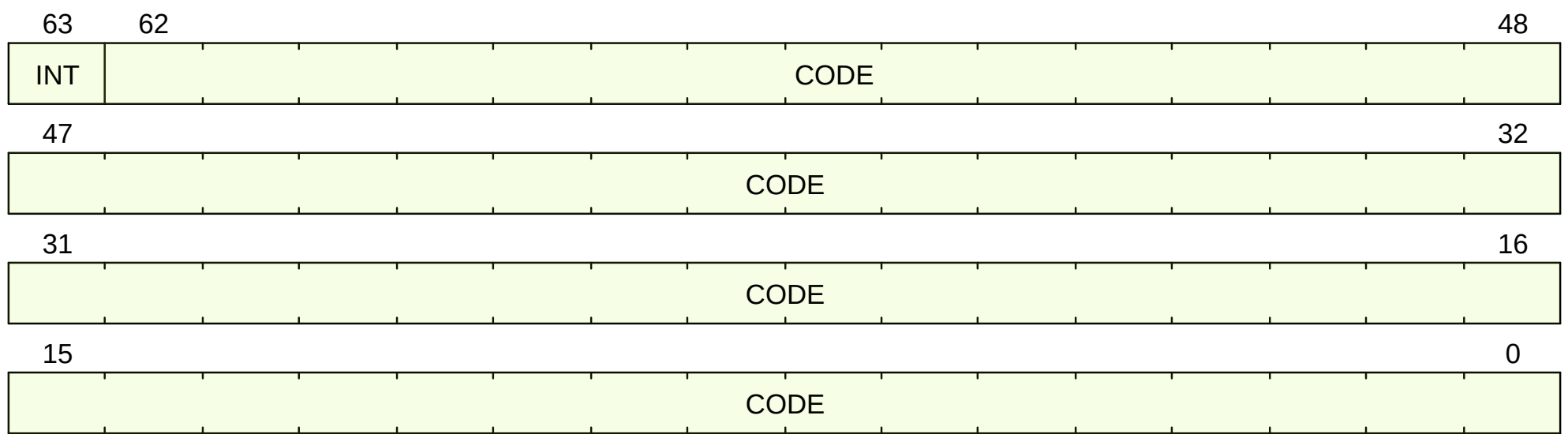


Figure 129. scause Format when CSR[mstatus].SXL == 1

C.127.3. Field Summary

Nam e	Location	Type	Reset Value
scause.INT	31 63	RW-RH	UNDEFINED_LEGAL
scause.CODE	30:0 62:0	RW-RH	UNDEFINED_LEGAL

C.127.4. Fields

[scause.INT](#) Field

Location:

- 31 when CSR[mstatus].SXL == 0
- 63 when CSR[mstatus].SXL == 1

Description:

Written by hardware when a trap is taken into S-mode.

When set, the last exception was caused by an asynchronous Interrupt.

[scause.INT](#) is writable.

```
[when,"TRAP_ON_ILLEGAL_WLRL == true"]
If scause is written with an undefined cause (combination of scause.INT and scause.CODE), an Illegal Instruction exception occurs.
```

```
[when,"TRAP_ON_ILLEGAL_WLRL == false"]
If scause is written with an undefined cause (combination of scause.INT and scause.CODE), neither scause.INT nor scause.CODE are modified.
```

Type:

RW-RH

Reset value:

UNDEFINED_LEGAL

`scause.CODE` Field

Location:

- 30:0 when CSR[mstatus].SXL == 0
- 62:0 when CSR[mstatus].SXL == 1

Description:

Written by hardware when a trap is taken into S-mode.

Holds the interrupt or exception code for the last taken trap.

`scause.CODE` is writable.

```
[when,"TRAP_ON_ILLEGAL_WLRL == true"]
If scause is written with an undefined cause (combination of scause.INT and scause.CODE), an Illegal Instruction exception occurs.
```

```
[when,"TRAP_ON_ILLEGAL_WLRL == false"]
If scause is written with an undefined cause (combination of scause.INT and scause.CODE), neither scause.INT nor scause.CODE are modified.
```

Valid interrupt codes are:

```
[separator="!"]
!===
<%- implemented_interrupt_codes.sort_by { |code| code.num }.each do |code| -%>
! <%= code.num %> ! <%= code.name %>
<%- end -%>
!===
```

Valid exception codes are:

```
[separator="!"]
!===
<%- implemented_exception_codes.sort_by { |code| code.num }.each do |code| -%>
! <%= code.num %> ! <%= code.name %>
<%- end -%>
!===
```

Type:

RW-RH

Reset value:

UNDEFINED_LEGAL

C.127.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through `csrrw`), the following determines the written value:

```
INT = # the write only holds if the INT/CODE combination is valid
# otherwise, the old value is retained
if (csr_value.INT == 1) {
  if (valid_interrupt_code?(csr_value.CODE)) {
    return 1;
  }
}
```



```

    return ILLEGAL_WLRL;
} else {
    if (valid_exception_code?(csr_value.CODE)) {
        return 1;
    }
    return ILLEGAL_WLRL;
}

CODE = # the write only holds if the INT/CODE combination is valid
# otherwise, the old value is retained
if (csr_value.INT == 1) {
    if (valid_interrupt_code?(csr_value.CODE)) {
        return csr_value.CODE;
    }
    return ILLEGAL_WLRL;
} else {
    if (valid_exception_code?(csr_value.CODE)) {
        return csr_value.CODE;
    }
    return ILLEGAL_WLRL;
}

```

C.128. scounteren

Supervisor Counter Enable

Delegates control of the hardware performance-monitoring counters to U-mode

C.128.1. Attributes

CSR Address	0x106
Defining extension	S
Length	32-bit
Privilege Mode	S

C.128.2. Format

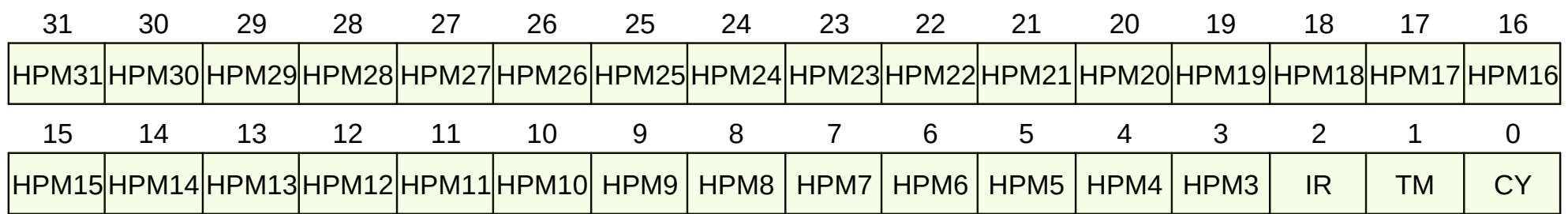


Figure 130. scounteren format

C.128.3. Field Summary

Name	Location	Type	Reset Value
scount eren.CY	0	RW	UNDEFINED_LEGAL
		RO	
scount eren.TM	1	RW	UNDEFINED_LEGAL
		RO	
scount eren.IR	2	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM3	3	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM4	4	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM5	5	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM6	6	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM7	7	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM8	8	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM9	9	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM10	10	RW	UNDEFINED_LEGAL
		RO	
scount eren.HPM11	11	RW	UNDEFINED_LEGAL
		RO	

Name	Location	Type	Reset Value
scount eren.H PM12	12	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM13	13	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM14	14	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM15	15	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM16	16	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM17	17	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM18	18	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM19	19	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM20	20	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM21	21	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM22	22	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM23	23	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM24	24	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM25	25	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM26	26	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM27	27	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM28	28	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM29	29	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM30	30	RW	UNDEFINED_LEGAL
		RO	
scount eren.H PM31	31	RW	UNDEFINED_LEGAL
		RO	

C.128.4. Fields

scounteren.CY Field

Location:

0

Description:

When both [scounteren.CY](#) and [mcounteren.CY](#) are set, the [cycle](#) CSR (an alias of [mcycle](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.CY](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.TM Field

Location:

1

Description:

When both [scounteren.TM](#) and [mcounteren.TM](#) are set, the [time](#) CSR (an alias of [mtime](#) memory-mapped CSR) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.TM](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.IR Field

Location:

2

Description:

When both [scounteren.IR](#) and [mcounteren.IR](#) are set, the [instret](#) CSR (an alias of memory-mapped [minstret](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.IR](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.HPM3 Field

Location:

3

Description:

When both [scounteren.HPM3](#) and [mcounteren.HPM3](#) are set, the [hpmcounter3](#) CSR (an alias of [mhpmcounter3](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM3](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.HPM4 Field

Location:

4

Description:

When both [scounteren.HPM4](#) and [mcounteren.HPM4](#) are set, the [hpmcounter4](#) CSR (an alias of [mhpmcounter4](#)) is accessible to U-mode

<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM4](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.HPM5 Field

Location:

5

Description:

When both [scounteren.HPM5](#) and [mcounteren.HPM5](#) are set, the [hpmcounter5](#) CSR (an alias of [mhpmcounter5](#)) is accessible to U-mode

<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM5](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.HPM6 Field

Location:

6

Description:

When both [scounteren.HPM6](#) and [mcounteren.HPM6](#) are set, the [hpmcounter6](#) CSR (an alias of [mhpmcounter6](#)) is accessible to U-mode

<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM6](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

scounteren.HPM7 Field

Location:

7

Description:

When both [scounteren.HPM7](#) and [mcounteren.HPM7](#) are set, the [hpmcounter7](#) CSR (an alias of [mhpmcounter7](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM7](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM8](#) Field

Location:

8

Description:

When both [scounteren.HPM8](#) and [mcounteren.HPM8](#) are set, the [hpmcounter8](#) CSR (an alias of [mhpmcounter8](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM8](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM9](#) Field

Location:

9

Description:

When both [scounteren.HPM9](#) and [mcounteren.HPM9](#) are set, the [hpmcounter9](#) CSR (an alias of [mhpmcounter9](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM9](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM10](#) Field

Location:

10

Description:

When both [scounteren.HPM10](#) and [mcounteren.HPM10](#) are set, the [hpmcounter10](#) CSR (an alias of [mhpmcounter10](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM10](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM11 Field

Location:
11

Description:
When both [scounteren.HPM11](#) and [mcounteren.HPM11](#) are set, the [hpmcounter11](#) CSR (an alias of [mhpmcounter11](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM11](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM12 Field

Location:
12

Description:
When both [scounteren.HPM12](#) and [mcounteren.HPM12](#) are set, the [hpmcounter12](#) CSR (an alias of [mhpmcounter12](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM12](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM13 Field

Location:
13

Description:
When both [scounteren.HPM13](#) and [mcounteren.HPM13](#) are set, the [hpmcounter13](#) CSR (an alias of [mhpmcounter13](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM13](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM14 Field

Location:
14

Description:

When both [scounteren.HPM14](#) and [mcounteren.HPM14](#) are set, the [hpmcounter14](#) CSR (an alias of [mhpmcounter14](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM14](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM15](#) Field

Location:

15

Description:

When both [scounteren.HPM15](#) and [mcounteren.HPM15](#) are set, the [hpmcounter15](#) CSR (an alias of [mhpmcounter15](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM15](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM16](#) Field

Location:

16

Description:

When both [scounteren.HPM16](#) and [mcounteren.HPM16](#) are set, the [hpmcounter16](#) CSR (an alias of [mhpmcounter16](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM16](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM17](#) Field

Location:

17

Description:

When both [scounteren.HPM17](#) and [mcounteren.HPM17](#) are set, the [hpmcounter17](#) CSR (an alias of [mhpmcounter17](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM17](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM18 Field

Location:
18

Description:
When both [scounteren.HPM18](#) and [mcounteren.HPM18](#) are set, the [hpmcounter18](#) CSR (an alias of [mhpmcounter18](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM18](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM19 Field

Location:
19

Description:
When both [scounteren.HPM19](#) and [mcounteren.HPM19](#) are set, the [hpmcounter19](#) CSR (an alias of [mhpmcounter19](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM19](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM20 Field

Location:
20

Description:
When both [scounteren.HPM20](#) and [mcounteren.HPM20](#) are set, the [hpmcounter20](#) CSR (an alias of [mhpmcounter20](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM20](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM21 Field

Location:
21

Description:

When both [scounteren.HPM21](#) and [mcounteren.HPM21](#) are set, the [hpmcounter21](#) CSR (an alias of [mhpmcounter21](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM21](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM22](#) Field

Location:

22

Description:

When both [scounteren.HPM22](#) and [mcounteren.HPM22](#) are set, the [hpmcounter22](#) CSR (an alias of [mhpmcounter22](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM22](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM23](#) Field

Location:

23

Description:

When both [scounteren.HPM23](#) and [mcounteren.HPM23](#) are set, the [hpmcounter23](#) CSR (an alias of [mhpmcounter23](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM23](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM24](#) Field

Location:

24

Description:

When both [scounteren.HPM24](#) and [mcounteren.HPM24](#) are set, the [hpmcounter24](#) CSR (an alias of [mhpmcounter24](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM24](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM25 Field

Location:
25

Description:
When both [scounteren.HPM25](#) and [mcounteren.HPM25](#) are set, the [hpmcounter25](#) CSR (an alias of [mhpmcounter25](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM25](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM26 Field

Location:
26

Description:
When both [scounteren.HPM26](#) and [mcounteren.HPM26](#) are set, the [hpmcounter26](#) CSR (an alias of [mhpmcounter26](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM26](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM27 Field

Location:
27

Description:
When both [scounteren.HPM27](#) and [mcounteren.HPM27](#) are set, the [hpmcounter27](#) CSR (an alias of [mhpmcounter27](#)) is accessible to U-mode
<% if ext?:(H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM27](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

scounteren.HPM28 Field

Location:
28

Description:

When both [scounteren.HPM28](#) and [mcounteren.HPM28](#) are set, the [hpmcounter28](#) CSR (an alias of [mhpmcounter28](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM28](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM29](#) Field

Location:

29

Description:

When both [scounteren.HPM29](#) and [mcounteren.HPM29](#) are set, the [hpmcounter29](#) CSR (an alias of [mhpmcounter29](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM29](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM30](#) Field

Location:

30

Description:

When both [scounteren.HPM30](#) and [mcounteren.HPM30](#) are set, the [hpmcounter30](#) CSR (an alias of [mhpmcounter30](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM30](#))<% end %>.

Type:

RW

RO

Reset value:

UNDEFINED_LEGAL

[scounteren.HPM31](#) Field

Location:

31

Description:

When both [scounteren.HPM31](#) and [mcounteren.HPM31](#) are set, the [hpmcounter31](#) CSR (an alias of [mhpmcounter31](#)) is accessible to U-mode
<% if ext?(:H) %>(delegation to VS/VU mode is further handled by [hcounteren.HPM31](#))<% end %>.

Type:

RW

RO

Reset value:
UNDEFINED_LEGAL

C.129. scountovf

Supervisor Count Overflow

A 32-bit read-only register that contains shadow copies of the OF bits in the 29 `mhpmevent` CSRs (`mhpmevent3` - `mhpmevent31`) — where `scountovf` bit X corresponds to `mhpmeventX`.

This register enables supervisor-level overflow interrupt handler software to quickly and easily determine which counter(s) have overflowed without needing to make an execution environment call up to M-mode.

Read access to bit X is subject to the same `mcouteren` (or `mcouteren` and `hcouteren`) CSRs that mediate access to the `hpmcounter` CSRs by S-mode (or VS-mode).

In M-mode, `scountovf` bit X is always readable. In S/HS-mode, `scountovf` bit X is readable when `mcouteren` bit X is set, and otherwise reads as zero. Similarly, in VS-mode, it is readable when both `mcouteren` and `hcouteren` bit X are set.

C.129.1. Attributes

CSR Address	0xda0
Defining extension	<code>Sscofpmf</code>
Length	32-bit
Privilege Mode	S

C.129.2. Format

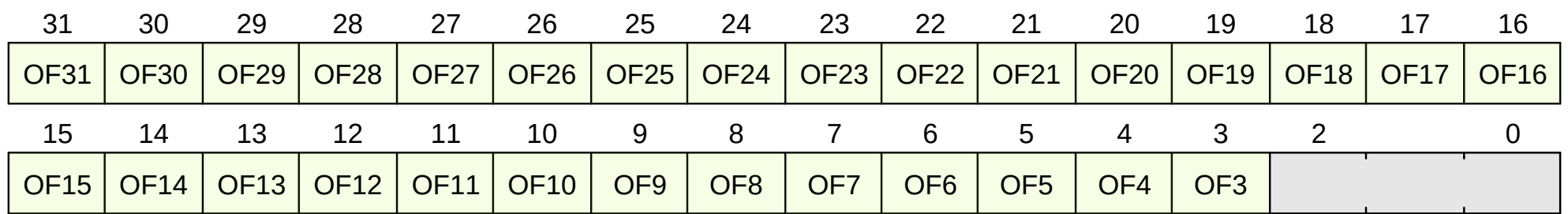


Figure 131. `scountovf` format

C.129.3. Field Summary

Name	Location	Type	Reset Value
<code>scountovf.OF3</code>	3	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF4</code>	4	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF5</code>	5	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF6</code>	6	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF7</code>	7	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF8</code>	8	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF9</code>	9	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF10</code>	10	RO RO-H	UNDEFINED_LEGAL
<code>scountovf.OF11</code>	11	RO RO-H	UNDEFINED_LEGAL

Name	Location	Type	Reset Value
scoun tovf.O F12	12	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F13	13	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F14	14	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F15	15	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F16	16	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F17	17	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F18	18	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F19	19	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F20	20	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F21	21	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F22	22	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F23	23	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F24	24	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F25	25	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F26	26	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F27	27	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F28	28	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F29	29	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F30	30	RO	UNDEFINED_LEGAL
		RO-H	
scoun tovf.O F31	31	RO	UNDEFINED_LEGAL
		RO-H	

C.129.4. Fields

scountovf.OF3 Field

Location:

3

Description:

[when="HPM_COUNTER_EN[3] == true"]
Shadow copy of mhpmevent3 overflow (OF) bit.

[when="HPM_COUNTER_EN[3] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF4 Field

Location:

4

Description:

[when="HPM_COUNTER_EN[4] == true"]
Shadow copy of mhpmevent4 overflow (OF) bit.

[when="HPM_COUNTER_EN[4] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF5 Field

Location:

5

Description:

[when="HPM_COUNTER_EN[5] == true"]
Shadow copy of mhpmevent5 overflow (OF) bit.

[when="HPM_COUNTER_EN[5] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF6 Field

Location:

6

Description:

[when="HPM_COUNTER_EN[6] == true"]
Shadow copy of mhpmevent6 overflow (OF) bit.

[when="HPM_COUNTER_EN[6] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF7 Field

Location:

7

Description:

[when="HPM_COUNTER_EN[7] == true"]
Shadow copy of mhpmevent7 overflow (OF) bit.

[when="HPM_COUNTER_EN[7] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF8 Field

Location:

8

Description:

[when="HPM_COUNTER_EN[8] == true"]
Shadow copy of mhpmevent8 overflow (OF) bit.

[when="HPM_COUNTER_EN[8] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF9 Field

Location:

9

Description:

[when="HPM_COUNTER_EN[9] == true"]
Shadow copy of mhpmevent9 overflow (OF) bit.

[when="HPM_COUNTER_EN[9] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountvf.OF10 Field

Location:

10

Description:

[when="HPM_COUNTER_EN[10] == true"]
Shadow copy of mhpmevent10 overflow (OF) bit.

[when="HPM_COUNTER_EN[10] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountvf.OF11 Field

Location:

11

Description:

[when="HPM_COUNTER_EN[11] == true"]
Shadow copy of mhpmevent11 overflow (OF) bit.

[when="HPM_COUNTER_EN[11] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountvf.OF12 Field

Location:

12

Description:

[when="HPM_COUNTER_EN[12] == true"]
Shadow copy of mhpmevent12 overflow (OF) bit.

[when="HPM_COUNTER_EN[12] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF13 Field

Location:

13

Description:

[when="HPM_COUNTER_EN[13] == true"]

Shadow copy of mhpmevent13 overflow (OF) bit.

[when="HPM_COUNTER_EN[13] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF14 Field

Location:

14

Description:

[when="HPM_COUNTER_EN[14] == true"]

Shadow copy of mhpmevent14 overflow (OF) bit.

[when="HPM_COUNTER_EN[14] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF15 Field

Location:

15

Description:

[when="HPM_COUNTER_EN[15] == true"]

Shadow copy of mhpmevent15 overflow (OF) bit.

[when="HPM_COUNTER_EN[15] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF16 Field

Location:

16

Description:

[when="HPM_COUNTER_EN[16] == true"]

Shadow copy of mhpmevent16 overflow (OF) bit.

[when="HPM_COUNTER_EN[16] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF17 Field

Location:

17

Description:

[when="HPM_COUNTER_EN[17] == true"]

Shadow copy of mhpmevent17 overflow (OF) bit.

[when="HPM_COUNTER_EN[17] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF18 Field

Location:

18

Description:

[when="HPM_COUNTER_EN[18] == true"]

Shadow copy of mhpmevent18 overflow (OF) bit.

[when="HPM_COUNTER_EN[18] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF19 Field

Location:

19

Description:

[when="HPM_COUNTER_EN[19] == true"]
Shadow copy of mhpmevent19 overflow (OF) bit.

[when="HPM_COUNTER_EN[19] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF20 Field

Location:

20

Description:

[when="HPM_COUNTER_EN[20] == true"]
Shadow copy of mhpmevent20 overflow (OF) bit.

[when="HPM_COUNTER_EN[20] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF21 Field

Location:

21

Description:

[when="HPM_COUNTER_EN[21] == true"]
Shadow copy of mhpmevent21 overflow (OF) bit.

[when="HPM_COUNTER_EN[21] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF22 Field

Location:

22

Description:

[when="HPM_COUNTER_EN[22] == true"]
Shadow copy of mhpmevent22 overflow (OF) bit.

[when="HPM_COUNTER_EN[22] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF23 Field

Location:

23

Description:

[when="HPM_COUNTER_EN[23] == true"]
Shadow copy of mhpmevent23 overflow (OF) bit.

[when="HPM_COUNTER_EN[23] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF24 Field

Location:

24

Description:

[when="HPM_COUNTER_EN[24] == true"]
Shadow copy of mhpmevent24 overflow (OF) bit.

[when="HPM_COUNTER_EN[24] == false"]
This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF25 Field

Location:

25

Description:

[when="HPM_COUNTER_EN[25] == true"]
Shadow copy of mhpmevent25 overflow (OF) bit.

[when="HPM_COUNTER_EN[25] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF26 Field

Location:

26

Description:

[when="HPM_COUNTER_EN[26] == true"]

Shadow copy of mhpmevent26 overflow (OF) bit.

[when="HPM_COUNTER_EN[26] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF27 Field

Location:

27

Description:

[when="HPM_COUNTER_EN[27] == true"]

Shadow copy of mhpmevent27 overflow (OF) bit.

[when="HPM_COUNTER_EN[27] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF28 Field

Location:

28

Description:

[when="HPM_COUNTER_EN[28] == true"]

Shadow copy of mhpmevent28 overflow (OF) bit.

[when="HPM_COUNTER_EN[28] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF29 Field

Location:

29

Description:

[when="HPM_COUNTER_EN[29] == true"]

Shadow copy of mhpmevent29 overflow (OF) bit.

[when="HPM_COUNTER_EN[29] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF30 Field

Location:

30

Description:

[when="HPM_COUNTER_EN[30] == true"]

Shadow copy of mhpmevent30 overflow (OF) bit.

[when="HPM_COUNTER_EN[30] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

scountovf.OF31 Field

Location:

31

Description:

[when="HPM_COUNTER_EN[31] == true"]

Shadow copy of mhpmevent31 overflow (OF) bit.

[when="HPM_COUNTER_EN[31] == false"]

This field is read-only zero because the counter is not enabled.

Type:

RO

RO-H

Reset value:

UNDEFINED_LEGAL

C.129.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
Bits<32> mask;
if (mode() == PrivilegeMode::VS) {
    mask = $bits(CSR[CSR[mcounteren]]) & $bits(CSR[CSR[hcounteren]]);
} else {
    mask = $bits(CSR[CSR[mcounteren]]) & $bits(CSR[CSR[scounteren]]);
}
Bits<32> value = 0;
value = value | (CSR[mhpmevent3].OF << 3);
value = value | (CSR[mhpmevent4].OF << 4);
value = value | (CSR[mhpmevent5].OF << 5);
value = value | (CSR[mhpmevent6].OF << 6);
value = value | (CSR[mhpmevent7].OF << 7);
value = value | (CSR[mhpmevent8].OF << 8);
value = value | (CSR[mhpmevent9].OF << 9);
value = value | (CSR[mhpmevent10].OF << 10);
value = value | (CSR[mhpmevent11].OF << 11);
value = value | (CSR[mhpmevent12].OF << 12);
value = value | (CSR[mhpmevent13].OF << 13);
value = value | (CSR[mhpmevent14].OF << 14);
value = value | (CSR[mhpmevent15].OF << 15);
value = value | (CSR[mhpmevent16].OF << 16);
value = value | (CSR[mhpmevent17].OF << 17);
value = value | (CSR[mhpmevent18].OF << 18);
value = value | (CSR[mhpmevent19].OF << 19);
value = value | (CSR[mhpmevent20].OF << 20);
value = value | (CSR[mhpmevent21].OF << 21);
value = value | (CSR[mhpmevent22].OF << 22);
value = value | (CSR[mhpmevent23].OF << 23);
value = value | (CSR[mhpmevent24].OF << 24);
value = value | (CSR[mhpmevent25].OF << 25);
value = value | (CSR[mhpmevent26].OF << 26);
value = value | (CSR[mhpmevent27].OF << 27);
value = value | (CSR[mhpmevent28].OF << 28);
value = value | (CSR[mhpmevent29].OF << 29);
value = value | (CSR[mhpmevent30].OF << 30);
value = value | (CSR[mhpmevent31].OF << 31);
return value & mask;
```

C.130. sepc

Supervisor Exception Program Counter

Written with the PC of an instruction on an exception or interrupt taken in (H)S-mode.

Also controls where the hart jumps on an exception return from (H)S-mode.

C.130.1. Attributes

CSR Address	0x141
Defining extension	S
Length	64-bit
Privilege Mode	S

C.130.2. Format

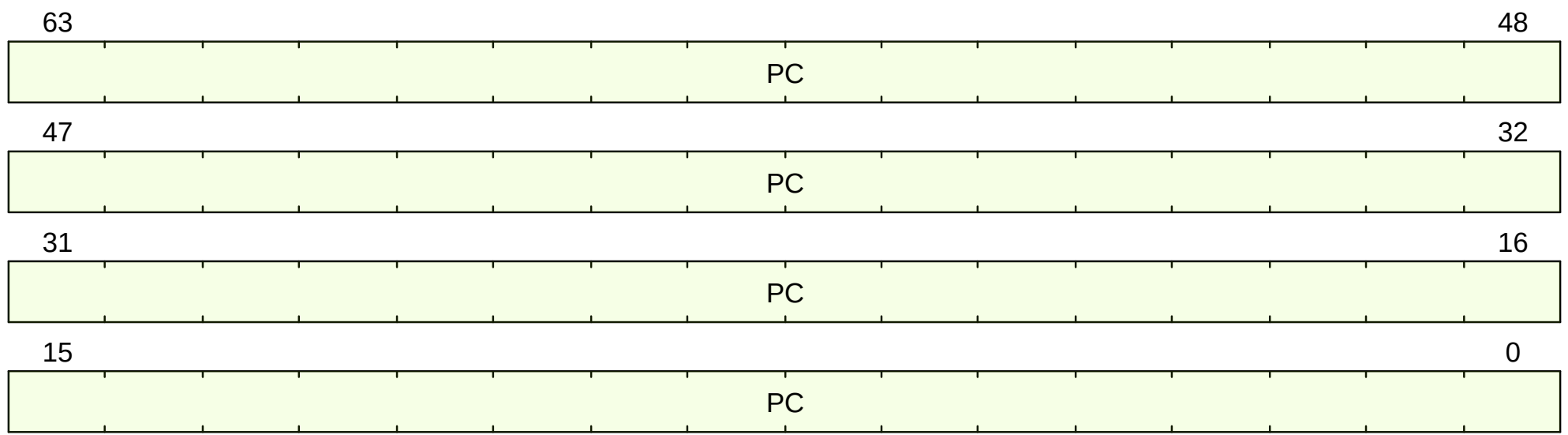


Figure 132. *sepc* format

C.130.3. Field Summary

Na me	Location	Type	Reset Value
sepc.PC	63:0	RW-RH	UNDEFINED_LEGAL

C.130.4. Fields

[sepc.PC](#) Field

Location:

63:0

Description:

When a trap is taken into S-mode, [sepc.PC](#) is written with the virtual address of the instruction that was interrupted or that encountered the exception. Otherwise, [sepc.PC](#) is never written by the implementation, though it may be explicitly written by software.

On an exception return from S-mode (from the SRET instruction), control transfers to the virtual address read out of [sepc.PC](#).

Because PCs are always <% if ext?(:C) %>halfword<% else %>word<% end %>-aligned, <% if ext?(:C) %>bit 0<% else %>bits 1:0<% end %> of [sepc.PC](#) are always read-only 0.

[when,"ext?(:C) && MUTABLE_MISA_C == true"]
When [misa.C](#) is clear, bit 1 is masked to zero. Writes to bit 1 are still captured, and may be visible on the next read with [misa.C](#) is set.

Holds bits 63:<%= ext?(:C) ? 2 : 1 %> of the virtual address associated with an exception.

Type:

RW-RH

Reset value:

UNDEFINED_LEGAL

C.130.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through [csrrw](#)), the following determines the written value:

```
PC = return csr_value.PC & ~64'b1;
```

C.130.6. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (implemented?(ExtensionName::C) && CSR[misa].C == 1'b1) {  
  return CSR[sepc].PC & ~64'b1;  
} else {  
  return CSR[sepc].PC;  
}
```

C.131. sip

Supervisor Interrupt Pending

A restricted view of the interrupt pending bits in [mip](#).

Hypervisor-related interrupts (VS-mode interrupts and Supervisor Guest interrupts) are not reflected in [sip](#) even though those interrupts can be taken in HS-mode. Instead, they are reported through [hip](#).

C.131.1. Attributes

CSR Address	0x144
Defining extension	S
Length	64-bit
Privilege Mode	S

C.131.2. Format

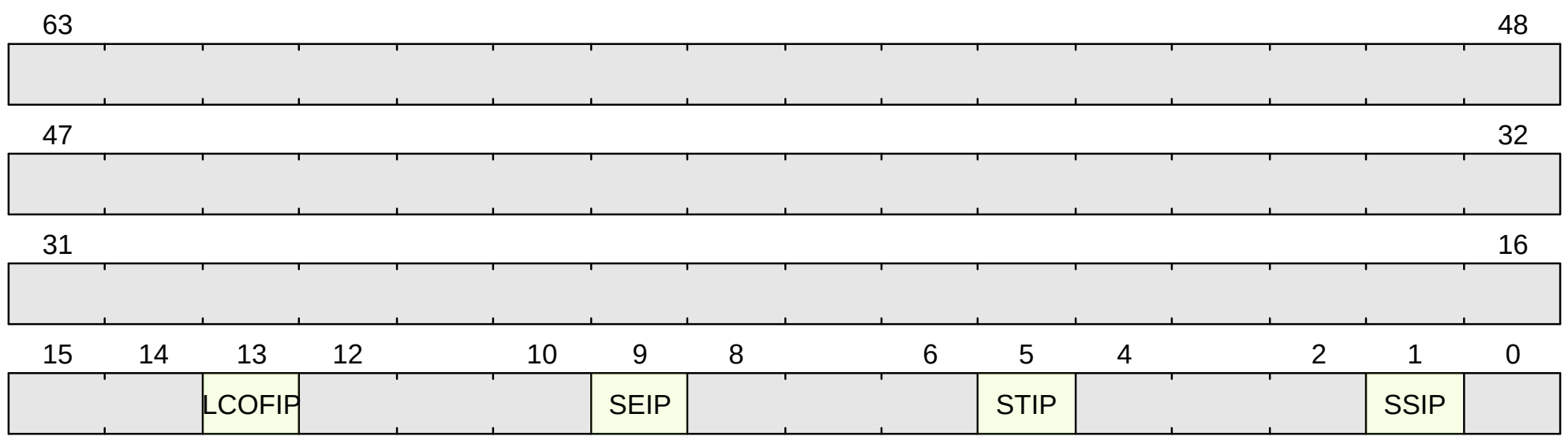


Figure 133. sip format

C.131.3. Field Summary

Na me	Location	Type	Reset Value
sip.S SIP	1	RW	UNDEFINED_LEGAL
sip.S TIP	5	RO-H	UNDEFINED_LEGAL
sip.S EIP	9	RO-H	UNDEFINED_LEGAL
sip.L COFI P	13	RW-H	UNDEFINED_LEGAL

C.131.4. Fields

[sip.SSIP](#) Field

Location:
1

Description:
Supervisor Software Interrupt Pending

Reports the current pending state of an (H)S-mode software interrupt.

When Supervisor Software Interrupts are not delegated to (H)S-mode ([mideleg.SSI](#) is clear), [sip.SSIP](#) is read-only 0.

Otherwise, [sip.SSIP](#) is an alias of [mip.SSIP](#).

<%- if ext?(:Smaia) -%>
When using AIA/IMSIC, IPIs are expected to be delivered as external interrupts

and SSIP is not backed by any hardware update (aside from any aliasing effects).

However, SSIP is still writable by S-mode software and, when written, can be used to generate an S-mode Software Interrupt.

```
<%- end -%>
```

Since it is an alias, writes to `sip.SSIP` are also be reflected in `mip.SSIP``<% if ext?(:Smaia) %>` and `mvip.SSIP``<% end %>`.

```
<% if ext?(:Smaia) %>_Aliases_<% else %>_Alias_<% end %>:
```

- `mip.SSIP` when `mideleg.SSI` is set
`<%- if ext?(:Smaia) -%>`
- `mvip.SSIP` when `mideleg.SSI` is set
`<%- end -%>`

To summarize:

[separator="!",%autowidth]

!===

! `mideleg.SSI` ! `sip.SSIP` behavior

! 0 ! read-only 0

! 1 ! writable alias of `mip.SSIP` `<% if ext?(:Smaia) %>`and `mvip.SSIP``<% end %>`

!===

Type:

RW

Reset value:

UNDEFINED_LEGAL

`sip.STIP` Field

Location:

5

Description:

Supervisor Timer Interrupt Pending

Reports the current pending state of an (H)S-mode timer interrupt.

When Supervisor Timer Interrupts are not delegated to (H)S-mode (*i.e.*, `mideleg.STI` is clear), `sip.STIP` is read-only 0.

Otherwise, `sip.STIP` is a read-only view of `mip.STIP`.

```
<% if ext?(:Smaia) %>_Aliases_<% else %>_Alias_<% end %>:
```

- `mip.STIP` when `mideleg.STI` is set
`<%- if ext?(:Smaia) -%>`
- `mvip.STIP` when `mideleg.SSI` is set and `menvcfg.STCE` is clear.
`<%- end -%>`

To summarize:

[separator="!",%autowidth]

!===

! `mideleg.STI` ! `sip.STIP` behavior

! 0 ! read-only 0

! 1 ! read-only alias of `mip.STIP` `<% if ext?(:Smaia) %>`(and `mvip.STIP` when `menvcfg.STCE` is clear)`<% end %>`

!===

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

sip.SEIP Field

Location:

9

Description:

Supervisor External Interrupt Pending

Reports the current pending state of an (H)S-mode external interrupt.

When Supervisor External Interrupts are not delegated to (H)S-mode (*i.e.*, [mideleg.SEI](#) is clear), [sip.SEIP](#) is read-only 0.

Otherwise, [sip.SEIP](#) is a read-only view of [mip.SEIP](#).

To summarize:
[separator="!",%autowidth]
!===
! [mideleg.SEI](#) ! [sip.SEIP](#) behavior

! 0 ! read-only 0
! 1 ! read-only alias of [mip.SEIP](#)
!===

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

sip.LCOFIP Field

Location:

13

Description:

Local Counter Overflow Interrupt pending

Reports the current pending state of a Local Counter Overflow interrupt.

When Local Counter Overflow interrupts are not delegated to (H)S-mode (*i.e.*, [mideleg.LCOFI](#) is clear), [sip.LCOFIP](#) is read-only 0.

Otherwise, [sip.LCOFIP](#) is an alias of [mip.LCOFIP](#).

Software writes 0 to [sip.LCOFIP](#) to clear the pending interrupt.

To summarize:
[separator="!",%autowidth]
!===
! [mideleg.LCOFI](#) ! [sip.LCOFIP](#) behavior

! 0 ! read-only 0
! 1
a! writable alias of [mip.LCOFIP](#) (and [vsip.LCOFIP](#) when [hideleg.LCOFI](#) is set)
!===

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

C.132. sscratch

Supervisor Scratch Register

Scratch register for software use. Bits are not interpreted by hardware.

C.132.1. Attributes

CSR Address	0x140
Defining extension	S
Length	64-bit
Privilege Mode	S

C.132.2. Format

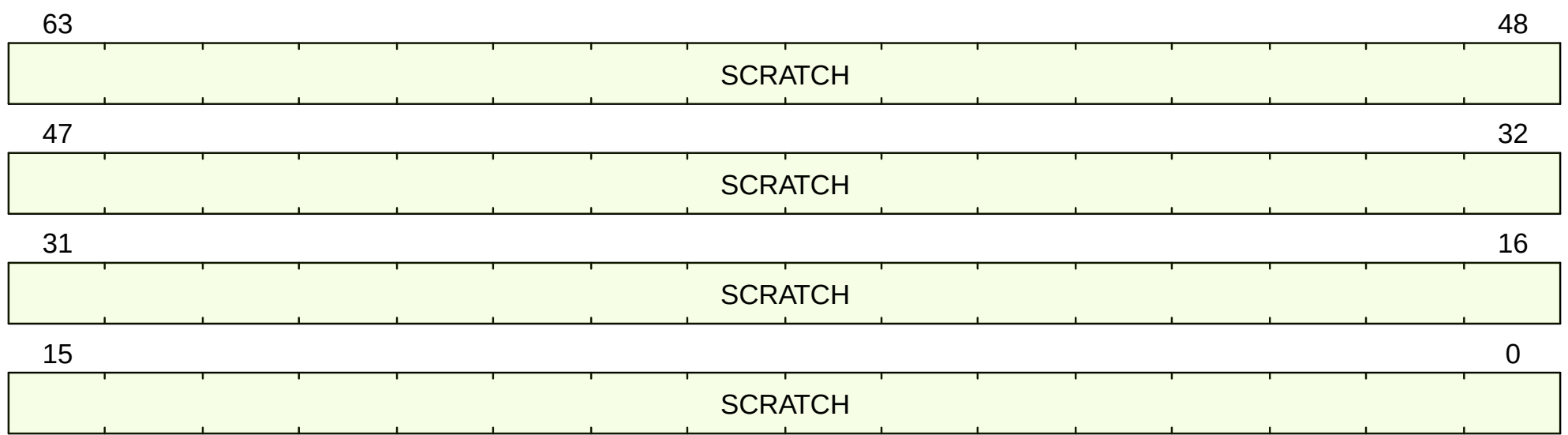


Figure 134. sscratch format

C.132.3. Field Summary

Name	Location	Type	Reset Value
sscratch.SCRATCH	63:0	RW	UNDEFINED_LEGAL

C.132.4. Fields

sscratch.SCRATCH Field

Location:

63:0

Description:

Scratch value

Type:

RW

Reset value:

UNDEFINED_LEGAL

C.133. sstatus

Supervisor Status

The sstatus register tracks and controls the hart’s current operating state.

All fields in sstatus are aliases of the same field in mstatus.

C.133.1. Attributes

CSR Address	0x100
Defining extension	S
Length	* 32 when CSR[mstatus].SXL == 0 * 64 when CSR[mstatus].SXL == 1
Privilege Mode	S

C.133.2. Format

This CSR format changes dynamically with XLEN.

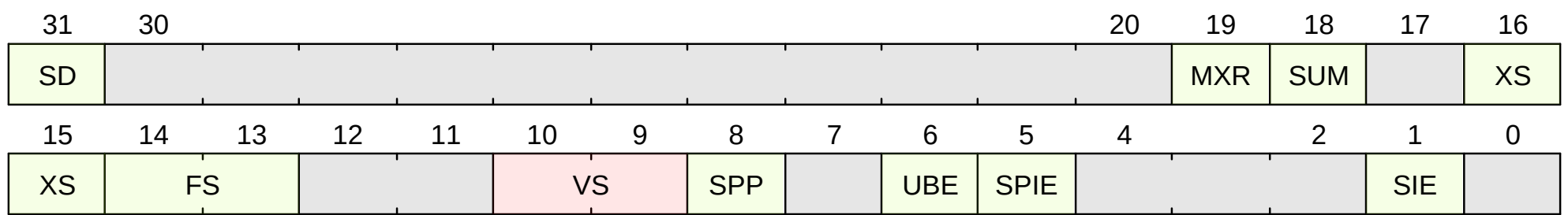


Figure 135. sstatus Format when CSR[mstatus].SXL == 0

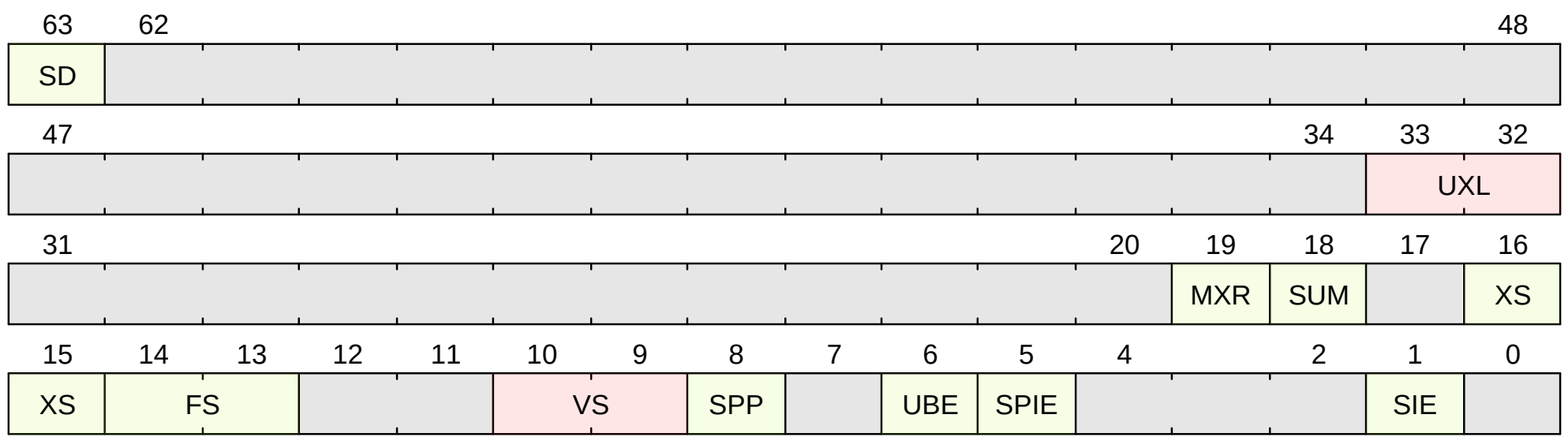


Figure 136. sstatus Format when CSR[mstatus].SXL == 1

C.133.3. Field Summary

Nam e	Location	Type	Reset Value
sstat us.S D	31 63	RO-H	UNDEFINED_LEGAL
sstat us.U XL	33:32	RO	2
sstat us.M XR	19	RW	UNDEFINED_LEGAL
sstat us.S UM	18	RW	UNDEFINED_LEGAL
sstat us.X S	16:15	RO	UNDEFINED_LEGAL
sstat us.FS	14:13	RW-H	UNDEFINED_LEGAL

Name	Location	Type	Reset Value
sstatus.VS	10:9	RW-H	UNDEFINED_LEGAL
sstatus.SPP	8	RW-H	UNDEFINED_LEGAL
sstatus.UBE	6	RO	UNDEFINED_LEGAL
sstatus.SPIE	5	RW-H	UNDEFINED_LEGAL
sstatus.SIE	1	RW-H	UNDEFINED_LEGAL

C.133.4. Fields

[sstatus.SD](#) Field

Location:

- 31 when CSR[mstatus].SXL == 0
- 63 when CSR[mstatus].SXL == 1

Description:

State Dirty

Alias of [mstatus.SD](#).

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

[sstatus.UXL](#) Field



UXL is only defined in RV64 ([CSR\[mstatus\].SXL == 1](#))

Location:

33:32

Description:

U-mode XLEN

Alias of [mstatus.UXL](#).

Type:

RO

Reset value:

2

[sstatus.MXR](#) Field

Location:

19

Description:

Make eXecutable Readable

Alias of [mstatus.MXR](#).

Type:
RW

Reset value:
UNDEFINED_LEGAL

sstatus.SUM Field

Location:
18

Description:
permit Supervisor Memory Access

Alias of [mstatus.SUM](#).

Type:
RW

Reset value:
UNDEFINED_LEGAL

sstatus.XS Field

Location:
16:15

Description:
Custom (X) extension context Status.

Alias of [mstatus.XS](#).

Type:
RO

Reset value:
UNDEFINED_LEGAL

sstatus.FS Field

Location:
14:13

Description:
Floating point context status.

Alias of [mstatus.FS](#).

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

sstatus.VS Field

Location:
10:9

Description:
Vector context status.

Alias of [mstatus.VS](#).

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

sstatus.SPP Field

Location:
8

Description:
S-mode Previous Privilege

Alias of [mstatus.SPP](#).

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

sstatus.UBE Field

Location:
6

Description:
U-mode Big Endian

Alias of [mstatus.UBE](#).

Type:
RO

Reset value:
UNDEFINED_LEGAL

sstatus.SPIE Field

Location:
5

Description:
S-mode Previous Interrupt Enable

Alias of [mstatus.SPIE](#).

Type:
RW-H

Reset value:
UNDEFINED_LEGAL

sstatus.SIE Field

Location:
1

Description:
S-mode Interrupt Enable

Alias of [mstatus.SIE](#).

Type:

RW-H

Reset value:

UNDEFINED_LEGAL

C.134. stval

Supervisor Trap Value

Holds trap-specific information

C.134.1. Attributes

CSR Address	0x143
Defining extension	S
Length	64-bit
Privilege Mode	S

C.134.2. Format

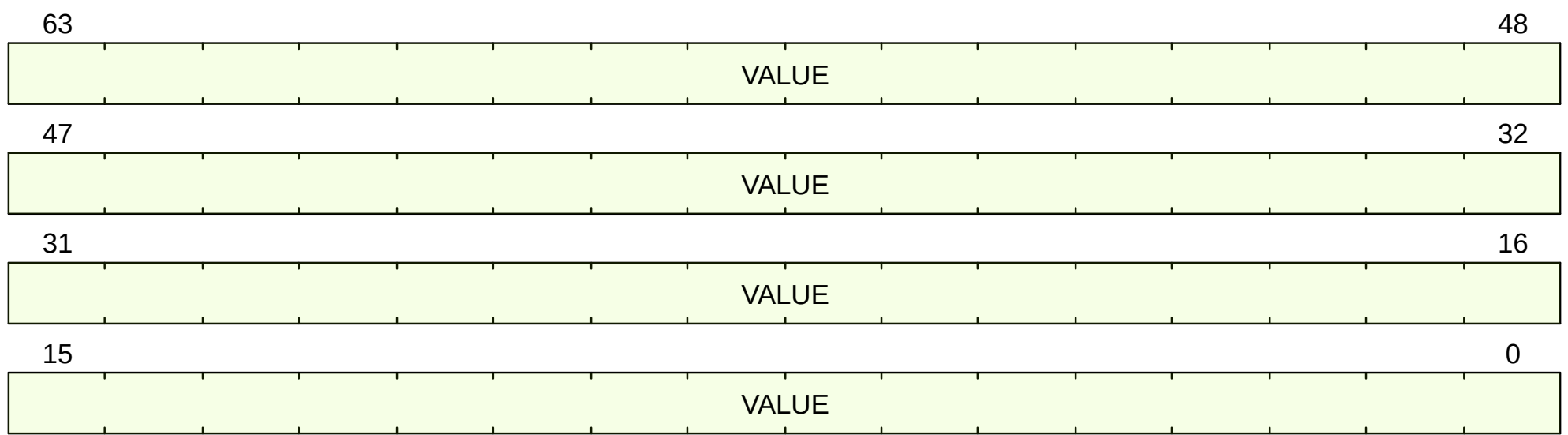


Figure 137. stval format

C.134.3. Field Summary

Nam e	Location	Type	Reset Value
stval. VAL UE	63:0	RW-H	0

C.134.4. Fields

stval.VALUE Field

Location:
63:0

Description:
Written with trap-specific information when a trap is taken into S-mode.

The values are:

[separator="!"]
!===
! Exception type ! Value

! [0] Instruction address misaligned ! The misaligned virtual PC (same as the value written to [mepc](#)).
! [1] Instruction access fault ! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the access fault <%- unless ext?(:C) -%>(same as the value written to [mepc](#))<%- end -%>.
! [2] Illegal Instruction ! The encoding of the illegal instruction.
! [3] Breakpoint
! [when,"REPORT_VA_IN_STVAL_ON_BREAKPOINT == true"]
When caused by an EBREAK instruction, the virtual PC of the breakpoint instruction.

[when,"REPORT_VA_IN_STVAL_ON_BREAKPOINT == false"]
When caused by an EBREAK instruction, zero.

When caused by a data address (*i.e.*, watchpoint) breakpoint, the faulting virtual address.

When caused by an instruction address breakpoint, the faulting virtual PC.

! [4] Load address misaligned ! The misaligned virtual load address.

! [5] Load access fault

! The part of virtual load address causing in the access fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte load is equally split across a page and the fault occurs on the second page,
address + 4 is reported).

(Even though the access fault arises on a physical address, the virtual address is reported)

! [6] Store/AMO address misaligned ! The misaligned virtual store/AMO address.

! [7] Store/AMO access fault

! The virtual store/AMO address causing the access fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte store is equally split across a page and the fault occurs on the second page,
address + 4 is reported).

(Even though the access fault arises on a physical address, the virtual address is reported)

! [8] Environment call from U-mode <% if ext?(:H) %>or VU-mode<% end %> ! Zero

! [9] Environment call from (H)S-mode ! Zero

<%- if ext?(:H) -%>

! [10] Environment call from VS-mode ! Zero

<%- end -%>

! [12] Instruction page fault

! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the page fault

<% unless ext?(:C) %>(same as the value written to [mepc](#))<% end %>.

! [13] Load page fault

! The part of the virtual load address causing in the page fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte load is equally split across a page and the fault occurs on the second page, address + 4 is reported).

! [15] Store/AMO page fault

! The virtual store/AMO address causing in the page fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte store is equally split across a page and the fault occurs on the second page, address + 4 is reported).

<%- if ext?(:H) -%>

! [20] Instruction guest-page fault

! The <% if ext?(:C) %> portion of the <% end %> virtual PC causing the fault <% unless ext?(:C) %>(same as the value written to [mepc](#))<% end %>.

The guest physical address is reported in [mtval2](#).

! [21] Load guest-page fault

! The part of the virtual address causing the fault.

When the load is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte load is equally split across a page and the fault occurs on the second page, address + 4 is reported).

The guest physical address is reported in [mtval2](#).

! [22] Virtual instruction

! The encoding of the faulting virtual instruction.

! [23] Store/AMO guest-page fault

! The part of the virtual address causing the fault.

When the store/AMO is misaligned, the reported value is the smallest address on the page causing a fault
(*e.g.*, if an 8-byte store is equally split across a page and the fault occurs on the second page, address + 4 is reported).

The guest physical address is reported in [htval](#).

<%- end -%>

!===

Type:

RW-H

Reset value:

0

C.135. stvec

Supervisor Trap Vector

Controls where traps jump.

C.135.1. Attributes

CSR Address	0x105
Defining extension	S
Length	64-bit
Privilege Mode	S

C.135.2. Format

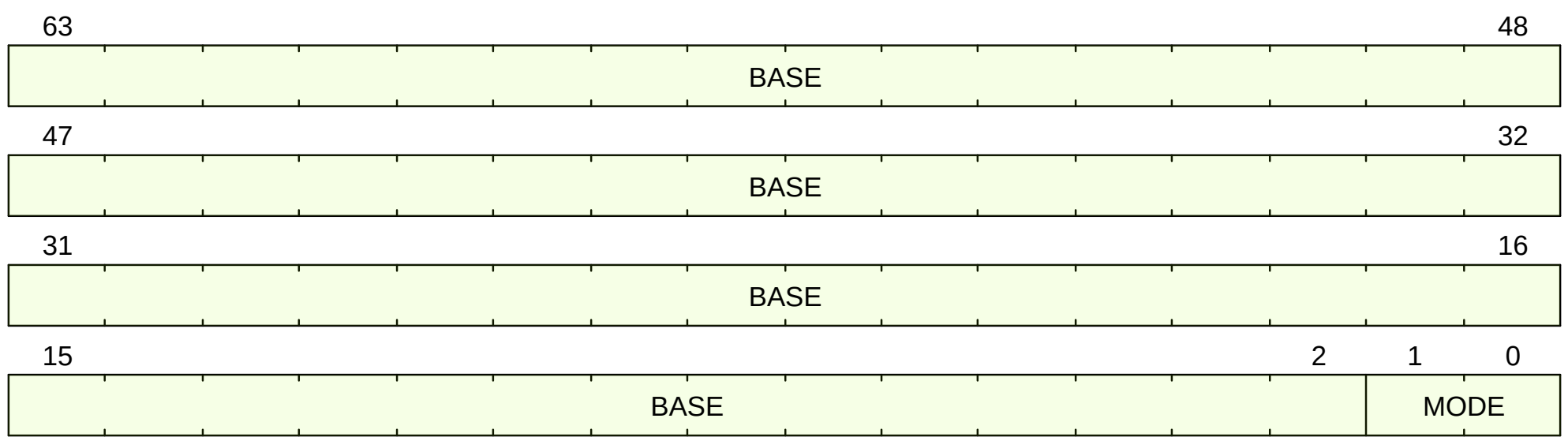


Figure 138. stvec format

C.135.3. Field Summary

Nam e	Location	Type	Reset Value
stvec .BASE	63:2	RW-R	UNDEFINED_LEGAL
stvec .MODE	1:0	RW-R	0

C.135.4. Fields

stvec.BASE Field

Location:
63:2

Description:
<%- va_size = ext?(:Sv57) ? 57 : (ext?(:Sv48) ? 49 :39) -%>
Bit 63:0 of the virtual address of the exception vector for any trap taken into S-mode.

If the base address is written with a non-cannonical address (*i.e.*, bits 63:<%= va_size %> do not match bit <%= va_size-1 %>), the write should be ignored.

Type:
RW-R

Reset value:
UNDEFINED_LEGAL

stvec.MODE Field

Location:

1:0

Description:

Vectoring mode for asynchronous interrupts.

0 - Direct, 1 - Vectored

When Direct, all synchronous exceptions and asynchronous interrupts jump to (`stvec.BASE << 2`).

When Vectored, asynchronous interrupts jump to (`stvec.BASE << 2 + scause*4`) while synchronous exceptions continue to jump to (`stvec.BASE << 2`).

Type:

RW-R

Reset value:

0

C.135.5. Software write

This CSR may store a value that is different from what software attempts to write.

When a software write occurs (*e.g.*, through `csrrw`), the following determines the written value:

```
BASE = # Base spec says that BASE must be 4-byte aligned, which will always be the case
# implementations may put further constraints on BASE when MODE != Direct
# If that is the case, stvec should have an override for the implementation
return csr_value.BASE;

MODE = if (STVEC_MODE_DIRECT && csr_value.MODE == 0) {
    return 0;
} else if (STVEC_MODE_VECTORED && csr_value.MODE == 1) {
    return 1;
} else {
    return UNDEFINED_LEGAL_DETERMINISTIC;
}
```


C.136. tdata1

Trigger Data 1

This register provides access to the trigger selected by [tselect](#). The reset values listed here apply to every underlying trigger.

This register is optional if no triggers are implemented. Writing 0 to this register must result in a trigger that is disabled. If this trigger supports multiple types, then the hardware should disable it by changing type to 15.

C.136.1. Attributes

CSR Address	0x7a1
Defining extension	Sdtrig
Length	* 32 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%) * 64 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%)
Privilege Mode	M

C.136.2. Format

This CSR format changes dynamically with XLEN.

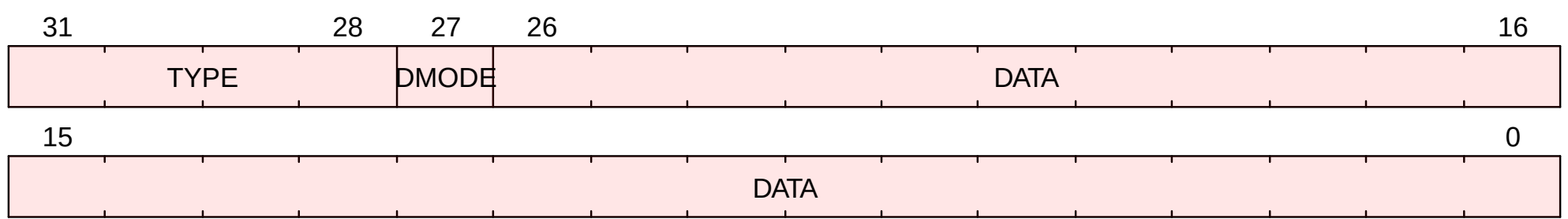


Figure 139. tdata1 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 0) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 0)

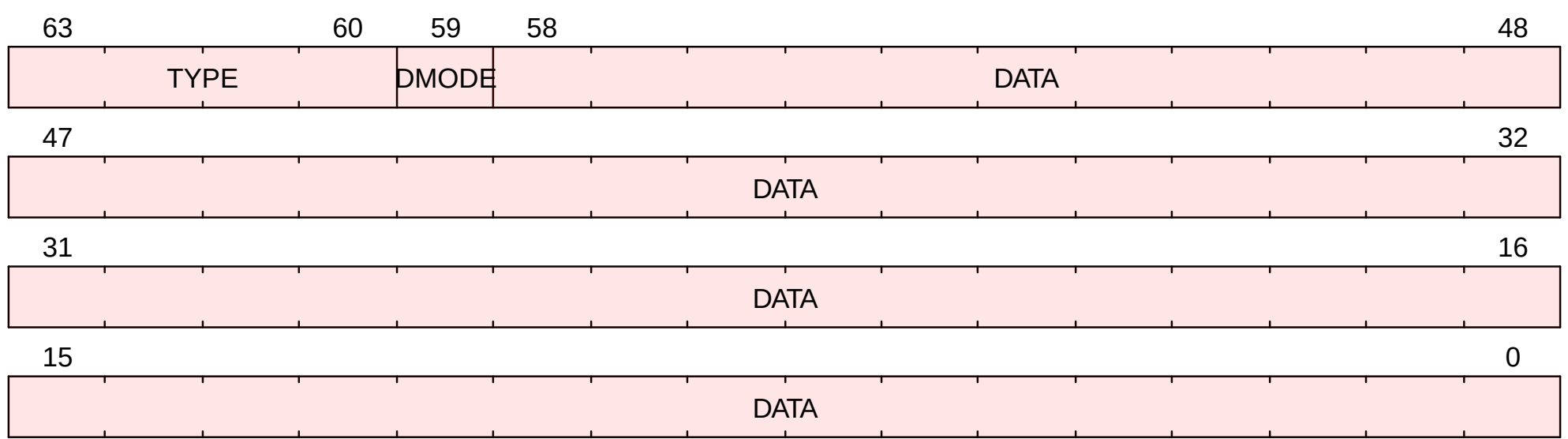


Figure 140. tdata1 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 1) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 1)

C.136.3. Field Summary

Nam e	Location	Type	Reset Value
tdata 1.TYP E	63:60	RW	UNDEFINED_LEGAL
tdata 1.DM ODE	59	RW	0
tdata 1.DAT A	58:0	RW	UNDEFINED_LEGAL

C.136.4. Fields

tdata1.TYPE Field

Location:

63:60

Description:

0 (none)

There is no trigger at this tselect.

1 (legacy)

The trigger is a legacy SiFive address match trigger. These should not be implemented and aren’t further documented here.

2 (mcontrol)

The trigger is an address/data match trigger. The remaining bits in this register act as described in mcontrol.

3 (icount)

The trigger is an instruction count trigger. The remaining bits in this register act as described in icount.

4 (itrigger)

The trigger is an interrupt trigger. The remaining bits in this register act as described in itrigger.

5 (etrigger)

The trigger is an exception trigger. The remaining bits in this register act as described in etrigger.

6 (mcontrol6)

The trigger is an address/data match trigger. The remaining bits in this register act as described in mcontrol6. This is similar to a type 2 trigger, but provides additional functionality and should be used instead of type 2 in newer implementations.

7 (tmexttrigger)

The trigger is a trigger source external to the TM. The remaining bits in this register act as described in tmexttrigger.

12—14 (custom)

These trigger types are available for non-standard use.

15 (disabled)

This trigger is disabled. In this state, tdata2 and tdata3 can be written with any value that is supported for any of the types this trigger implements. The remaining bits in this register, except for DMODE, are ignored.

Other values are reserved for future use.

Type:

RW

Reset value:

UNDEFINED_LEGAL

tdata1.DMODE Field

Location:

59

Description:

If type is 0, then this bit is hard-wired to 0.

0 (both): Both Debug and M-mode can write the tdata registers at the selected tselect.

1 (dmode): Only Debug Mode can write the tdata registers at the selected tselect. Writes from other modes are ignored.

This bit is only writable from Debug Mode. In ordinary use, external debuggers will always set this bit when configuring a trigger. When clearing this bit, debuggers should also set the action field (whose location depends on type) to something other than 1.

Type:

RW

Reset value:

0

tdata1.DATA Field

Location:

58:0

Description:

If type is 0, then this field is hard-wired to 0.
Trigger-specific data.

Type:

RW

Reset value:

UNDEFINED_LEGAL

C.137. tdata2

Trigger Data 2

This register provides access to the trigger selected by [tselect](#). The reset values listed here apply to every underlying trigger.

Trigger-specific data. It is optional if no implemented triggers use it. If the trigger is disabled, then this register can be written with any value supported by any of the trigger types supported by this trigger. If XLEN is less than DXLEN, writes to this register are sign-extended.

C.137.1. Attributes

CSR Address	0x7a2
Defining extension	Sdtrig
Length	* 32 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %) * 64 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%)
Privilege Mode	M

C.137.2. Format

This CSR format changes dynamically with XLEN.

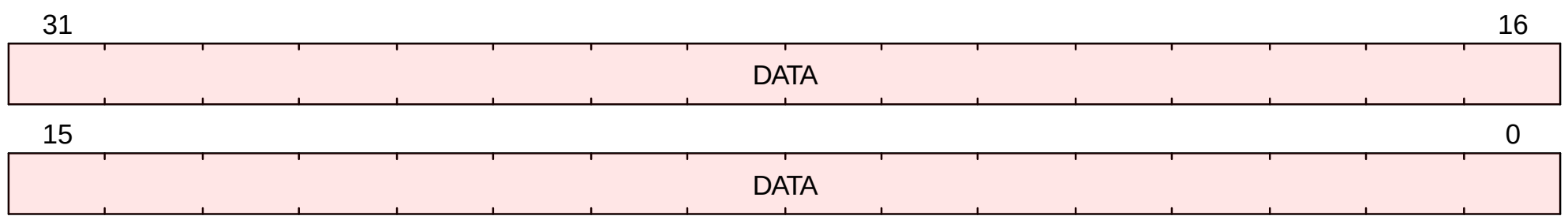


Figure 141. tdata2 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 0) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 0)

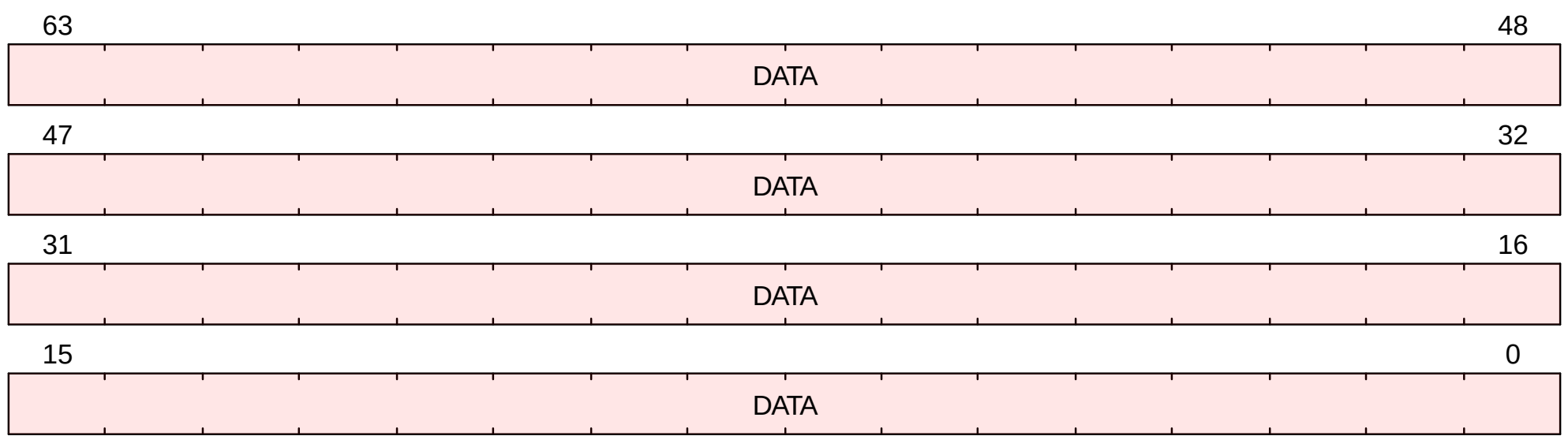


Figure 142. tdata2 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 1) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 1)

C.137.3. Field Summary

Nam e	Location	Type	Reset Value
tdata2.DA TA	63:0	RW	UNDEFINED_LEGAL

C.137.4. Fields

[tdata2.DA TA](#) Field

Location:

63:0

Description:

Data value

Type:

RW

Reset value:

UNDEFINED_LEGAL

C.138. tdata3

Trigger Data 3

This register provides access to the trigger selected by [tselect](#). The reset values listed here apply to every underlying trigger.

Trigger-specific data. It is optional if no implemented triggers use it. If the trigger is disabled, then this register can be written with any value supported by any of the trigger types supported by this trigger. If XLEN is less than DXLEN, writes to this register are sign-extended.

C.138.1. Attributes

CSR Address	0x7a3
Defining extension	Sdtrig
Length	* 32 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %) * 64 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%)
Privilege Mode	M

C.138.2. Format

This CSR format changes dynamically with XLEN.

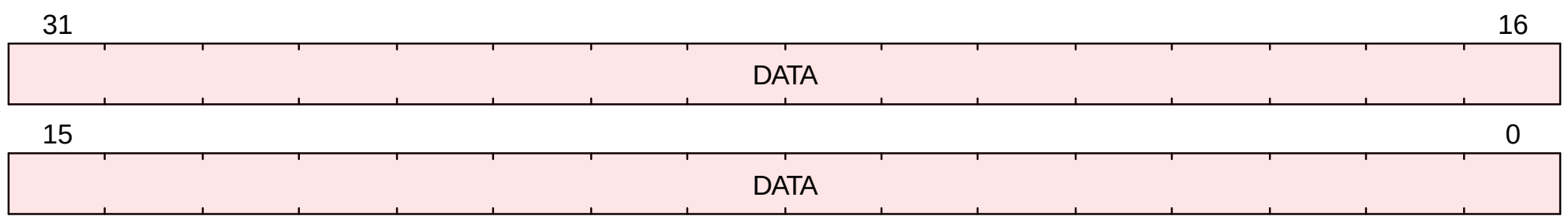


Figure 143. tdata3 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 0) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 0)

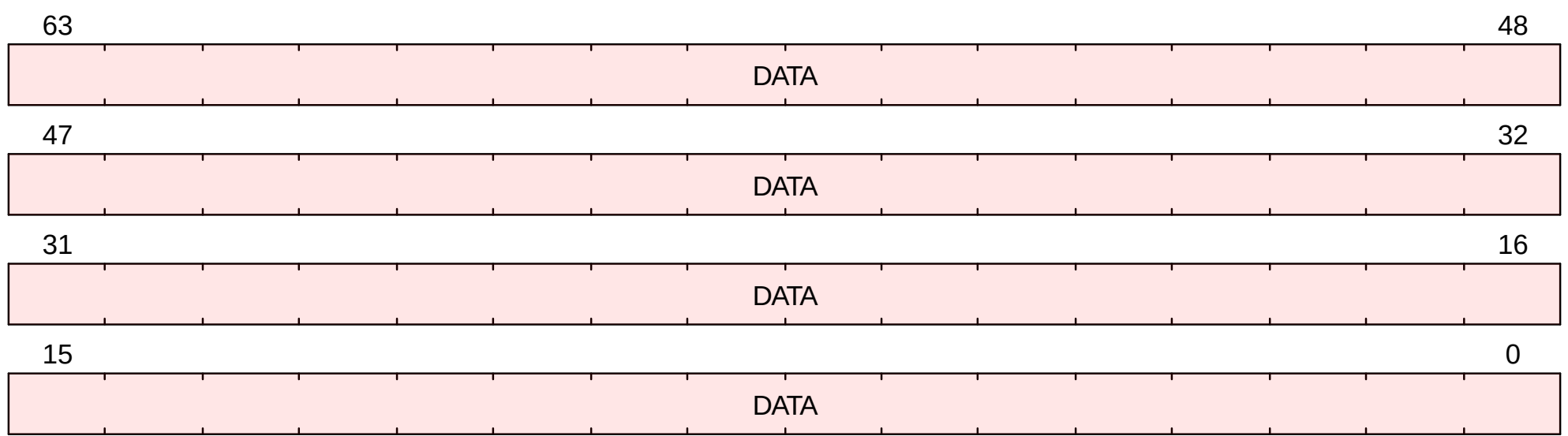


Figure 144. tdata3 Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 1) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 1)

C.138.3. Field Summary

Nam e	Location	Type	Reset Value
tdata3.DATA	63:0	RW	UNDEFINED_LEGAL

C.138.4. Fields

[tdata3.DATA](#) Field

Location:

63:0

Description:

Data value

Type:

RW

Reset value:

UNDEFINED_LEGAL

C.139. time

Timer for RDTIME Instruction

This CSR does not exist, and access will cause an IllegalInstruction exception.

Shadow of the memory-mapped M-mode CSR `mtime`.

Privilege mode access is controlled with `mcounteren.TM`, `scounteren.TM`, and `hcounteren.TM` as follows:

mcounteren.TM	scounteren.TM	scounteren.TM	time behavior			
			S-mode	U-mode	VS-mode	VU-mode
0	-	-	Illegal Instruction	Illegal Instruction	Illegal Instruction	Illegal Instruction
1	0	0	read-only	Illegal Instruction	Illegal Instruction	Illegal Instruction
1	1	0	read-only	read-only	Illegal Instruction	Illegal Instruction
1	0	1	read-only	Illegal Instruction	read-only	Illegal Instruction
1	1	1	read-only	read-only	read-only	read-only

C.139.1. Attributes

CSR Address	0xc01
Defining extension	Zicntr
Length	64-bit
Privilege Mode	U

C.139.2. Format

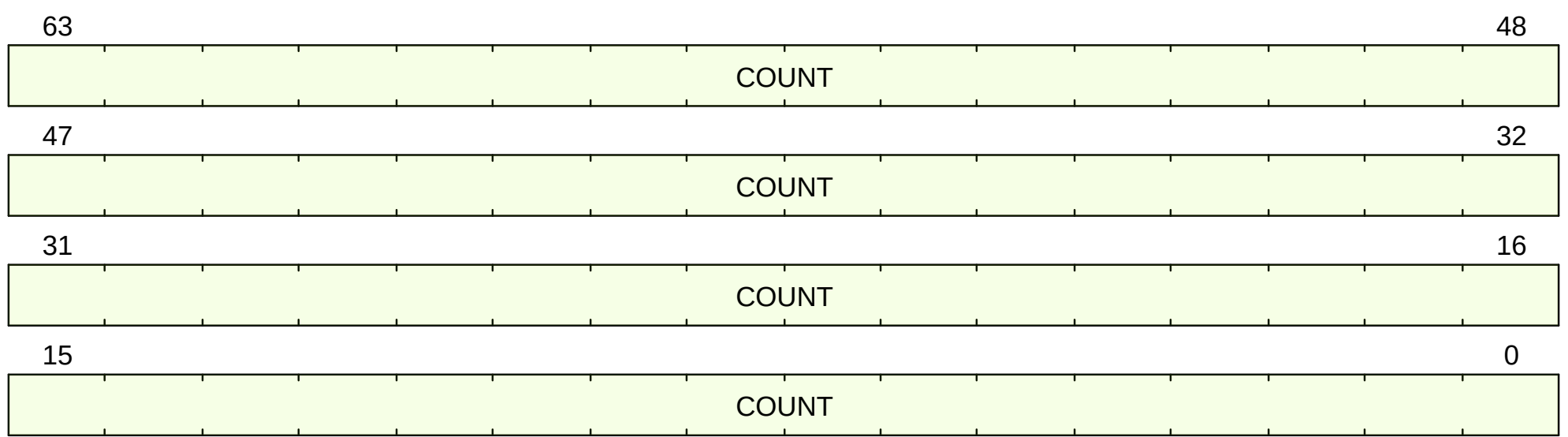


Figure 145. time format

C.139.3. Field Summary

Nam e	Location	Type	Reset Value
time.COUNT	63:0	RO-H	UNDEFINED_LEGAL

C.139.4. Fields

time.COUNT Field

Location:

63:0

Description:

Reports the current wall-clock time from the timer device.

Alias of the `mtime` memory-mapped CSR.

Type:

RO-H

Reset value:

UNDEFINED_LEGAL

C.139.5. Software read

This CSR may return a value that is different from what is stored in hardware.

```
if (!TIME_CSR_IMPLEMENTED) {
    unimplemented_csr($encoding);
}
if (mode() == PrivilegeMode::S) {
    if (CSR[mcounteren].TM == 1'b0) {
        raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
} else if (mode() == PrivilegeMode::U) {
    if (CSR[misa].S == 1'b1) {
        if ((CSR[mcounteren].TM & CSR[scounteren].TM) == 1'b0) {
            raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
        }
    } else if (CSR[mcounteren].TM == 1'b0) {
        raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
} else if (mode() == PrivilegeMode::VS) {
    if (CSR[hcounteren].TM == 1'b0 && CSR[mcounteren].TM == 1'b1) {
        raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    } else if (CSR[mcounteren].TM == 1'b0) {
        raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
} else if (mode() == PrivilegeMode::VU) {
    if (CSR[hcounteren].TM & CSR[scounteren].TM == 1'b0 && (CSR[mcounteren].IR == 1'b1) {
        raise(ExceptionCode::VirtualInstruction, mode(), $encoding);
    } else if (CSR[mcounteren].TM == 1'b0) {
        raise(ExceptionCode::IllegalInstruction, mode(), $encoding);
    }
}
return read_mtime();
```

C.140. tselect

Trigger Select

This register determines which trigger is accessible through the other Trigger Module registers.

It is optional if no triggers are implemented. The set of accessible triggers must start at 0, and be contiguous. This register is WARL. Writes of values greater than or equal to the number of supported triggers may result in a different value in this register than what was written or may point to a trigger where type=0.

To verify that what they wrote is a valid index, debuggers can read back the value and check that tselect holds what they wrote and read tdata1 to see that type is non-zero. Since triggers can be used both by Debug Mode and M-mode, the external debugger must restore this register if it modifies it.

C.140.1. Attributes

CSR Address	0x7a0
Defining extension	Sdtrig
Length	* 32 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%)* 64 when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1)
	(priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == %%)
	(priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == %%)
Privilege Mode	M

C.140.2. Format

This CSR format changes dynamically with XLEN.

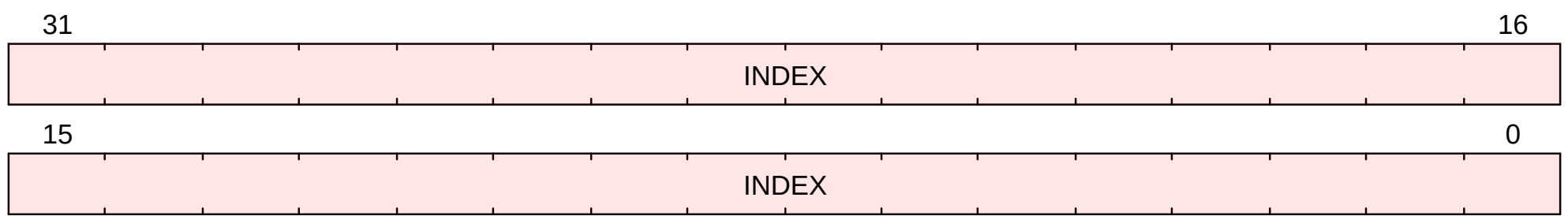


Figure 146. tselect Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 0) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 0) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 0)

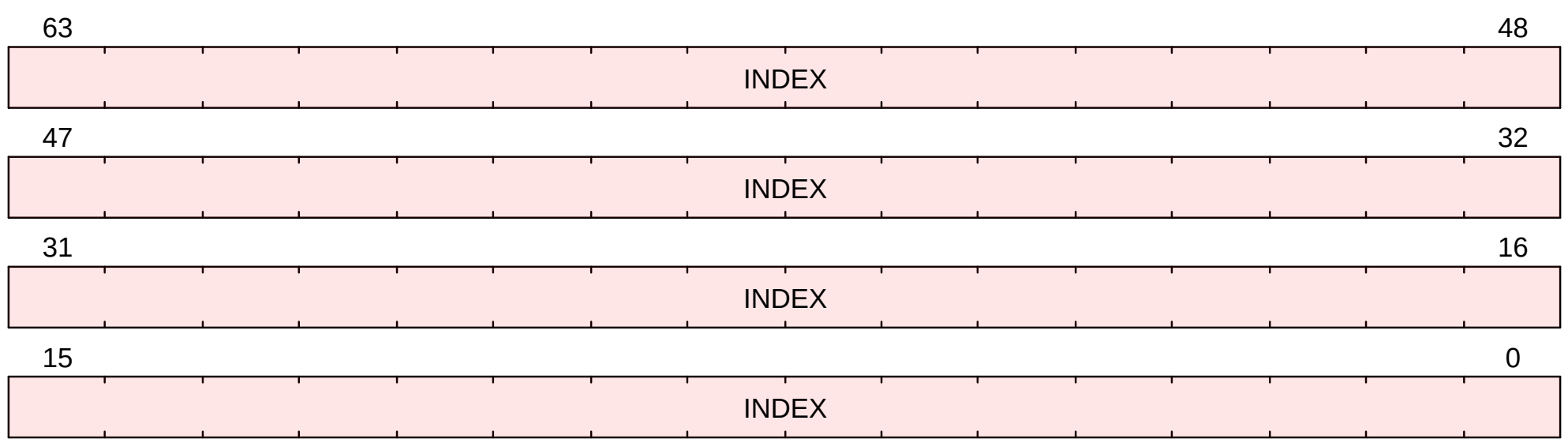


Figure 147. tselect Format when (priv_mode() == PrivilegeMode::M && CSR[misa].MXL == 1) || (priv_mode() == PrivilegeMode::S && CSR[mstatus].SXL == 1) || (priv_mode() == PrivilegeMode::VS && CSR[hstatus].VSXL == 1)

C.140.3. Field Summary

Nam e	Location	Type	Reset Value
tselec t.IND EX	63:0	RW	UNDEFINED_LEGAL

C.140.4. Fields

`tselect.INDEX` Field

Location:	63:0
Description:	Index value
Type:	RW
Reset value:	UNDEFINED_LEGAL

Appendix D: IDL Function Details

D.1. implemented? (generated)

Return true if the implementation supports *extension*.

Return Type	Boolean
Arguments	ExtensionName extension

D.2. implemented_version? (generated)

Return true if the implementation supports *extension* meeting 'version_requirement'.

Return Type	Boolean
Arguments	ExtensionName extension, String version_requirement

D.3. implemented_csr? (generated)

Return true if csr_addr is an implemented CSR

Return Type	Boolean
Arguments	Bits<12> csr_addr

D.4. direct_csr_lookup (generated)

Return CSR info for a CSR with direct address csr_addr.

If no CSR exists, <return_value>.valid == false

Return Type	Csr
Arguments	Bits<12> csr_addr

D.5. indirect_csr_lookup (generated)

Return CSR info for a CSR with indirect address csr_addr at window slot window_slot.

If no CSR exists, <return_value>.valid == false

Return Type	Csr
Arguments	Bits<MXLEN> csr_addr, Bits<4> window_slot

D.6. csr_hw_read (generated)

Returns the raw value of csr

Return Type	Bits
Arguments	Csr csr

D.7. csr_sw_read (generated)

Returns the result of CSR[csr].sw_read(); i.e., the software view of the register

Return Type	Bits
Arguments	Csr csr

D.8. csr_sw_write (generated)

Writes value to csr, applying an WARL transformations first.

Uses the sw_write(...) functions of CSR field definitions.

Return Type	void
Arguments	Csr csr, Bits<MXLEN> value

D.9. unpredictable (builtin)

Indicate that the hart has reached a state that is unpredictable because the RISC-V spec allows multiple behaviors. Generally, this will be a fatal condition to any emulation, since it is unclear what to do next.

The single argument *why* is a string describing why the hart entered an unpredictable state.

Return Type	void
Arguments	String why

D.10. unreachable (builtin)

Indicate that the IDL line should be unreachable.

If this function is called, it represents a bug in the IDL code.

Return Type	void
Arguments	None

D.11. read_hpm_counter (builtin)

Returns the value of hpmcounterN.

N must be between 3..31.

hpmcounterN must be implemented.

Return Type	Bits
Arguments	Bits<5> n

D.12. hartid (builtin)

Returns the value for [mhartid](#) as seen by this hart.

Must obey the rules of the priv spec:

The [mhartid](#) CSR is an MXLEN-bit read-only register containing the integer ID of the hardware thread running the code. This register must be readable in any implementation. Hart IDs might not necessarily be numbered

contiguously in a multiprocessor system, but at least one hart must have a hart ID of zero. Hart IDs must be unique within the execution environment.

Return Type	XReg
Arguments	None

D.13. read_mcycle (builtin)

Return the current value of the cycle counter.

Return Type	Bits
Arguments	None

D.14. read_mtime (builtin)

Return the current value of the real time device.

Return Type	Bits
Arguments	None

D.15. sw_write_mcycle (builtin)

Given a *value* that software is trying to write into mcycle, perform the write and return the value that will actually be written.

Return Type	Bits
Arguments	Bits<64> value

D.16. cache_block_zero (builtin)

Zero the cache block at the given physical address.

The cache block may be zeroed using 1 or more writes.

A cache-block-sized region is zeroed regardless of whether or not the memory is in a cacheable PMA region.

Return Type	void
Arguments	XReg cache_block_physical_address

D.17. eei_ecall_from_m (builtin)

When TRAP_ON_ECALL_FROM_M is false, this function will be called to emulate the EEI handling of ECALL-from-M.

If TRAP_ON_ECALL_FROM_M is true, this function will never be called, and does not need to be provided (if pruning is applied to IDL).

Return Type	void
Arguments	None

D.18. eei_ecall_from_s (builtin)

When TRAP_ON_ECALL_FROM_S is false, this function will be called to emulate the EEI handling of ECALL-from-S.

If TRAP_ON_ECALL_FROM_S is true, this function will never be called, and does not need to be provided (if pruning is applied to IDL).

Return Type	void
Arguments	None

D.19. eei_ecall_from_u (builtin)

When TRAP_ON_ECALL_FROM_U is false, this function will be called to emulate the EEI handling of ECALL-from-U.

If TRAP_ON_ECALL_FROM_U is true, this function will never be called, and does not need to be provided (if pruning is applied to IDL).

Return Type	void
Arguments	None

D.20. eei_ecall_from_vs (builtin)

When TRAP_ON_ECALL_FROM_VS is false, this function will be called to emulate the EEI handling of ECALL-from-VS.

If TRAP_ON_ECALL_FROM_VS is true, this function will never be called, and does not need to be provided (if pruning is applied to IDL).

Return Type	void
Arguments	None

D.21. eei_ebreak (builtin)

When TRAP_ON_EBREAK is false, this function will be called to emulate the EEI handling of EBREAK

If TRAP_ON_EBREAK is true, this function will never be called, and does not need to be provided (if pruning is applied to IDL).

Return Type	void
Arguments	None

D.22. memory_model_acquire (builtin)

Perform an acquire; that is, ensure that no subsequent operation in program order appears to an external observer to occur after the operation calling this function.

Return Type	void
Arguments	None

D.23. memory_model_release (builtin)

Perform a release; that is, ensure that no prior store in program order can be observed external to this hart after this function returns.

Return Type	void
Arguments	None

D.24. assert (builtin)

Assert that a condition is true. Failure represents an error in the IDL model.

Return Type	void
Arguments	Boolean test, String message

D.25. notify_mode_change (builtin)

Called whenever the privilege mode changes. Downstream tools can use this to hook events.

Return Type	void
Arguments	PrivilegeMode new_mode, PrivilegeMode old_mode

D.26. abort_current_instruction (builtin)

Abort the current instruction, and start refetching from \$pc.

Return Type	void
Arguments	None

D.27. ebreak (builtin)

Raise an **Environment Break** exception, returning control to the debug environment.

Return Type	void
Arguments	None

D.28. prefetch_instruction (builtin)

Hint to prefetch a block containing virtual_address for an upcoming fetch.

Return Type	void
Arguments	XReg virtual_address

D.29. prefetch_read (builtin)

Hint to prefetch a block containing virtual_address for an upcoming load.

Return Type	void
Arguments	XReg virtual_address

D.30. prefetch_write (builtin)

Hint to prefetch a block containing virtual_address for an upcoming store.

Return Type	void
Arguments	XReg virtual_address

D.31. fence (builtin)

Execute a memory ordering fence.(according to the FENCE instruction).

Return Type	void

Arguments	Boolean pi, Boolean pr, Boolean po, Boolean pw, Boolean si, Boolean sr, Boolean so, Boolean sw

D.32. fence_tso (builtin)

Execute a TSO memory ordering fence.(according to the FENCE instruction).

Return Type	void
Arguments	None

D.33. ifence (builtin)

Execute a memory ordering instruction fence (according to FENCE.I).

Return Type	void
Arguments	None

D.34. pause (builtin)

Pause hart retirement for a implementation-defined period of time, which may be zero.

See [Zihintpause](#) for more.

Return Type	void
Arguments	None

D.35. pow (generated)

Return **value** to the power **exponent**.

Return Type	XReg
Arguments	XReg value, XReg exponent

D.36. maybe_cache_translation (generated)

Given a translation result, potentially cache the result for later use. This function models a TLB fill operation. A valid implementation does nothing.

Return Type	void
Arguments	XReg vaddr, MemoryOperation op, TranslationResult result

D.37. cached_translation (generated)

Possibly returns a cached translation result matching vaddr.

CachedTranslationResult contains a Boolean 'valid' field. If valid, 'result' is a usable translation. Otherwise, the cache lookup failed.

Return Type	CachedTranslationResult
Arguments	XReg vaddr, MemoryOperation op

D.38. order_pgtbl_writes_before_vmafence (builtin)

Orders all writes prior to this call in global memory order that affect a page table in the set identified by `order_type` before any subsequent `sfence.vma/hfence.vma/sinval.vma/hinval.gvma/hinval.vvma` in program order.

Performs the ordering function of `SFENCE.VMA/HFENCE.[GV]VMA/SFENCE.W.INVALID`.

A valid implementation does nothing if address caching is not used.

Return Type	void
Arguments	VmaOrderType order_type

D.39. order_pgtbl_reads_after_vmafence (builtin)

Orders all reads after to this call in global memory order to a page table in the set identified by `order_type` after any prior `sfence.vma/hfence.vma/sinval.vma/hinval.gvma/hinval.vvma` in program order.

Performs the ordering function of `SFENCE.VMA/HFENCE.[GV]VMA/SFENCE.INVALID.IR`.

A valid implementation does nothing if address caching is not used.

Return Type	void
Arguments	VmaOrderType order_type

D.40. invalidate_translations (generated)

Locally invalidate the cached S-mode/VS-mode/G-stage address translations contained in the set identified by `inval_type`.

A valid implementation does nothing if address caching is not used.

Return Type	void
Arguments	VmaOrderType inval_type

D.41. read_physical_memory

Read from physical memory.

Return Type	Bits<len>
Arguments	XReg paddr

```
if (len == 8) {
    return read_physical_memory_8(paddr);
} else if (len == 16) {
    return read_physical_memory_16(paddr);
} else if (len == 32) {
    return read_physical_memory_32(paddr);
} else if (len == 64) {
    return read_physical_memory_64(paddr);
} else {
    assert(false, "Invalid len");
}
```

D.42. read_physical_memory_8 (builtin)

Read a byte from physical memory.

Return Type	Bits ⁸
Arguments	XReg paddr

D.43. read_physical_memory_16 (builtin)

Read two bytes from physical memory.

Return Type	Bits ¹⁶
Arguments	XReg paddr

D.44. read_physical_memory_32 (builtin)

Read four bytes from physical memory.

Return Type	Bits
Arguments	XReg paddr

D.45. read_physical_memory_64 (builtin)

Read eight bytes from physical memory.

Return Type	Bits
Arguments	XReg paddr

D.46. write_physical_memory

Write to physical memory.

Return Type	void
Arguments	XReg paddr, Bits<len> value

```

if (len == 8) {
    write_physical_memory_8(paddr, value);
} else if (len == 16) {
    write_physical_memory_16(paddr, value);
} else if (len == 32) {
    write_physical_memory_32(paddr, value);
} else if (len == 64) {
    write_physical_memory_64(paddr, value);
} else {
    assert(false, "Invalid len");
}

```

D.47. write_physical_memory_8 (builtin)

Write a byte to physical memory.

Return Type	void

Arguments	XReg paddr, Bits<8> value

D.48. write_physical_memory_16 (builtin)

Write two bytes to physical memory.

Return Type	void
Arguments	XReg paddr, Bits<16> value

D.49. write_physical_memory_32 (builtin)

Write four bytes to physical memory.

Return Type	void
Arguments	XReg paddr, Bits<32> value

D.50. write_physical_memory_64 (builtin)

Write eight bytes to physical memory.

Return Type	void
Arguments	XReg paddr, Bits<64> value

D.51. wfi (builtin)

Wait-for-interrupt: hint that the processor should enter a low power state until the next interrupt.

A valid implementation is a no-op.

The model will advance the PC; this function does not need to.

Return Type	void
Arguments	None

D.52. pma_applies? (builtin)

Checks if *attr* is applied to the entire physical address region between [paddr, paddr + len) based on static PMA attributes.

Return Type	Boolean
Arguments	PmaAttribute attr, Bits<PHYS_ADDR_WIDTH> paddr, U32 len

D.53. atomic_check_then_write_32 (builtin)

Atomically:

- Reads 32-bits from paddr
- Compares the read value to compare_value
- Writes write_value to paddr **if** the comparison was bitwise-equal

returns true if the write occurs, and false otherwise

Preconditions:

- `paddr` will be aligned to 32-bits

Return Type	Boolean	
Arguments	Bits<PHYS_ADDR_WIDTH> <code>paddr</code> , Bits<32> <code>write_value</code>	<code>compare_value</code> , Bits<32>

D.54. `atomic_check_then_write_64` (builtin)

Atomically:

- Reads 64-bits from `paddr`
- Compares the read value to `compare_value`
- Writes `write_value` to `paddr` **if** the comparison was bitwise-equal

returns true if the write occurs, and false otherwise

Preconditions:

- `paddr` will be aligned to 64-bits

Return Type	Boolean	
Arguments	Bits<PHYS_ADDR_WIDTH> <code>paddr</code> , Bits<64> <code>write_value</code>	<code>compare_value</code> , Bits<64>

D.55. `atomically_set_pte_a` (builtin)

Atomically:

- Reads the *pte_len* value at *pte_addr*
 - If the read value does not exactly equal `pte_value`, returns false
- Sets the 'A' bit and writes the result to *pte_addr*
- return true

Preconditions:

- `pte_addr` will be aligned to 64-bits

Return Type	Boolean	
Arguments	Bits<PHYS_ADDR_WIDTH> <code>pte_addr</code> , Bits<MXLEN> <code>pte_len</code>	<code>pte_value</code> , U32

D.56. `atomically_set_pte_a_d` (builtin)

Atomically:

- Reads the *pte_len* value at *pte_addr*
 - If the read value does not exactly equal `pte_value`, returns false
- Sets the 'A' and 'D' bits and writes the result to *pte_addr*
- return true

Preconditions:

- `pte_addr` will be aligned to 64-bits

Return Type	Boolean	

Arguments	Bits<PHYS_ADDR_WIDTH> pte_addr, Bits<MXLEN> pte_value, U32 pte_len

D.57. atomic_read_modify_write_32 (builtin)

Atomically read-modify-write 32-bits starting at phys_address using value and op.

Return the original (unmodified) read value.

All access checks/alignment checks/etc. should be done before calling this function; it’s assumed the RMW is OK to proceed.

Return Type	Bits
Arguments	Bits<PHYS_ADDR_WIDTH> phys_addr, Bits<32> value, AmoOperation op

D.58. atomic_read_modify_write_64 (builtin)

Atomically read-modify-write 64-bits starting at phys_address using value and op.

Return the original (unmodified) read value.

All access checks/alignment checks/etc. should be done before calling this function; it’s assumed the RMW is OK to proceed.

Return Type	Bits
Arguments	Bits<PHYS_ADDR_WIDTH> phys_addr, Bits<64> value, AmoOperation op

D.59. set_external_interrupt

Set an external interrupt targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```

if (target_mode == PrivilegeMode::M) {
    CSR[mip].MEIP = 1'b1;
} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    pending_smode_external_interrupt = true;
} else if ((CSR[misa].H == 1'b1) && (target_mode == PrivilegeMode::VS)) {
    CSR[mip].VSEIP = 1'b1;
} else {
    assert(false, "Invalid target_mode");
}
refresh_pending_interrupts();

```

D.60. clear_external_interrupt

Clear an external interrupt targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```

if (target_mode == PrivilegeMode::M) {
    CSR[mip].MEIP = 1'b0;
}

```



```

} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    pending_smode_external_interrupt = false;
} else if ((CSR[misa].H == 1'b1) && (target_mode == PrivilegeMode::VS)) {
    CSR[mip].VSEIP = 1'b0;
} else {
    assert(false, "Invalid target_mode");
}
refresh_pending_interrupts();

```

D.61. set_software_interrupt

Set a software interrupt targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```

if (target_mode == PrivilegeMode::M) {
    CSR[mip].MSIP = 1'b1;
} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    CSR[mip].SSIP = 1'b1;
} else {
    assert(false, "Invalid target_mode");
}
refresh_pending_interrupts();

```

D.62. clear_software_interrupt

Clear a software interrupt targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```

if (target_mode == PrivilegeMode::M) {
    CSR[mip].MSIP = 1'b0;
} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    CSR[mip].SSIP = 1'b0;
} else {
    assert(false, "Invalid target_mode");
}
refresh_pending_interrupts();

```

D.63. set_timer_interrupt

Set a timer interrupt from the platform targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```

if (target_mode == PrivilegeMode::M) {
    CSR[mip].MTIP = 1'b1;
} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    CSR[mip].STIP = 1'b1;
} else if ((CSR[misa].H == 1'b1) && (target_mode == PrivilegeMode::VS)) {
    pending_vsmode_timer_interrupt = true;
} else {
    assert(false, "Invalid target_mode");
}

```

```
refresh_pending_interrupts();
```

D.64. clear_timer_interrupt

Set a timer interrupt from the platform targeting target_mode

Return Type	void
Arguments	PrivilegeMode target_mode

```
if (target_mode == PrivilegeMode::M) {
    CSR[mip].MTIP = 1'b0;
} else if ((CSR[misa].S == 1'b1) && (target_mode == PrivilegeMode::S)) {
    CSR[mip].STIP = 1'b0;
} else if ((CSR[misa].H == 1'b1) && (target_mode == PrivilegeMode::VS)) {
    pending_vsmode_timer_interrupt = false;
} else {
    assert(false, "Invalid target_mode");
}
refresh_pending_interrupts();
```

D.65. refresh_pending_interrupts

refreshes the calculation of a pending interrupt

needs to be called after any state update that could change a pending interrupt. This includes: - CSR[mip] - CSR[mie] - CSR[mstatus].MIE - CSR[mstatus].SIE - CSR[vsstatus].SIE - CSR[mideleg] - CSR[sideleg] - CSR[hideleg] - CSR[hvip] - CSR[hgeip] - CSR[hgeie] - mode changes

Return Type	void
Arguments	None

```
Bits<MXLEN> pending_ints = CSR[CSR[mip]].sw_read() & $bits(CSR[CSR[mie]]);
if (pending_ints == 0) {
    pending_and_enabled_interrupts = 0;
    return ;
}
Boolean HAS_MIDELEG = implemented_version?(ExtensionName::S, "<= 1.9.1") || (implemented_version?(ExtensionName::S, "> 1.9.1") &&
    implemented_version?(ExtensionName::Sm, "> 1.9.1"));
Bits<MXLEN> mmode_enabled_ints = mode() == PrivilegeMode::M && (CSR[mstatus].MIE == 1'b0 ? 0 : ($bits(CSR[CSR[mie]])) &
    (HAS_MIDELEG ? ~$bits(CSR[CSR[mideleg]]) : ~MXLEN'0));
Bits<MXLEN> mmode_pending_and_enabled = pending_ints & mmode_enabled_ints;
if (mmode_pending_and_enabled != 0) {
    pending_and_enabled_interrupts = mmode_pending_and_enabled;
    return ;
}
if (CSR[misa].S == 1'b1) {
    Bits<MXLEN> smode_enabled_ints = mode() == PrivilegeMode::M || (CSR[mstatus].SIE == 1'b0 ? 0 : $bits(CSR[CSR[mie]])) &
    ($bits(CSR[CSR[mideleg]]));
    Bits<MXLEN> smode_pending_and_enabled = pending_ints & smode_enabled_ints;
    if (smode_pending_and_enabled != 0) {
        pending_and_enabled_interrupts = smode_pending_and_enabled;
        return ;
    }
}
pending_and_enabled_interrupts = 0;
```

D.66. highest_priority_interrupt

Given a bitmask of interrupts in the format of MIE/MIP, return the highest priority interrupt code that is set

Interrupt priority is: MEI, MSI, MTI, SEI, SSI, STI, SGEI, VSEI, VSSI, VSTI, LCOFI

Return Type	InterruptCode

Arguments	Bits<MXLEN> int_mask

```

if (int_mask[$bits(InterruptCode::MachineExternal)] == 1'b1) {
    return InterruptCode::MachineExternal;
} else if (int_mask[$bits(InterruptCode::MachineSoftware)] == 1'b1) {
    return InterruptCode::MachineSoftware;
} else if (int_mask[$bits(InterruptCode::MachineTimer)] == 1'b1) {
    return InterruptCode::MachineTimer;
} else if (CSR[misa].S == 1'b1) {
    if (int_mask[$bits(InterruptCode::SupervisorExternal)] == 1'b1) {
        return InterruptCode::SupervisorExternal;
    } else if (int_mask[$bits(InterruptCode::SupervisorSoftware)] == 1'b1) {
        return InterruptCode::SupervisorSoftware;
    } else if (int_mask[$bits(InterruptCode::SupervisorTimer)] == 1'b1) {
        return InterruptCode::SupervisorTimer;
    }
} else if (implemented?(ExtensionName::Sscofpmf)) {
    if (int_mask[$bits(InterruptCode::LocalCounterOverflow)] == 1'b1) {
        return InterruptCode::LocalCounterOverflow;
    }
}
}
assert(false, "There is no valid interrupt");

```

D.67. choose_interrupt

Return the highest priority interrupt that is both pending and enabled and the mode it will be taken in

Return Type	InterruptCode, PrivilegeMode
Arguments	None

```

InterruptCode chosen;
Boolean HAS_MIDELEG = implemented_version?(ExtensionName::S, "<= 1.9.1") || (implemented_version?(ExtensionName::S, "> 1.9.1") &&
implemented_version?(ExtensionName::Sm, "> 1.9.1"));
Bits<MXLEN> mmode_pending_and_enabled = pending_and_enabled_interrupts & ~(HAS_MIDELEG ? $bits(CSR[CSR[mideleg]]) : MXLEN'0);
if (mmode_pending_and_enabled != 0) {
    assert((mode() != PrivilegeMode::M) || (CSR[mstatus].MIE == 1'b1), "M-mode interrupts are not enabled");
    chosen = highest_priotity_interrupt(mmode_pending_and_enabled);
} else if (CSR[misa].S == 1'b1) {
    Bits<MXLEN> smode_pending_and_enabled = (pending_and_enabled_interrupts & $bits(CSR[CSR[mideleg]]));
    if (smode_pending_and_enabled != 0) {
        assert((mode() == PrivilegeMode::U) || (mode() == PrivilegeMode::VU) || (mode() == PrivilegeMode::VS) || (mode() ==
PrivilegeMode::S) && (CSR[mstatus].SIE == 1'b1), "S-mode interrupt can't be triggered");
        chosen = highest_priority_interrupt(smode_pending_and_enabled);
    }
}
assert($bits(chosen) != 0, "Didn't pick interrupt?");
PrivilegeMode to_mode;
Bits<MXLEN> chosen_mask = (MXLEN'1 << $bits(chosen));
if (((HAS_MIDELEG ? $bits(CSR[CSR[mideleg]]) : MXLEN'0) & chosen_mask) == 0) {
    to_mode = PrivilegeMode::M;
} else {
    if (CSR[misa].S == 1'b1) {
        to_mode = PrivilegeMode::S;
    } else {
        to_mode = PrivilegeMode::U;
    }
}
return chosen, to_mode;

```

D.68. take_interrupt

Take (adjust CSRs and set PC to handler) the highest priority interrupt that is both pending and enabled

Return Type	void

Arguments	None

```

PrivilegeMode to_mode;
InterruptCode code;
(code, to_mode = choose_interrupt());
if (to_mode == PrivilegeMode::M) {
    CSR[mepc].PC = $pc;
    CSR[mstatus].MPP = $bits(mode())[1:0];
    if (CSR[misa].H == 1'b1) {
        if (MXLEN == 64) {
            CSR[mstatus].MPV = $bits(mode())[2];
        } else {
            CSR[mstatush].MPV = $bits(mode())[2];
        }
        CSR[mtval2].VALUE = 0;
        CSR[mtinst].VALUE = 0;
    }
    CSR[mcause].CODE = $bits(code);
    CSR[mcause].INT = 1'b1;
    CSR[mtval].VALUE = 0;
    if (CSR[mtvec].MODE == 0) {
        $pc = {CSR[mtvec].BASE, 2'b00};
    } else if (CSR[mtvec].MODE == 1'b1) {
        $pc = {CSR[mtvec].BASE, 2'b00} + ($bits(code) * 4);
    }
} else if ((CSR[misa].S == 1'b1) && (to_mode == PrivilegeMode::S)) {
    CSR[sepc].PC = $pc;
    CSR[mstatus].SPP = $bits(mode())[0];
    if (CSR[misa].H == 1'b1) {
        CSR[hstatus].SPV = $bits(mode())[2];
    }
    CSR[scause].CODE = $bits(code);
    CSR[scause].INT = 1'b1;
    CSR[stval].VALUE = 0;
    if (CSR[stvec].MODE == 0) {
        $pc = {CSR[stvec].BASE, 2'b00};
    } else if (CSR[stvec].MODE == 1'b1) {
        $pc = {CSR[stvec].BASE, 2'b00} + ($bits(code) * 4);
    }
} else if ((CSR[misa].H == 1'b1) && (to_mode == PrivilegeMode::VS)) {
    CSR[vsepc].PC = $pc;
    CSR[vsstatus].SPP = $bits(mode())[0];
    CSR[vscause].CODE = $bits(code);
    CSR[vscause].INT = 1'b1;
    CSR[vstval].VALUE = 0;
    if (CSR[vstvec].MODE == 0) {
        $pc = {CSR[vstvec].BASE, 2'b00};
    } else if (CSR[vstvec].MODE == 1'b1) {
        $pc = {CSR[vstvec].BASE, 2'b00} + ($bits(code) * 4);
    }
}
set_mode_no_refresh(to_mode);

```

D.69. fetch_memory_aligned_16

Fetch 16 bits from virtual memory using a known aligned address.

Return Type	Bits ¹⁶
Arguments	XReg virtual_address

```

TranslationResult result;
if (CSR[misa].S == 1) {
    result = translate(virtual_address, MemoryOperation::Fetch, mode(), virtual_address);
} else {
    result.paddr = virtual_address;
}
access_check(result.paddr, 16, virtual_address, MemoryOperation::Fetch, ExceptionCode::InstructionAccessFault, mode());

```

```
return read_physical_memory<16>(result.paddr);
```

D.70. fetch_memory_aligned_32

Fetch 32 bits from virtual memory using a known aligned address.

Return Type	Bits
Arguments	XReg virtual_address

```
TranslationResult result;
if (CSR[misa].S == 1) {
    result = translate(virtual_address, MemoryOperation::Fetch, mode(), virtual_address);
} else {
    result.paddr = virtual_address;
}
access_check(result.paddr, 32, virtual_address, MemoryOperation::Fetch, ExceptionCode::InstructionAccessFault, mode());
return read_physical_memory<32>(result.paddr);
```

D.71. power_of_2?

Returns true if value is a power of two, false otherwise

Return Type	Boolean
Arguments	Bits<N> value

```
return (value != 0) && value & (value - 1 == 0);
```

D.72. has_virt_mem?

Returns true if some virtual memory translation (Sv*) is supported in the config.

Return Type	Boolean
Arguments	None

```
return implemented?(ExtensionName::Sv32) || implemented?(ExtensionName::Sv39) || implemented?(ExtensionName::Sv48) ||
implemented?(ExtensionName::Sv57);
```

D.73. max_va_size

Returns the largest possible Virtual Address width in any supported translation mode.

The max VA is determined by physical address size when in M mode or S-mode with Bare translation. Otherwise, max VA is the size of a virtual address in the largest supported Sv* mode.

Return the largest that applies.

Return Type	Bits⑧
Arguments	None

```
Bits<8> translated_va_size = 0;
if (implemented?(ExtensionName::Sv57)) {
    translated_va_size = 57;
} else if (implemented?(ExtensionName::Sv48)) {
    translated_va_size = 48;
} else if (implemented?(ExtensionName::Sv39)) {
    translated_va_size = 39;
```

```

} else if (implemented?(ExtensionName::Sv32)) {
    translated_va_size = 32;
}
if (PHYS_ADDR_WIDTH > translated_va_size) {
    if (PHYS_ADDR_WIDTH > MXLEN) {
        return MXLEN;
    } else {
        return PHYS_ADDR_WIDTH;
    }
} else {
    return translated_va_size;
}

```

D.74. highest_set_bit

Returns the position of the highest (nearest MSB) bit that is '1', or -1 if value is zero.

Return Type	Bits③
Arguments	XReg value

```

for (Bits<8> i = xlen() - 1; i >= 0; i--) {
    if (value[i] == 1) {
        return i;
    }
}
return -'sd1;

```

D.75. lowest_set_bit

Returns the position of the lowest (nearest LSB) bit that is '1', or XLEN if value is zero.

Return Type	Bits③
Arguments	XReg value

```

for (Bits<8> i = 0; i < xlen(); i++) {
    if (value[i] == 1) {
        return i;
    }
}
return xlen();

```

D.76. bit_length

Returns the minimum number of bits needed to represent value.

Only works on unsigned values.

The value 0 returns 1.

Return Type	XReg
Arguments	XReg value

```

for (XReg i = 63; i > 0; i--) {
    if (value[i] == 1) {
        return i;
    }
}
return 1;

```

D.77. count_leading_zeros

Returns the number of leading 0 bits before the most-significant 1 bit of value, or N if value is zero.

Return Type	Bits<bit_length(N)>
Arguments	Bits<N> value

```
for (U32 i = 0; i < N; i++) {
    if (value[N - 1 - i] == 1) {
        return i;
    }
}
return N;
```

D.78. sext

Sign extend **value** starting at **first_extended_bit**.

Bits [**XLEN-1**:**`first\_extended\_bit`**] of the return value should get the value of bit (**first_extended bit - 1**).

Return Type	XReg
Arguments	XReg value, XReg first_extended_bit

```
if (first_extended_bit == MXLEN) {
    return value;
} else {
    Bits<1> sign = value[first_extended_bit - 1];
    for (U32 i = MXLEN - 1; i >= first_extended_bit; i--) {
        value[i] = sign;
    }
    return value;
}
```

D.79. is_naturally_aligned

Checks if value is naturally aligned to N bits.

Return Type	Boolean
Arguments	XReg value

```
return true if (N == 8);
XReg Mask = (N / 8) - 1;
return (value & ~Mask) == value;
```

D.80. in_naturally_aligned_region?

Checks if a length-bit access starting at address lies entirely within an N-bit naturally-aligned region.

Return Type	Boolean
Arguments	XReg address, U32 length

```
XReg Mask = (N / 8) - 1;
return (address & ~Mask) == ((address + length - 1) & ~Mask);
```

D.81. contains?

Given a *region* defined by region_start, region_size, determine if a *target* defined by target_start, target_size is completely contained with the region.

Return Type	Boolean
Arguments	XReg region_start, U32 region_size, XReg target_start, U32 target_size

```
return target_start >= region_start && (target_start + target_size) <= (region_start + region_size);
```

D.82. set_fp_flag

Add flag to the sticky flags bits in CSR[fcsr]

Return Type	void
Arguments	FpFlag flag

```
if (flag == FpFlag::NX) {
    CSR[fcsr].NX = 1;
} else if (flag == FpFlag::UF) {
    CSR[fcsr].UF = 1;
} else if (flag == FpFlag::OF) {
    CSR[fcsr].OF = 1;
} else if (flag == FpFlag::DZ) {
    CSR[fcsr].DZ = 1;
} else if (flag == FpFlag::NV) {
    CSR[fcsr].NV = 1;
}
```

D.83. rm_to_mode

Convert rm to a RoundingMode.

encoding is the full encoding of the instruction rm comes from.

Will raise an IllegalInstruction exception if rm is a reserved encoding.

Return Type	RoundingMode
Arguments	Bits<3> rm, Bits<32> encoding

```
if (rm == $bits(RoundingMode::RNE)) {
    return RoundingMode::RNE;
} else if (rm == $bits(RoundingMode::RTZ)) {
    return RoundingMode::RTZ;
} else if (rm == $bits(RoundingMode::RDN)) {
    return RoundingMode::RDN;
} else if (rm == $bits(RoundingMode::RUP)) {
    return RoundingMode::RUP;
} else if (rm == $bits(RoundingMode::RMM)) {
    return RoundingMode::RMM;
} else if (rm == $bits(RoundingMode::DYN)) {
    return $enum(RoundingMode, CSR[fcsr].FRM);
} else {
    raise(ExceptionCode::IllegalInstruction, mode(), encoding);
}
```

D.84. mark_f_state_dirty

Potentially updates mstatus.FS to the Dirty (3) state, depending on configuration settings.

Return Type	void
Arguments	None

```
if (HW_MSTATUS_FS_DIRTY_UPDATE == "precise") {
    CSR[mstatus].FS = 3;
} else if (HW_MSTATUS_FS_DIRTY_UPDATE == "imprecise") {
    unpredictable("The hart may or may not update mstatus.FS now");
}
```

D.85. nan_box

Produces a properly NaN-boxed floating-point value from a floating-point value of smaller size by adding all 1’s to the upper bits.

Return Type	Bits<TO_SIZE>
Arguments	Bits<FROM_SIZE> from_value

```
assert(FROM_SIZE < TO_SIZE, "Bad template arguments; FROM_SIZE must be less than TO_SIZE");
return {{TO_SIZE - FROM_SIZE{1'b1}}, from_value};
```

D.86. check_f_ok

Checks if instructions from the F extension can be executed, and, if not, raise an exception.

Return Type	void
Arguments	Bits<INSTR_ENC_SIZE> encoding

```
if (MUTABLE_MISA_F && CSR[misa].F == 0) {
    raise(ExceptionCode::IllegalInstruction, mode(), encoding);
}
if (CSR[mstatus].FS == 0) {
    raise(ExceptionCode::IllegalInstruction, mode(), encoding);
}
```

D.87. is_sp_neg_inf?

Return true if sp_value is negative infinity.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return sp_value == SP_NEG_INF;
```

D.88. is_sp_pos_inf?

Return true if sp_value is positive infinity.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return sp_value == SP_POS_INF;
```

D.89. is_sp_neg_norm?

Returns true if sp_value is a negative normal number.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return (sp_value[31] == 1) && (sp_value[30:23] != 0b11111111) && !((sp_value[30:23] == 0b00000000) && sp_value[22:0] != 0);
```

D.90. is_sp_pos_norm?

Returns true if sp_value is a positive normal number.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return (sp_value[31] == 0) && (sp_value[30:23] != 0b11111111) && !((sp_value[30:23] == 0b00000000) && sp_value[22:0] != 0);
```

D.91. is_sp_neg_subnorm?

Returns true if sp_value is a negative subnormal number.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return (sp_value[31] == 1) && (sp_value[30:23] == 0) && (sp_value[22:0] != 0);
```

D.92. is_sp_pos_subnorm?

Returns true if sp_value is a positive subnormal number.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return (sp_value[31] == 0) && (sp_value[30:23] == 0) && (sp_value[22:0] != 0);
```

D.93. is_sp_neg_zero?

Returns true if sp_value is negative zero.

Return Type	Boolean
Arguments	Bits<32> sp_value

```
return sp_value == SP_NEG_ZERO;
```


D.94. is_sp_pos_zero?

Returns true if sp_value is positive zero.

Return Type	Boolean
Arguments	Bits<32> sp_value
<pre>return sp_value == SP_POS_ZERO;</pre>	

D.95. is_sp_nan?

Returns true if sp_value is a NaN (quiet or signaling)

Return Type	Boolean
Arguments	Bits<32> sp_value
<pre>return (sp_value[30:23] == 0b11111111) && (sp_value[22:0] != 0);</pre>	

D.96. is_sp_signaling_nan?

Returns true if sp_value is a signaling NaN

Return Type	Boolean
Arguments	Bits<32> sp_value
<pre>return (sp_value[30:23] == 0b11111111) && (sp_value[22] == 0) && (sp_value[21:0] != 0);</pre>	

D.97. is_sp_quiet_nan?

Returns true if sp_value is a quiet NaN

Return Type	Boolean
Arguments	Bits<32> sp_value
<pre>return (sp_value[30:23] == 0b11111111) && (sp_value[22] == 1);</pre>	

D.98. softfloat_shiftRightJam32

Shifts a right by the number of bits given in dist, which must not be zero. If any nonzero bits are shifted off, they are "jammed" into the least-significant bit of the shifted value by setting the least-significant bit to 1. This shifted-and-jammed value is returned. The value of dist can be arbitrarily large. In particular, if dist is greater than 32, the result will be either 0 or 1, depending on whether a is zero or nonzero.

Return Type	Bits
Arguments	Bits<32> a, Bits<32> dist
<pre>return (dist < 31) ? a >> dist (a << (-dist & 31 != 0) ? 1 : 0) : ((a != 0) ? 1 : 0);</pre>	

D.99. softfloat_shiftRightJam64

Shifts a right by the number of bits given in `dist`, which must not be zero. If any nonzero bits are shifted off, they are "jammed" into the least-significant bit of the shifted value by setting the least-significant bit to 1. This shifted-and-jammed value is returned.

The value of '`dist`' can be arbitrarily large. In particular, if `dist` is greater than 64, the result will be either 0 or 1, depending on whether `a` is zero or nonzero.

Return Type	Bits
Arguments	Bits<64> a, Bits<32> dist

```
return (dist < 63) ? a >> dist | (a << (-dist & 63 != 0) ? 1 : 0) : ((a != 0) ? 1 : 0);
```

D.100. softfloat_roundToI32

Round to signed 32-bit integer, using `rounding_mode`

Return Type	Bits
Arguments	Bits<1> sign, Bits<64> sig, RoundingMode roundingMode

```
Bits<16> roundIncrement = 0x800;
if ((roundingMode != RoundingMode::RMM) && (roundingMode != RoundingMode::RNE)) {
    roundIncrement = 0;
    if (sign == 1 ? (roundingMode == RoundingMode::RDN) : (roundingMode == RoundingMode::RUP)) {
        roundIncrement = 0xFFF;
    }
}
Bits<16> roundBits = sig & 0xFFF;
sig = sig + roundIncrement;
if ((sig & 0xFFFFF00000000000) != 0) {
    set_fp_flag(FpFlag::NV);
    return sign == 1 ? WORD_NEG_OVERFLOW : WORD_POS_OVERFLOW;
}
Bits<32> sig32 = sig >> 12;
if ((roundBits == 0x800 && (roundingMode == RoundingMode::RNE))) {
    sig32 = sig32 & ~32'b1;
}
Bits<32> z = (sign == 1) ? -sig32 : sig32;
if ((z != 0) && $signed(z) < 's0) != (sign == 1) {
    set_fp_flag(FpFlag::NV);
    return sign == 1 ? WORD_NEG_OVERFLOW : WORD_POS_OVERFLOW;
}
if (roundBits != 0) {
    set_fp_flag(FpFlag::NX);
}
return z;
```

D.101. softfloat_roundToUI32

Round to unsigned 32-bit integer, using `rounding_mode`

Return Type	Bits
Arguments	Bits<1> sign, Bits<64> sig, RoundingMode roundingMode

```
Bits<16> roundIncrement = 0x800;
if ((roundingMode != RoundingMode::RMM) && (roundingMode != RoundingMode::RNE)) {
    roundIncrement = 0;
    if (sign == 1) {
        if (sig == 0) {
```

```
        return 0;
    }
    if (roundingMode == RoundingMode::RDN) {
        set_fp_flag(FpFlag::NV);
    }
} else {
    if (roundingMode == RoundingMode::RUP) {
        roundIncrement = 0xFFF;
    }
}
}
Bits<16> roundBits = sig & 0xFFF;
sig = sig + roundIncrement;
if ((sig & 0xFFFFF00000000000) != 0) {
    set_fp_flag(FpFlag::NV);
    return sign == 1 ? UI32_NEG_OVERFLOW : UI32_POS_OVERFLOW;
}
Bits<32> z = sig >> 12;
if ((roundBits == 0x800 && (roundingMode == RoundingMode::RNE))) {
    z = z & ~32'b1;
}
if ((z != 0) && (sign == 1)) {
    set_fp_flag(FpFlag::NV);
    return sign == 1 ? UI32_NEG_OVERFLOW : UI32_POS_OVERFLOW;
}
if (roundBits != 0) {
    set_fp_flag(FpFlag::NX);
}
return z;
```

D.102. packToF32UI

Pack components into a 32-bit value

Return Type	Bits
Arguments	Bits<1> sign, Bits<8> exp, Bits<23> sig

```
return {sign, exp, sig};
```

D.103. packToF16UI

Pack components into a 16-bit value

Return Type	Bits
Arguments	Bits<1> sign, Bits<5> exp, Bits<10> sig

```
return {sign, exp, sig};
```

D.104. softfloat_normSubnormalF16Sig

normalize subnormal half-precision value

Return Type	Bits<5>, Bits ¹⁰
Arguments	Bits<16> hp_value

```
Bits<8> shift_dist = count_leading_zeros<16>(hp_value);
return 1 - shift_dist, hp_value << shift_dist;
```

D.105. softfloat_roundPackToF32

Round FP value according to mdode and then pack it in IEEE format.

Return Type	Bits
Arguments	Bits<1> sign, Bits<8> exp, Bits<23> sig, RoundingMode mode

```
Bits<8> roundIncrement = 0x40;
if ((mode != RoundingMode::RNE) && (mode != RoundingMode::RMM)) {
    roundIncrement = (mode == sign != 0) ? RoundingMode::RDN : RoundingMode::RUP ? 0x7F : 0;
}
Bits<8> roundBits = sig & 0x7f;
if (0xFD <= exp) {
    if ($signed(exp) < 's0) {
        Boolean isTiny = ($signed(exp) < -8's1) || (sig + roundIncrement < 0x80000000);
        sig = softfloat_shiftRightJam32(sig, -exp);
        exp = 0;
        roundBits = sig & 0x7F;
        if (isTiny && (roundBits != 0)) {
            set_fp_flag(FpFlag::UF);
        }
    } else if ('shFD < $signed(exp) || (0x80000000 <= sig + roundIncrement)) {
        set_fp_flag(FpFlag::OF);
        set_fp_flag(FpFlag::NX);
        return packToF32UI(sign, 0xFF, 0) - roundIncrement == 0) ? 1 : 0);    } } sig = (sig + roundIncrement);
if (sig == 0) {
    exp = 0;
}
return packToF32UI(sign, exp, sig);
```

D.106. softfloat_normRoundPackToF32

Normalize, round, and pack into a 32-bit floating point value

Return Type	Bits
Arguments	Bits<1> sign, Bits<8> exp, Bits<23> sig, RoundingMode mode

```
Bits<8> shiftDist = count_leading_zeros<32>(sig) - 1;
exp = exp - shiftDist;
if ((7 <= shiftDist) && (exp < 0xFD)) {
    return packToF32UI(sign, (sig != 0) ? exp : 0, sig << (shiftDist - 7));
} else {
    return softfloat_roundPackToF32(sign, exp, sig << shiftDist, mode);
}
```

D.107. signF32UI

Extract sign-bit of a 32-bit floating point number

Return Type	Bits①
Arguments	Bits<32> a

```
return a[31];
```

D.108. expF32UI

Extract exponent of a 32-bit floating point number

Return Type	Bits⑧
Arguments	Bits<32> a

```
return a[30:23];
```

D.109. fracF32UI

Extract significand of a 32-bit floating point number

Return Type	Bits
Arguments	Bits<32> a

```
return a[22:0];
```

D.110. returnNonSignalingNaN

Returns a non-signalling NaN version of the floating-point number Does not modify the input

Return Type	U32
Arguments	U32 a

```
U32 a_copy = a;
a_copy[22] = 1'b1;
return a_copy;
```

D.111. returnMag

Returns magnitude of the given number Does not modify the input

Return Type	U32
Arguments	U32 a

```
U32 a_copy = a;
a_copy[31] = 1'b0;
return a_copy;
```

D.112. returnLargerMag

Returns the larger number between a and b by magnitude If either number is signaling NaN then that is made quiet

Return Type	U32
Arguments	U32 a, U32 b

```
U32 mag_a = returnMag(a);
U32 mag_b = returnMag(b);
U32 nonsig_a = returnNonSignalingNaN(a);
U32 nonsig_b = returnNonSignalingNaN(b);
if (mag_a < mag_b) {
```

```
    return nonsig_b;
}
if (mag_b < mag_a) {
    return nonsig_a;
}
return (nonsig_a < nonsig_b) ? nonsig_a : nonsig_b;
```

D.113. softfloat_propagateNaNF32UI

Interpreting 'a' and 'b' as the bit patterns of two 32-bit floating- | point values, at least one of which is a NaN, returns the bit pattern of | the combined NaN result. If either 'a' or 'b' has the pattern of a | signaling NaN, the invalid exception is raised.

Return Type	U32
Arguments	U32 a, U32 b

```
Boolean isSigNaN_a = is_sp_signaling_nan?(a);
Boolean isSigNaN_b = is_sp_signaling_nan?(b);
if (isSigNaN_a || isSigNaN_b) {
    set_fp_flag(FpFlag::NV);
}
return SP_CANONICAL_NAN;
```

D.114. softfloat_addMagsF32

Returns sum of the magnitudes of 2 floating point numbers

Return Type	U32
Arguments	U32 a, U32 b, RoundingMode mode

```
Bits<8> expA = expF32UI(a);
Bits<23> sigA = fracF32UI(a);
Bits<8> expB = expF32UI(b);
Bits<23> sigB = fracF32UI(b);
U32 sigZ;
U32 z;
Bits<1> signZ;
Bits<8> expZ;
Bits<8> expDiff = expA - expB;
if (expDiff == 8'd0) {
    if (expA == 8'd0) {
        z = a + b;
        return z;
    }
    if (expA == 8'hFF) {
        if ((sigA != 8'd0) || (sigB != 8'd0)) {
            return softfloat_propagateNaNF32UI(a, b);
        }
        return a;
    }
    signZ = signF32UI(a);
    expZ = expA;
    sigZ = 32'h01000000 + sigA + sigB;
    if (sigZ & 0x1) == 0) && (expZ < 8'hFE {
        sigZ = sigZ >> 1;
        return (32'h0 + (signZ << 31) + (expZ << 23) + sigZ);
    }
    sigZ = sigZ << 6;
} else {
    signZ = signF32UI(a);
    U32 sigA_32 = 32'h0 + (sigA << 6);
    U32 sigB_32 = 32'h0 + (sigA << 6);
    if (expDiff < 0) {
        if (expB == 8'hFF) {
            if (sigB != 0) {
```



```

        return softfloat_propagateNaNF32UI(a, b);
    }
    return packToF32UI(signZ, 8'hFF, 23'h0);
}
expZ = expB;
sigA_32 = (expA == 0) ? 2 * sigA_32 : (sigA_32 + 0x20000000);
sigA_32 = softfloat_shiftRightJam32(sigA_32, (32'h0 - expDiff));
} else {
    if (expA == 8'hFF) {
        if (sigA != 0) {
            return softfloat_propagateNaNF32UI(a, b);
        }
        return a;
    }
    expZ = expA;
    sigB_32 = (expB == 0) ? 2 * sigB_32 : (sigB_32 + 0x20000000);
    sigB_32 = softfloat_shiftRightJam32(sigB_32, (32'h0 + expDiff));
}
U32 sigZ = 0x20000000 + sigA + sigB;
if (sigZ < 0x40000000) {
    expZ = expZ - 1;
    sigZ = sigZ << 1;
}
}
return softfloat_roundPackToF32(signZ, expZ, sigZ[22:0], mode);

```

D.115. softfloat_subMagsF32

Returns difference of the magnitudes of 2 floating point numbers

Return Type	U32
Arguments	U32 a, U32 b, RoundingMode mode

```

Bits<8> expA = expF32UI(a);
Bits<23> sigA = fracF32UI(a);
Bits<8> expB = expF32UI(b);
Bits<23> sigB = fracF32UI(b);
U32 sigZ;
U32 z;
Bits<1> signZ;
Bits<8> expZ;
U32 sigDiff;
U32 sigX;
U32 sigY;
U32 sigA_32;
U32 sigB_32;
Bits<8> shiftDist;
Bits<8> expDiff = expA - expB;
if (expDiff == 8'd0) {
    if (expA == 8'hFF) {
        if ((sigA != 8'd0) || (sigB != 8'd0)) {
            return softfloat_propagateNaNF32UI(a, b);
        }
        return a;
    }
    sigDiff = sigA - sigB;
    if (sigDiff == 0) {
        return packToF32UI(((mode == RoundingMode::RDN) ? 1 : 0), 0, 0);
    }
    if (expA != 0) {
        expA = expA - 1;
    }
    signZ = signF32UI(a);
    if (sigDiff < 0) {
        signZ = ~signZ;
        sigDiff = -32'sh1 * sigDiff;
    }
    shiftDist = count_leading_zeros<32>(sigDiff) - 8;
    expZ = expA - shiftDist;

```

```

    if (expZ < 0) {
        shiftDist = expA;
        expZ = 0;
    }
    return packToF32UI(signZ, expZ, sigDiff << shiftDist);
} else {
    signZ = signF32UI(a);
    sigA_32 = 32'h0 + (sigA << 7);
    sigB_32 = 32'h0 + (sigB << 7);
    if (expDiff < 0) {
        signZ = ~signZ;
        if (expB == 0xFF) {
            if (sigB_32 != 0) {
                return softfloat_propagateNaNF32UI(a, b);
            }
            return packToF32UI(signZ, expB, 0);
        }
        expZ = expB - 1;
        sigX = sigB_32 | 0x40000000;
        sigY = sigA_32 + ((expA != 0) ? 0x40000000 : sigA_32);
        expDiff = -expDiff;
    } else {
        if (expA == 0xFF) {
            if (sigA_32 != 0) {
                return softfloat_propagateNaNF32UI(a, b);
            }
            return a;
        }
        expZ = expA - 1;
        sigX = sigA_32 | 0x40000000;
        sigY = sigB_32 + ((expB != 0) ? 0x40000000 : sigB_32);
    }
    return softfloat_normRoundPackToF32(signZ, expZ, sigX - softfloat_shiftRightJam32(sigY, expDiff), mode);
}

```

D.116. f32_add

Returns sum of 2 floating point numbers

Return Type	U32
Arguments	U32 a, U32 b, RoundingMode mode

```

U32 a_xor_b = a ^ b;
if (signF32UI(a_xor_b) == 1) {
    return softfloat_subMagsF32(a, b, mode);
} else {
    return softfloat_addMagsF32(a, b, mode);
}

```

D.117. f32_sub

Returns difference of 2 floating point numbers

Return Type	U32
Arguments	U32 a, U32 b, RoundingMode mode

```

U32 a_xor_b = a ^ b;
if (signF32UI(a_xor_b) == 1) {
    return softfloat_addMagsF32(a, b, mode);
} else {
    return softfloat_subMagsF32(a, b, mode);
}

```


D.118. i32_to_f32

Converts 32-bit signed integer to 32-bit floating point number

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
Bits<1> sign = a[31];
if ((a & 0x7FFFFFFF) == 0) {
    return (sign == 1) ? packToF32UI(1, 0x9E, 0) : packToF32UI(0, 0, 0);
}
U32 magnitude_of_A = returnMag(a);
return softfloat_normRoundPackToF32(sign, 0x9C, magnitude_of_A, mode);
```

D.119. ui32_to_f32

Converts 32-bit unsigned integer to 32-bit floating point number

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
if (a == 0) {
    return a;
}
if (a[31] == 1) {
    return softfloat_roundPackToF32(0, 0x9D, a >> 1 | (a & 1), mode);
} else {
    return softfloat_normRoundPackToF32(0, 0x9C, a, mode);
}
```

D.120. f32_to_i32

Converts 32-bit floating point number to a signed 32-bit integer

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
Bits<1> sign = signF32UI(a);
Bits<8> exp = expF32UI(a);
Bits<23> sig = fracF32UI(a);
Bits<8> shiftDist;
U64 sig64;
if ((exp == 8'hFF) && (sig != 0)) {
    sign = 0;
    set_fp_flag(FpFlag::NV);
    return I32_NAN;
}
if (exp != 0) {
    sig = sig | 32'h00800000;
}
sig64 = sig << 32;
shiftDist = 8'hAA - exp;
if (shiftDist > 0) {
    sig64 = softfloat_shiftRightJam64(sig64, shiftDist);
}
return softfloat_roundToI32(sign, sig64, mode);
```

D.121. f32_to_ui32

Converts 32-bit floating point number to an unsigned 32-bit integer

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
Bits<1> sign = signF32UI(a);
Bits<8> exp = expF32UI(a);
Bits<23> sig = fracF32UI(a);
Bits<8> shiftDist;
U64 sig64;
if ((exp == 8'hFF) && (sig != 0)) {
    sign = 0;
    set_fp_flag(FpFlag::NV);
    return UI32_NAN;
}
if (exp != 0) {
    sig = sig | 32'h00800000;
}
sig64 = sig `<< 32;
shiftDist = 8'hAA - exp;
if (shiftDist > 0) {
    sig64 = softfloat_shiftRightJam64(sig64, shiftDist);
}
return softfloat_roundToUI32(sign, sig64, mode);
```

D.122. softfloat_roundPackToF32_no_flag

Round FP value according to mmode and then pack it in IEEE format. No flags to be set

Return Type	Bits
Arguments	Bits<1> sign, Bits<8> exp, Bits<23> sig, RoundingMode mode

```
Bits<8> roundIncrement = 0x40;
if ((mode != RoundingMode::RNE) && (mode != RoundingMode::RMM)) {
    roundIncrement = (mode == sign != 0) ? RoundingMode::RDN : RoundingMode::RUP ? 0x7F : 0;
}
Bits<8> roundBits = sig & 0x7f;
if (0xFD <= exp) {
    if ($signed(exp) < 's0) {
        Boolean isTiny = ($signed(exp) < -8's1) || (sig + roundIncrement < 0x80000000);
        sig = softfloat_shiftRightJam32(sig, -exp);
        exp = 0;
        roundBits = sig & 0x7F;
    } else if ('shFD < $signed(exp) || (0x80000000 <= sig + roundIncrement)) {
        return packToF32UI(sign, 0xFF, 0) - roundIncrement == 0) ? 1 : 0);    } } sig = (sig + roundIncrement);
if (sig == 0) {
    exp = 0;
}
return packToF32UI(sign, exp, sig);
```

D.123. softfloat_normRoundPackToF32_no_flag

Normalize, round, and pack into a 32-bit floating point value No flags to be set

Return Type	Bits
Arguments	Bits<1> sign, Bits<8> exp, Bits<23> sig, RoundingMode mode

```
Bits<8> shiftDist = count_leading_zeros<32>(sig) - 1;
exp = exp - shiftDist;
if ((7 <= shiftDist) && (exp < 0xFD)) {
    return packToF32UI(sign, (sig != 0) ? exp : 0, sig << (shiftDist - 7));
} else {
    return softfloat_roundPackToF32_no_flag(sign, exp, sig << shiftDist, mode);
}
```

D.124. i32_to_f32_no_flag

Converts 32-bit signed integer to 32-bit floating point number No flags to be set

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
Bits<1> sign = a[31];
if ((a & 0x7FFFFFFF) == 0) {
    return (sign == 1) ? packToF32UI(1, 0x9E, 0) : packToF32UI(0, 0, 0);
}
U32 magnitude_of_A = returnMag(a);
return softfloat_normRoundPackToF32_no_flag(sign, 0x9C, magnitude_of_A, mode);
```

D.125. softfloat_roundToI32_no_flag

Round to signed 32-bit integer, using rounding_mode No flag to be set

Return Type	Bits
Arguments	Bits<1> sign, Bits<64> sig, RoundingMode roundingMode

```
Bits<16> roundIncrement = 0x800;
if ((roundingMode != RoundingMode::RMM) && (roundingMode != RoundingMode::RNE)) {
    roundIncrement = 0;
    if (sign == 1 ? (roundingMode == RoundingMode::RDN) : (roundingMode == RoundingMode::RUP)) {
        roundIncrement = 0xFFF;
    }
}
Bits<16> roundBits = sig & 0xFFF;
sig = sig + roundIncrement;
if ((sig & 0xFFFFF00000000000) != 0) {
    return sign == 1 ? WORD_NEG_OVERFLOW : WORD_POS_OVERFLOW;
}
Bits<32> sig32 = sig >> 12;
if ((roundBits == 0x800 && (roundingMode == RoundingMode::RNE))) {
    sig32 = sig32 & ~32'b1;
}
Bits<32> z = (sign == 1) ? -sig32 : sig32;
if ((z != 0) && $signed(z) < 's0) != (sign == 1) {
    return sign == 1 ? WORD_NEG_OVERFLOW : WORD_POS_OVERFLOW;
}
return z;
```

D.126. f32_to_i32_no_flag

Converts 32-bit floating point number to a signed 32-bit integer No flags to be set

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
Bits<1> sign = signF32UI(a);
Bits<8> exp = expF32UI(a);
Bits<23> sig = fracF32UI(a);
Bits<8> shiftDist;
U64 sig64;
if ((exp == 8'hFF) && (sig != 0)) {
    sign = 0;
    return I32_NAN;
}
if (exp != 0) {
    sig = sig | 32'h00800000;
}
sig64 = sig `<< 32;
shiftDist = 8'hAA - exp;
if (shiftDist > 0) {
    sig64 = softfloat_shiftRightJam64(sig64, shiftDist);
}
return softfloat_roundToI32_no_flag(sign, sig64, mode);
```

D.127. round_f32_to_integral

Rounds 32-bit floating point number to a signed 32-bit integer. This 32-bit integer is represented as a floating point number and returned.

Return Type	U32
Arguments	U32 a, RoundingMode mode

```
if ((is_sp_neg_inf?(a)) || (is_sp_pos_inf?(a)) || (is_sp_pos_zero?(a)) || (is_sp_neg_zero?(a))) {
    return a;
} else if (is_sp_signaling_nan?(a)) {
    set_fp_flag(FpFlag::NV);
    return a;
}
U32 intermediate;
intermediate = f32_to_i32_no_flag(a, mode);
return i32_to_f32_no_flag(intermediate, mode);
```

D.128. vector_state

Get the current vector state from CSRs

Return Type	VectorState
Arguments	None

```
VectorState state;
state.log2_sew = 3 + CSR[vtype].VSEW;
state.sew = 7'b1 << state.log2_sew;
Bits<3> vlmul = CSR[vtype].VLMUL;
state.lmul_type = CSR[vtype].VLMUL[2] == 1'b1 ? VectorLmulType::Divide : VectorLmulType::Multiply;
state.log2_lmul = CSR[vtype].VLMUL[1:0];
if (vlmul == 3'b101) {
    state.log2_lmul = 3;
} else if (vlmul == 3'b110) {
    state.log2_lmul = 2;
} else if (vlmul == 3'b111) {
    state.log2_lmul = 1;
} else if (vlmul == 3'b100) {
    unpredictable("VLMUL value 0b100 is reserved");
}
return state;
```

D.129. mode

Returns the current active privilege mode.

Return Type	PrivilegeMode
Arguments	None

```
if ((!implemented?(ExtensionName::S)) && (!implemented?(ExtensionName::U)) && (!implemented?(ExtensionName::H))) {
  return PrivilegeMode::M;
} else {
  return current_mode;
}
```

D.130. set_mode_no_refresh

Set the current privilege mode to `new_mode`, but don't refresh interrupts

Return Type	void
Arguments	PrivilegeMode new_mode

```
if (new_mode != current_mode) {
  notify_mode_change(new_mode, current_mode);
  current_mode = new_mode;
}
```

D.131. set_mode

Set the current privilege mode to `new_mode`

Return Type	void
Arguments	PrivilegeMode new_mode

```
if (new_mode != current_mode) {
  notify_mode_change(new_mode, current_mode);
  current_mode = new_mode;
  refresh_pending_interrupts();
}
```

D.132. compatible_mode?

Returns true if target_mode is more privileged than actual_mode.

Return Type	Boolean
Arguments	PrivilegeMode target_mode, PrivilegeMode actual_mode

```
if (target_mode == PrivilegeMode::M) {
  return actual_mode == PrivilegeMode::M;
} else if (target_mode == PrivilegeMode::S) {
  return (actual_mode == PrivilegeMode::M) || (actual_mode == PrivilegeMode::S);
} else if (target_mode == PrivilegeMode::U) {
  return (actual_mode == PrivilegeMode::M) || (actual_mode == PrivilegeMode::S) || (actual_mode == PrivilegeMode::U);
} else if (target_mode == PrivilegeMode::VS) {
  return (actual_mode == PrivilegeMode::M) || (actual_mode == PrivilegeMode::S) || (actual_mode == PrivilegeMode::VS);
} else if (target_mode == PrivilegeMode::VU) {
  return (actual_mode == PrivilegeMode::M) || (actual_mode == PrivilegeMode::S) || (actual_mode == PrivilegeMode::VS) ||
(actual_mode == PrivilegeMode::VU);
}
```

D.133. exception_handling_mode

Returns the target privilege mode that will handle synchronous exception `exception_code`

Return Type	PrivilegeMode
Arguments	ExceptionCode exception_code

```
if (mode() == PrivilegeMode::M) {
    return PrivilegeMode::M;
} else if (implemented?(ExtensionName::S) && mode() == PrivilegeMode::HS) || (mode() == PrivilegeMode::U) {
    if (($bits(CSR[CSR[medeleg]]) & (MXLEN'1 << $bits(exception_code))) != 0) {
        return PrivilegeMode::HS;
    } else {
        return PrivilegeMode::M;
    }
} else {
    assert(implemented?(ExtensionName::H) && mode() == PrivilegeMode::VS) || (mode() == PrivilegeMode::VU, "Unexpected mode");
    if (($bits(CSR[CSR[medeleg]]) & (MXLEN'1 << $bits(exception_code))) != 0) {
        if (($bits(CSR[CSR[hedeleg]]) & (MXLEN'1 << $bits(exception_code))) != 0) {
            return PrivilegeMode::VS;
        } else {
            return PrivilegeMode::HS;
        }
    } else {
        return PrivilegeMode::M;
    }
}
```

D.134. creg2reg

Maps a C register index (e.g., `rs1'` in the specification) to an X register index. From the specification:

Table 22. Registers specified by the three-bit `rs1'`, `rs2'`, and `rd'` fields of the CIW, CL, CS, CA, and CB formats.

RVC Register Number	000	001	010	011	100	101	110	111
Integer Register Number	x8	x9	x10	x11	x12	x13	x14	x15
Integer Register ABI Name	s0	s1	a0	a1	a2	a3	a4	a5
Floating-Point Register Number	f8	f9	f10	f11	f12	f13	f14	f15
Floating-Point Register ABI Name	fs0	fs1	fa0	fa1	fa2	fa3	fa4	fa5

Return Type	Bits5
Arguments	Bits<3> creg_idx

```
return {2'b01, creg_idx};
```

D.135. unimplemented_csr

Either raises an IllegalInstruction exception or enters unpredictable state, depending on the setting of the TRAP_ON_UNIMPLEMENTED_CSR parameter.

Return Type	void
Arguments	Bits<INSTR_ENC_SIZE> encoding

```
if (TRAP_ON_UNIMPLEMENTED_CSR) {
    raise(ExceptionCode::IllegalInstruction, mode(), encoding);
} else {
    unpredictable("Accessing an unimplmented CSR");
}
```


}

D.136. mtval_readonly?

Returns whether or not CSR[mtval] is read-only based on implementation options

Return Type	Boolean
Arguments	None

```
return !(REPORT_VA_IN_MTVAL_ON_BREAKPOINT || REPORT_VA_IN_MTVAL_ON_LOAD_MISALIGNED || REPORT_VA_IN_MTVAL_ON_STORE_AMO_MISALIGNED ||
REPORT_VA_IN_MTVAL_ON_INSTRUCTION_MISALIGNED || REPORT_VA_IN_MTVAL_ON_LOAD_ACCESS_FAULT ||
REPORT_VA_IN_MTVAL_ON_STORE_AMO_ACCESS_FAULT || REPORT_VA_IN_MTVAL_ON_INSTRUCTION_ACCESS_FAULT ||
REPORT_VA_IN_MTVAL_ON_LOAD_PAGE_FAULT || REPORT_VA_IN_MTVAL_ON_STORE_AMO_PAGE_FAULT || REPORT_VA_IN_MTVAL_ON_INSTRUCTION_PAGE_FAULT
|| REPORT_ENCODING_IN_MTVAL_ON_ILLEGAL_INSTRUCTION || REPORT_CAUSE_IN_MTVAL_ON_SHADOW_STACK_SOFTWARE_CHECK ||
REPORT_CAUSE_IN_MTVAL_ON_LANDING_PAD_SOFTWARE_CHECK);
```

D.137. stval_readonly?

Returns whether or not CSR[stval] is read-only based on implementation options

Return Type	Boolean
Arguments	None

```
if (implemented?(ExtensionName::S)) {
    return !(REPORT_VA_IN_STVAL_ON_BREAKPOINT || REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED || REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED
|| REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED || REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT ||
REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT || REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT ||
REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT || REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT || REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT
|| REPORT_ENCODING_IN_STVAL_ON_ILLEGAL_INSTRUCTION || REPORT_CAUSE_IN_STVAL_ON_SHADOW_STACK_SOFTWARE_CHECK ||
REPORT_CAUSE_IN_STVAL_ON_LANDING_PAD_SOFTWARE_CHECK);
} else {
    return true;
}
```

D.138. vstval_readonly?

Returns whether or not CSR[vstval] is read-only based on implementation options

Return Type	Boolean
Arguments	None

```
if (implemented?(ExtensionName::H)) {
    return !(REPORT_VA_IN_VSTVAL_ON_BREAKPOINT || REPORT_VA_IN_VSTVAL_ON_LOAD_MISALIGNED ||
REPORT_VA_IN_VSTVAL_ON_STORE_AMO_MISALIGNED || REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_MISALIGNED ||
REPORT_VA_IN_VSTVAL_ON_LOAD_ACCESS_FAULT || REPORT_VA_IN_VSTVAL_ON_STORE_AMO_ACCESS_FAULT ||
REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_ACCESS_FAULT || REPORT_VA_IN_VSTVAL_ON_LOAD_PAGE_FAULT ||
REPORT_VA_IN_VSTVAL_ON_STORE_AMO_PAGE_FAULT || REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_PAGE_FAULT ||
REPORT_ENCODING_IN_VSTVAL_ON_ILLEGAL_INSTRUCTION || REPORT_CAUSE_IN_VSTVAL_ON_SHADOW_STACK_SOFTWARE_CHECK ||
REPORT_CAUSE_IN_VSTVAL_ON_LANDING_PAD_SOFTWARE_CHECK);
} else {
    return true;
}
```

D.139. mtval_for

Given an exception code and a **legal** non-zero value for mtval, returns the value to be written in mtval considering implementation options

Return Type	XReg

Arguments	ExceptionCode exception_code, XReg tval

```

if (exception_code == ExceptionCode::Breakpoint) {
    return REPORT_VA_IN_MTVAL_ON_BREAKPOINT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAddressMisaligned) {
    return REPORT_VA_IN_MTVAL_ON_LOAD_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAddressMisaligned) {
    return REPORT_VA_IN_MTVAL_ON_STORE_AMO_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAddressMisaligned) {
    return REPORT_VA_IN_MTVAL_ON_INSTRUCTION_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAccessFault) {
    return REPORT_VA_IN_MTVAL_ON_LOAD_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAccessFault) {
    return REPORT_VA_IN_MTVAL_ON_STORE_AMO_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAccessFault) {
    return REPORT_VA_IN_MTVAL_ON_INSTRUCTION_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadPageFault) {
    return REPORT_VA_IN_MTVAL_ON_LOAD_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoPageFault) {
    return REPORT_VA_IN_MTVAL_ON_STORE_AMO_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionPageFault) {
    return REPORT_VA_IN_MTVAL_ON_INSTRUCTION_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::IllegalInstruction) {
    return REPORT_ENCODING_IN_MTVAL_ON_ILLEGAL_INSTRUCTION ? tval : 0;
} else if (exception_code == ExceptionCode::SoftwareCheck) {
    return tval;
} else {
    return 0;
}

```

D.140. stval_for

Given an exception code and a **legal** non-zero value for stval, returns the value to be written in stval considering implementation options

Return Type	XReg
Arguments	ExceptionCode exception_code, XReg tval

```

if (exception_code == ExceptionCode::Breakpoint) {
    return REPORT_VA_IN_STVAL_ON_BREAKPOINT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAddressMisaligned) {
    return REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAddressMisaligned) {
    return REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAddressMisaligned) {
    return REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAccessFault) {
    return REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAccessFault) {
    return REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAccessFault) {
    return REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadPageFault) {
    return REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoPageFault) {
    return REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionPageFault) {
    return REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::IllegalInstruction) {
    return REPORT_ENCODING_IN_STVAL_ON_ILLEGAL_INSTRUCTION ? tval : 0;
} else if (exception_code == ExceptionCode::SoftwareCheck) {
    return tval;
} else {
    return 0;
}

```


D.141. vstval_for

Given an exception code and a **legal** non-zero value for vstval, returns the value to be written in vstval considering implementation options

Return Type	XReg
Arguments	ExceptionCode exception_code, XReg tval

```
if (exception_code == ExceptionCode::Breakpoint) {
    return REPORT_VA_IN_VSTVAL_ON_BREAKPOINT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAddressMisaligned) {
    return REPORT_VA_IN_VSTVAL_ON_LOAD_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAddressMisaligned) {
    return REPORT_VA_IN_VSTVAL_ON_STORE_AMO_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAddressMisaligned) {
    return REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_MISALIGNED ? tval : 0;
} else if (exception_code == ExceptionCode::LoadAccessFault) {
    return REPORT_VA_IN_VSTVAL_ON_LOAD_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoAccessFault) {
    return REPORT_VA_IN_VSTVAL_ON_STORE_AMO_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionAccessFault) {
    return REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_ACCESS_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::LoadPageFault) {
    return REPORT_VA_IN_VSTVAL_ON_LOAD_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::StoreAmoPageFault) {
    return REPORT_VA_IN_VSTVAL_ON_STORE_AMO_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::InstructionPageFault) {
    return REPORT_VA_IN_VSTVAL_ON_INSTRUCTION_PAGE_FAULT ? tval : 0;
} else if (exception_code == ExceptionCode::IllegalInstruction) {
    return REPORT_ENCODING_IN_VSTVAL_ON_ILLEGAL_INSTRUCTION ? tval : 0;
} else if (exception_code == ExceptionCode::SoftwareCheck) {
    return tval;
} else {
    return 0;
}
```

D.142. raise_guest_page_fault

Raise a guest page fault exception.

Return Type	void
Arguments	MemoryOperation op, XReg gpa, XReg gva, XReg tinst_value, PrivilegeMode from_mode

```
ExceptionCode code;
Boolean write_gpa_in_tval;
if (op == MemoryOperation::Read) {
    code = ExceptionCode::LoadGuestPageFault;
    write_gpa_in_tval = REPORT_GPA_IN_TVAL_ON_LOAD_GUEST_PAGE_FAULT;
} else if (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite) {
    code = ExceptionCode::StoreAmoGuestPageFault;
    write_gpa_in_tval = REPORT_GPA_IN_TVAL_ON_STORE_AMO_GUEST_PAGE_FAULT;
} else {
    assert(op == MemoryOperation::Fetch, "unexpected memory operation");
    code = ExceptionCode::InstructionGuestPageFault;
    write_gpa_in_tval = REPORT_GPA_IN_TVAL_ON_INSTRUCTION_GUEST_PAGE_FAULT;
}
PrivilegeMode handling_mode = exception_handling_mode(code);
if (handling_mode == PrivilegeMode::S) {
    CSR[htval].VALUE = write_gpa_in_tval ? (gpa >> 2) : 0;
    CSR[htinst].VALUE = tinst_value;
    CSR[sepc].PC = $pc;
    if (!stval_readonly?()) {
        CSR[stval].VALUE = stval_for(code, gva);
    }
    $pc = {CSR[stvec].BASE, 2'b00};
}
```

```
CSR[scause].INT = 1'b0;
CSR[scause].CODE = $bits(code);
CSR[hstatus].GVA = 1;
CSR[hstatus].SPV = 1;
CSR[hstatus].SPVP = $bits(from_mode)[0];
CSR[mstatus].SPP = $bits(from_mode)[0];
} else {
  assert(handling_mode == PrivilegeMode::M, "unexpected privilege mode");
  CSR[mtval2].VALUE = write_gpa_in_tval ? (gpa >> 2) : 0;
  CSR[mtinst].VALUE = tinst_value;
  CSR[mstatus].MPP = $bits(from_mode)[1:0];
  if (MXLEN == 64) {
    CSR[mstatus].MPV = 1;
  } else {
    CSR[mstatush].MPV = 1;
  }
}
set_mode(handling_mode);
abort_current_instruction();
```

D.143. raise

Raise synchronous exception number `exception_code`.

The exception may be imprecise, and will cause execution to enter an unpredictable state, if `PRECISE_SYNCHRONOUS_EXCEPTIONS` is false.

Otherwise, the exception will be precise.

Return Type	void
Arguments	ExceptionCode exception_code, PrivilegeMode from_mode, XReg tval

```
if (!PRECISE_SYNCHRONOUS_EXCEPTIONS) {
  unpredictable("Imprecise synchronous exception");
} else {
  raise_precise(exception_code, from_mode, tval);
}
```

D.144. raise_precise

Raise synchronous exception number `exception_code`.

Return Type	void
Arguments	ExceptionCode exception_code, PrivilegeMode from_mode, XReg tval

```
PrivilegeMode handling_mode = exception_handling_mode(exception_code);
if (handling_mode == PrivilegeMode::M) {
  CSR[mepc].PC = $pc;
  if (!mtval_readonly?()) {
    CSR[mtval].VALUE = mtval_for(exception_code, tval);
  }
  $pc = {CSR[mtvec].BASE, 2'b00};
  CSR[mcause].INT = 1'b0;
  CSR[mcause].CODE = $bits(exception_code);
  if (CSR[misa].H == 1) {
    CSR[mtval2].VALUE = 0;
    CSR[mtinst].VALUE = 0;
    if (from_mode == PrivilegeMode::VU || from_mode == PrivilegeMode::VS) {
      if (MXLEN == 32) {
        CSR[mstatush].MPV = 1;
      } else {
        CSR[mstatus].MPV = 1;
      }
    }
  } else {
    if (MXLEN == 32) {
```

```
        CSR[mstatush].MPV = 0;
    } else {
        CSR[mstatus].MPV = 0;
    }
}
}
CSR[mstatus].MPP = $bits(from_mode);
} else if (CSR[misa].S == 1 && (handling_mode == PrivilegeMode::S)) {
    CSR[sepc].PC = $pc;
    if (!stval_readonly?()) {
        CSR[stval].VALUE = stval_for(exception_code, tval);
    }
    $pc = {CSR[stvec].BASE, 2'b00};
    CSR[scause].INT = 1'b0;
    CSR[scause].CODE = $bits(exception_code);
    CSR[mstatus].SPP = $bits(from_mode)[0];
    if (CSR[misa].H == 1) {
        CSR[htval].VALUE = 0;
        CSR[htinst].VALUE = 0;
        CSR[hstatus].SPV = $bits(from_mode)[2];
        if (from_mode == PrivilegeMode::VU || from_mode == PrivilegeMode::VS) {
            CSR[hstatus].SPV = 1;
            if (exception_code == ExceptionCode::Breakpoint) && (REPORT_VA_IN_STVAL_ON_BREAKPOINT || exception_code ==
ExceptionCode::LoadAddressMisaligned) && (REPORT_VA_IN_STVAL_ON_LOAD_MISALIGNED || exception_code ==
ExceptionCode::StoreAmoAddressMisaligned) && (REPORT_VA_IN_STVAL_ON_STORE_AMO_MISALIGNED || exception_code ==
ExceptionCode::InstructionAddressMisaligned) && (REPORT_VA_IN_STVAL_ON_INSTRUCTION_MISALIGNED || exception_code ==
ExceptionCode::LoadAccessFault) && (REPORT_VA_IN_STVAL_ON_LOAD_ACCESS_FAULT || exception_code ==
ExceptionCode::StoreAmoAccessFault) && (REPORT_VA_IN_STVAL_ON_STORE_AMO_ACCESS_FAULT || exception_code ==
ExceptionCode::InstructionAccessFault) && (REPORT_VA_IN_STVAL_ON_INSTRUCTION_ACCESS_FAULT || exception_code ==
ExceptionCode::LoadPageFault) && (REPORT_VA_IN_STVAL_ON_LOAD_PAGE_FAULT || exception_code == ExceptionCode::StoreAmoPageFault) &&
(REPORT_VA_IN_STVAL_ON_STORE_AMO_PAGE_FAULT || exception_code == ExceptionCode::InstructionPageFault) &&
(REPORT_VA_IN_STVAL_ON_INSTRUCTION_PAGE_FAULT) {
                CSR[hstatus].GVA = 1;
            } else {
                CSR[hstatus].GVA = 0;
            }
            CSR[hstatus].SPVP = $bits(from_mode)[0];
        } else {
            CSR[hstatus].SPV = 0;
            CSR[hstatus].GVA = 0;
        }
    }
}
} else if (CSR[misa].H == 1 && (handling_mode == PrivilegeMode::VS)) {
    CSR[vsepc].PC = $pc;
    if (!vstval_readonly?()) {
        CSR[vstval].VALUE = vstval_for(exception_code, tval);
    }
    $pc = {CSR[vstvec].BASE, 2'b00};
    CSR[vscause].INT = 1'b0;
    CSR[vscause].CODE = $bits(exception_code);
    CSR[vsstatus].SPP = $bits(from_mode)[0];
}
set_mode(handling_mode);
abort_current_instruction();
```

D.145. ialign

Returns IALIGN, the smallest instruction encoding size, in bits.

Return Type	Bits⑥
Arguments	None

```
if (implemented?(ExtensionName::C) && (CSR[misa].C == 0x1)) {
    return 16;
} else {
    return 32;
}
```

D.146. jump

Jump to virtual address `target_addr`.

If target address is misaligned, raise a `MisalignedAddress` exception.

Return Type	void
Arguments	XReg target_addr

```
if ((ialign() == 16) && target_addr & 0x1) != 0 {
    raise(ExceptionCode::InstructionAddressMisaligned, mode(), target_addr);
} else if ((ialign() == 32) && (target_addr & 0x3) != 0) {
    raise(ExceptionCode::InstructionAddressMisaligned, mode(), target_addr);
}
$pc = target_addr;
```

D.147. jump_halfword

Jump to virtual halfword address `target_hw_addr`.

If target address is misaligned, raise a `MisalignedAddress` exception.

Return Type	void
Arguments	XReg target_hw_addr

```
assert((target_hw_addr & 0x1) == 0x0, "Expected halfword-aligned address in jump_halfword");
if (ialign() != 16) {
    if ((target_hw_addr & 0x3) != 0) {
        raise(ExceptionCode::InstructionAddressMisaligned, mode(), target_hw_addr);
    }
}
$pc = target_hw_addr;
```

D.148. valid_interrupt_code?

Returns true if `code` is a legal interrupt number.

Return Type	Boolean
Arguments	XReg code

```
if (code > 1 << $enum_element_size(InterruptCode - 1)) {
    return false;
}
if ($array_includes?($enum_to_a(InterruptCode), code)) {
    return true;
} else {
    return false;
}
```

D.149. valid_exception_code?

Returns true if `code` is a legal exception number.

Return Type	Boolean

Arguments	XReg code

```

if (code > 1 `<< $enum_element_size(ExceptionCode - 1)) {
    return false;
}
if ($array_includes?($enum_to_a(ExceptionCode), code)) {
    return true;
} else {
    return false;
}

```

D.150. xlen

Returns the effective XLEN for the current privilege mode.

Return Type	Bits③
Arguments	None

```

if (MXLEN == 32) {
    return 32;
} else {
    if (mode() == PrivilegeMode::M) {
        if (CSR[misa].MXL == $bits(XRegWidth::XLEN32)) {
            return 32;
        } else if (CSR[misa].MXL == $bits(XRegWidth::XLEN64)) {
            return 64;
        } else {
            unreachable();
        }
    } else if (implemented?(ExtensionName::S) && mode() == PrivilegeMode::S) {
        if (CSR[mstatus].SXL == $bits(XRegWidth::XLEN32)) {
            return 32;
        } else if (CSR[mstatus].SXL == $bits(XRegWidth::XLEN64)) {
            return 64;
        } else {
            unreachable();
        }
    } else if (implemented?(ExtensionName::U) && mode() == PrivilegeMode::U) {
        if (CSR[mstatus].UXL == $bits(XRegWidth::XLEN32)) {
            return 32;
        } else if (CSR[mstatus].UXL == $bits(XRegWidth::XLEN64)) {
            return 64;
        } else {
            unreachable();
        }
    } else if (implemented?(ExtensionName::H) && mode() == PrivilegeMode::VS) {
        if (CSR[hstatus].VSXL == $bits(XRegWidth::XLEN32)) {
            return 32;
        } else if (CSR[hstatus].VSXL == $bits(XRegWidth::XLEN64)) {
            return 64;
        } else {
            unreachable();
        }
    } else if (implemented?(ExtensionName::H) && mode() == PrivilegeMode::VU) {
        if (CSR[vsstatus].UXL == $bits(XRegWidth::XLEN32)) {
            return 32;
        } else if (CSR[vsstatus].UXL == $bits(XRegWidth::XLEN64)) {
            return 64;
        } else {
            unreachable();
        }
    }
}
}

```

D.151. virtual_mode?

Returns True if the current mode is virtual (VS or VU).

Return Type	Boolean
Arguments	None

```
return (mode() == PrivilegeMode::VS) || (mode() == PrivilegeMode::VU);
```

D.152. mask_eaddr

Mask upper N bits of an effective address if pointer masking is enabled

Return Type	XReg
Arguments	XReg eaddr

```
return eaddr;
```

D.153. pmp_match_64

Given a physical address, see if any PMP entry matches.

If there is a complete match, return the PmpCfg that guards the region. If there is no match or a partial match, report that result.

Return Type	PmpMatchResult, PmpCfg
Arguments	Bits<PHYS_ADDR_WIDTH> paddr, U32 access_size

```
Bits<12> pmpcfg0_addr = 0x3a0;
Bits<12> pmpaddr0_addr = 0x3b0;
for (U32 i = 0; i < NUM_PMP_ENTRIES; i++) {
    Bits<12> pmpcfg_idx = pmpcfg0_addr + (i / 8) * 2;
    Bits<6> shamt = (i % 8) * 8;
    Csr pmpcfg_csr = direct_csr_lookup(pmpcfg_idx);
    PmpCfg cfg = (csr_hw_read(pmpcfg_csr) >> shamt)[7:0];
    Bits<12> pmpaddr_idx = pmpaddr0_addr + i;
    Csr pmpaddr_csr = direct_csr_lookup(pmpaddr_idx);
    Bits<64> pmpaddr_csr_value = csr_sw_read(pmpaddr_csr);
    Bits<PHYS_ADDR_WIDTH> range_base = 0;
    Bits<PHYS_ADDR_WIDTH> range_limit = 0;
    if (cfg.A == $bits(PmpCfg_A::TOR)) {
        if (i == 0) {
            range_base = 0;
        } else {
            Csr tor_pmpaddr_csr = direct_csr_lookup(pmpaddr_idx - 1);
            range_base = (csr_sw_read(tor_pmpaddr_csr))[PHYS_ADDR_WIDTH - 1:0];
        }
        range_limit = (pmpaddr_csr_value)[PHYS_ADDR_WIDTH - 1:0] - 1;
    } else if (cfg.A == $bits(PmpCfg_A::NAPOT)) {
        Bits<PHYS_ADDR_WIDTH - 1> pmpaddr_value = pmpaddr_csr_value[PHYS_ADDR_WIDTH - 1:0];
        Bits<PHYS_ADDR_WIDTH - 1> mask = pmpaddr_value ^ (pmpaddr_value + 1);
        range_base = (pmpaddr_value & ~mask);
        range_limit = range_base + mask;
    } else if (cfg.A == $bits(PmpCfg_A::NA4)) {
        range_base = pmpaddr_csr_value[PHYS_ADDR_WIDTH - 1:0];
        range_limit = range_base + 3;
    }
    if (paddr {
        return PmpMatchResult::FullMatch, cfg;
    } else if (! {
        return PmpMatchResult::PartialMatch, -;
    }
}
```



```
}
return PmpMatchResult::NoMatch, -;
```

D.154. pmp_match_32

Given a physical address, see if any PMP entry matches.

If there is a complete match, return the PmpCfg that guards the region. If there is no match or a partial match, report that result.

Return Type	PmpMatchResult, PmpCfg
Arguments	Bits<PHYS_ADDR_WIDTH> paddr, U32 access_size

```
Bits<12> pmpcfg0_addr = 0x3a0;
Bits<12> pmpaddr0_addr = 0x3b0;
for (U32 i = 0; i < NUM_PMP_ENTRIES; i++) {
    Bits<12> pmpcfg_idx = pmpcfg0_addr + (i / 4);
    Bits<6> shamt = (i % 4) * 8;
    Csr pmpcfg_csr = direct_csr_lookup(pmpcfg_idx);
    PmpCfg cfg = (csr_hw_read(pmpcfg_csr) >> shamt)[7:0];
    Bits<12> pmpaddr_idx = pmpaddr0_addr + i;
    Csr pmpaddr_csr = direct_csr_lookup(pmpaddr_idx);
    Bits<32> pmpaddr_csr_value = csr_sw_read(pmpaddr_csr);
    Bits<PHYS_ADDR_WIDTH> range_base = 0;
    Bits<PHYS_ADDR_WIDTH> range_limit = 0;
    if (cfg.A == $bits(PmpCfg_A::TOR)) {
        if (i == 0) {
            range_base = 0;
        } else {
            Csr tor_pmpaddr_csr = direct_csr_lookup(pmpaddr_idx - 1);
            range_base = csr_sw_read(tor_pmpaddr_csr)[PHYS_ADDR_WIDTH - 1:0];
        }
        range_limit = (pmpaddr_csr_value)[PHYS_ADDR_WIDTH - 1:0] - 1;
    } else if (cfg.A == $bits(PmpCfg_A::NAPOT)) {
        Bits<PHYS_ADDR_WIDTH - 1> pmpaddr_value = pmpaddr_csr_value[PHYS_ADDR_WIDTH - 3:0];
        Bits<PHYS_ADDR_WIDTH - 1> mask = pmpaddr_value ^ (pmpaddr_value + 1);
        range_base = pmpaddr_value & ~mask;
        range_limit = range_base + mask;
    } else if (cfg.A == $bits(PmpCfg_A::NA4)) {
        range_base = pmpaddr_csr_value[PHYS_ADDR_WIDTH - 1:0];
        range_limit = range_base + 3;
    }
    if (paddr {
        return PmpMatchResult::FullMatch, cfg;
    } else if (! {
        return PmpMatchResult::PartialMatch, -;
    }
}
return PmpMatchResult::NoMatch, -;
```

D.155. pmp_match

Given a physical address, see if any PMP entry matches.

If there is a complete match, return the PmpCfg that guards the region. If there is no match or a partial match, report that result.

Return Type	PmpMatchResult, PmpCfg
Arguments	Bits<PHYS_ADDR_WIDTH> paddr, U32 access_size

```
if (MXLEN == 64) {
    return pmp_match_64(paddr, access_size);
} else {
    return pmp_match_32(paddr, access_size);
}
```

D.156. mpv

Returns the current value of CSR[mstatus].MPV (when MXLEN == 64) of CSR[mstatush].MPV (when MXLEN == 32)

Return Type	Bits①
Arguments	None

```
if (implemented?(ExtensionName::H)) {
    return (MXLEN == 32) ? CSR[mstatush].MPV : CSR[mstatus].MPV;
} else {
    assert(false, "TODO");
}
```

D.157. effective_ldst_mode

Returns the effective privilege mode for normal explicit loads and stores, taking into account the current actual privilege mode and modifications from mstatus.MPRV.

Return Type	PrivilegeMode
Arguments	None

```
if (mode() == PrivilegeMode::M) {
    if (CSR[misa].U == 1 && CSR[mstatus].MPRV == 1) {
        if (CSR[mstatus].MPP == 0b00) {
            if (CSR[misa].H == 1 && mpv() == 0b1) {
                return PrivilegeMode::VU;
            } else {
                return PrivilegeMode::U;
            }
        } else if (CSR[misa].S == 1 && CSR[mstatus].MPP == 0b01) {
            if (CSR[misa].H == 1 && mpv() == 0b1) {
                return PrivilegeMode::VS;
            } else {
                return PrivilegeMode::S;
            }
        }
    }
}
return mode();
```

D.158. pmp_check

Given a physical address and operation type, return whether or not the access is allowed by PMP.

Return Type	Boolean
Arguments	Bits<PHYS_ADDR_WIDTH> paddr, U32 access_size, MemoryOperation type

```
PrivilegeMode mode = effective_ldst_mode();
PmpMatchResult match_result;
PmpCfg cfg;
(match_result, cfg = pmp_match(paddr, access_size));
if (match_result == PmpMatchResult::FullMatch) {
    if (mode == PrivilegeMode::M && (cfg.L == 0)) {
        return true;
    }
    if (type == MemoryOperation::Write && (cfg.W == 0)) {
        return false;
    } else if (type == MemoryOperation::Read && (cfg.R == 0)) {
        return false;
    } else if (type == MemoryOperation::Fetch && (cfg.X == 0)) {
        return false;
    }
}
```



```
    } else if (match_result == PmpMatchResult::NoMatch) {
        if (mode == PrivilegeMode::M) {
            return true;
        } else {
            return false;
        }
    } else {
        assert(match_result == PmpMatchResult::PartialMatch, "PMP matching logic error");
        return false;
    }
    return true;
}
```

D.159. access_check

Checks if the physical address paddr is able to access memory, and raises the appropriate exception if not.

Return Type	void
Arguments	Bits<PHYS_ADDR_WIDTH> paddr, U32 access_size, XReg vaddr, MemoryOperation type, ExceptionCode fault_type, PrivilegeMode from_mode

```
if (paddr > 1 << PHYS_ADDR_WIDTH) - access_size {
    raise(fault_type, from_mode, vaddr);
}
if (implemented?(ExtensionName::Smpmp)) {
    if (!pmp_check(paddr[PHYS_ADDR_WIDTH - 1:0], access_size, type)) {
        raise(fault_type, from_mode, vaddr);
    }
}
```

D.160. base32?

return True iff current effective XLEN == 32

Return Type	Boolean
Arguments	None

```
if (MXLEN == 32) {
    return true;
} else {
    XRegWidth xlen32 = XRegWidth::XLEN32;
    if (mode() == PrivilegeMode::M) {
        return CSR[misa].MXL == $bits(xlen32);
    } else if (implemented?(ExtensionName::S) && mode() == PrivilegeMode::S) {
        return CSR[mstatus].SXL == $bits(xlen32);
    } else if (implemented?(ExtensionName::U) && mode() == PrivilegeMode::U) {
        return CSR[mstatus].UXL == $bits(xlen32);
    } else if (implemented?(ExtensionName::H) && mode() == PrivilegeMode::VS) {
        return CSR[hstatus].VSXL == $bits(xlen32);
    } else {
        assert(implemented?(ExtensionName::H) && mode() == PrivilegeMode::VU, "Unexpected mode");
        return CSR[vsstatus].UXL == $bits(xlen32);
    }
}
```

D.161. base64?

return True iff current effective XLEN == 64

Return Type	Boolean
Arguments	None

```
return xlen() == 64;
```

D.162. current_translation_mode

Returns the current first-stage translation mode for an explicit load or store from mode given the machine state (e.g., value of `satp` or `vsatp` csr).

Returns `SatpMode::Reserved` if the setting found in `satp` or `vsatp` is invalid.

Return Type	SatpMode
Arguments	PrivilegeMode mode

```
PrivilegeMode effective_mode = effective_ldst_mode();
if (effective_mode == PrivilegeMode::M) {
    return SatpMode::Bare;
}
if (CSR[misa].H == 1'b1) {
    if (effective_mode == PrivilegeMode::VS || effective_mode == PrivilegeMode::VU) {
        Bits<4> mode_val = CSR[vsatp].MODE;
        if (mode_val == $bits(SatpMode::Bare)) {
            return SatpMode::Bare;
        } else if (mode_val == $bits(SatpMode::Sv32)) {
            if (MXLEN == 64) {
                if ((effective_mode == PrivilegeMode::VS) && (CSR[hstatus].VSXL != $bits(XRegWidth::XLEN32))) {
                    return SatpMode::Reserved;
                }
                if ((effective_mode == PrivilegeMode::VU) && (CSR[vsstatus].UXL != $bits(XRegWidth::XLEN32))) {
                    return SatpMode::Reserved;
                }
            }
            if (!SV32_VSMODE_TRANSLATION) {
                return SatpMode::Reserved;
            }
            return SatpMode::Sv32;
        } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv39))) {
            if (effective_mode == PrivilegeMode::VS && CSR[hstatus].VSXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (effective_mode == PrivilegeMode::VU && CSR[vsstatus].UXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (!SV39_VSMODE_TRANSLATION) {
                return SatpMode::Reserved;
            }
            return SatpMode::Sv39;
        } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv48))) {
            if (effective_mode == PrivilegeMode::VS && CSR[hstatus].VSXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (effective_mode == PrivilegeMode::VU && CSR[vsstatus].UXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (!SV48_VSMODE_TRANSLATION) {
                return SatpMode::Reserved;
            }
            return SatpMode::Sv48;
        } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv57))) {
            if (effective_mode == PrivilegeMode::VS && CSR[hstatus].VSXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (effective_mode == PrivilegeMode::VU && CSR[vsstatus].UXL != $bits(XRegWidth::XLEN64)) {
                return SatpMode::Reserved;
            }
            if (!SV57_VSMODE_TRANSLATION) {
                return SatpMode::Reserved;
            }
            return SatpMode::Sv57;
        } else {
            return SatpMode::Reserved;
        }
    }
}
```

```

    }
} else {
    return SatpMode::Reserved;
}
} else if (CSR[misa].S == 1'b1) {
    assert(effective_mode == PrivilegeMode::S || effective_mode == PrivilegeMode::U, "unexpected priv mode");
    Bits<4> mode_val = CSR[satp].MODE;
    if (mode_val == $bits(SatpMode::Bare)) {
        return SatpMode::Bare;
    } else if (mode_val == $bits(SatpMode::Sv32)) {
        if (MXLEN == 64) {
            if (effective_mode == PrivilegeMode::S && CSR[mstatus].SXL != $bits(XRegWidth::XLEN32)) {
                return SatpMode::Reserved;
            }
            if (effective_mode == PrivilegeMode::U && CSR[sstatus].UXL != $bits(XRegWidth::XLEN32)) {
                return SatpMode::Reserved;
            }
        }
        if (!implemented?(ExtensionName::Sv32)) {
            return SatpMode::Reserved;
        }
        return SatpMode::Sv32;
    } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv39))) {
        if (effective_mode == PrivilegeMode::S && CSR[mstatus].SXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (effective_mode == PrivilegeMode::U && CSR[sstatus].UXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (!implemented?(ExtensionName::Sv39)) {
            return SatpMode::Reserved;
        }
        return SatpMode::Sv39;
    } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv48))) {
        if (effective_mode == PrivilegeMode::S && CSR[mstatus].SXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (effective_mode == PrivilegeMode::U && CSR[sstatus].UXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (!implemented?(ExtensionName::Sv48)) {
            return SatpMode::Reserved;
        }
        return SatpMode::Sv48;
    } else if ((MXLEN == 64) && (mode_val == $bits(SatpMode::Sv57))) {
        if (effective_mode == PrivilegeMode::S && CSR[mstatus].SXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (effective_mode == PrivilegeMode::U && CSR[sstatus].UXL != $bits(XRegWidth::XLEN64)) {
            return SatpMode::Reserved;
        }
        if (!implemented?(ExtensionName::Sv57)) {
            return SatpMode::Reserved;
        }
        return SatpMode::Sv57;
    } else {
        return SatpMode::Reserved;
    }
} else {
    return SatpMode::Reserved;
}
}

```

D.163. current_gstage_translation_mode

Returns the current second-stage translation mode for a load or store from VS-mode or VU-mode.

Return Type	HgatpMode
Arguments	None

```

return $enum(HgatpMode, CSR[hgatp].MODE);

```

D.164. translate_gstage

Translates a guest physical address to a physical address.

Return Type	TranslationResult
Arguments	XReg gpaddr, XReg vaddr, MemoryOperation op, PrivilegeMode effective_mode, Bits<INSTR_ENC_SIZE> encoding

```
TranslationResult result;
if (effective_mode == PrivilegeMode::S || effective_mode == PrivilegeMode::U) {
    result.paddr = gpaddr;
    return result;
}
Boolean mxr = CSR[mstatus].MXR == 1;
if (GSTAGE_MODE_BARE && CSR[hgatp].MODE == $bits(HgatpMode::Bare)) {
    result.paddr = gpaddr;
    return result;
} else if (SV32X4_TRANSLATION && CSR[hgatp].MODE == $bits(HgatpMode::Sv32x4)) {
    return gstage_page_walk<32, 34, 32, 2>(gpaddr, vaddr, op, effective_mode, false, encoding);
} else if (SV39X4_TRANSLATION && CSR[hgatp].MODE == $bits(HgatpMode::Sv39x4)) {
    return gstage_page_walk<39, 56, 64, 3>(gpaddr, vaddr, op, effective_mode, false, encoding);
} else if (SV48X4_TRANSLATION && CSR[hgatp].MODE == $bits(HgatpMode::Sv48x4)) {
    return gstage_page_walk<48, 56, 64, 4>(gpaddr, vaddr, op, effective_mode, false, encoding);
} else if (SV57X4_TRANSLATION && CSR[hgatp].MODE == $bits(HgatpMode::Sv57x4)) {
    return gstage_page_walk<57, 56, 64, 5>(gpaddr, vaddr, op, effective_mode, false, encoding);
} else {
    if (op == MemoryOperation::Read) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst_value_for_guest_page_fault(op, encoding, true), effective_mode);
    } else if (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst_value_for_guest_page_fault(op, encoding, true), effective_mode);
    } else {
        assert(op == MemoryOperation::Fetch, "unexpected memory op");
        raise_guest_page_fault(op, gpaddr, vaddr, tinst_value_for_guest_page_fault(op, encoding, true), effective_mode);
    }
}
```

D.165. tinst_value_for_guest_page_fault

Returns the value of htinst/mtinst for a Guest Page Fault

Return Type	XReg
Arguments	MemoryOperation op, Bits<INSTR_ENC_SIZE> encoding, Boolean for_final_vs_pte

```
if (for_final_vs_pte) {
    if (op == MemoryOperation::Fetch) {
        if (TINST_VALUE_ON_FINAL_INSTRUCTION_GUEST_PAGE_FAULT == "always zero") {
            return 0;
        } else {
            assert(TINST_VALUE_ON_FINAL_INSTRUCTION_GUEST_PAGE_FAULT == "always pseudoinstruction", "Instruction guest page faults can only report zero/pseudo instruction in tval");
            return 0x00002000;
        }
    } else if (op == MemoryOperation::Read) {
        if (TINST_VALUE_ON_FINAL_LOAD_GUEST_PAGE_FAULT == "always zero") {
            return 0;
        } else if (TINST_VALUE_ON_FINAL_LOAD_GUEST_PAGE_FAULT == "always pseudoinstruction") {
            if (($array_size(VSXLEN) == 1 && VSXLEN[0] == 32) || MXLEN == 64) && (CSR[hstatus].VSXL == $bits(XRegWidth::XLLEN32)) {
                return 0x00002000;
            } else {
                return 0x00003000;
            }
        } else if (TINST_VALUE_ON_FINAL_LOAD_GUEST_PAGE_FAULT == "always transformed standard instruction") {
            return tinst_transform(encoding, 0);
        } else {
```

```
        unpredictable("Custom value written into htinst/mtinst");
    }
} else if (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite) {
    if (TINST_VALUE_ON_FINAL_STORE_AMO_GUEST_PAGE_FAULT == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_FINAL_STORE_AMO_GUEST_PAGE_FAULT == "always pseudoinstruction") {
        if (($array_size(VSXLEN) == 1 && VSXLEN[0] == 32) || MXLEN == 64) && (CSR[hstatus].VSXL == $bits(XRegWidth::XLEN32)) {
            return 0x00002020;
        } else {
            return 0x00003020;
        }
    } else if (TINST_VALUE_ON_FINAL_STORE_AMO_GUEST_PAGE_FAULT == "always transformed standard instruction") {
        return tinst_transform(encoding, 0);
    } else {
        unpredictable("Custom value written into htinst/mtinst");
    }
}
} else {
    if (REPORT_GPA_IN_TVAL_ON_INTERMEDIATE_GUEST_PAGE_FAULT) {
        if (($array_size(VSXLEN) == 1 && VSXLEN[0] == 32) || MXLEN == 64) && (CSR[hstatus].VSXL == $bits(XRegWidth::XLEN32)) {
            return 0x00002000;
        } else if (($array_size(VSXLEN) == 1 && VSXLEN[0] == 64) || MXLEN == 64) && (CSR[hstatus].VSXL == $bits(XRegWidth::XLEN64)) {
            return 0x00003000;
        }
    }
}
}
```

D.166. tinst_transform

Returns the standard transformation of an encoding for htinst/mtinst

Return Type	Bits<INSTR_ENC_SIZE>
Arguments	Bits<INSTR_ENC_SIZE> encoding, Bits<5> addr_offset

```
if (encoding[1:0] == 0b11) {
    if (encoding[6:2] == 5'b00001) {
        return {{12{1'b0}}, addr_offset, encoding[14:0]};
    } else if (encoding[6:2] == 5'b01000) {
        return {{7{1'b0}}, encoding[24:20], addr_offset, encoding[14:12], {5{1'b0}}, encoding[6:0]};
    } else if (encoding[6:2] == 5'b01011) {
        return {encoding[31:20], addr_offset, encoding[14:0]};
    } else if (encoding[6:2] == 5'b00011) {
        return {encoding[31:20], addr_offset, encoding[14:0]};
    } else {
        assert(false, "Bad transform");
    }
} else {
    assert(false, "TODO: compressed instruction");
}
```

D.167. transformed_standard_instruction_for_tinst

Transforms an instruction encoding for htinst.

Return Type	Bits<INSTR_ENC_SIZE>
Arguments	Bits<INSTR_ENC_SIZE> original

```
assert(false, "TODO");
return 0;
```

D.168. tinst_value

Returns the value of htinst/mtinst for the given exception code.

Return Type	XReg
Arguments	ExceptionCode code, Bits<INSTR_ENC_SIZE> encoding

```
if (code == ExceptionCode::InstructionAddressMisaligned) {
    if (TINST_VALUE_ON_INSTRUCTION_ADDRESS_MISALIGNED == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to an InstructionAddressMisaligned exception");
    }
} else if (code == ExceptionCode::InstructionAccessFault) {
    return 0;
} else if (code == ExceptionCode::IllegalInstruction) {
    return 0;
} else if (code == ExceptionCode::Breakpoint) {
    if (TINST_VALUE_ON_BREAKPOINT == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a Breakpoint exception");
    }
} else if (code == ExceptionCode::VirtualInstruction) {
    if (TINST_VALUE_ON_VIRTUAL_INSTRUCTION == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a VirtualInstruction exception");
    }
} else if (code == ExceptionCode::LoadAddressMisaligned) {
    if (TINST_VALUE_ON_LOAD_ADDRESS_MISALIGNED == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_LOAD_ADDRESS_MISALIGNED == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a LoadAddressMisaligned exception");
    }
} else if (code == ExceptionCode::LoadAccessFault) {
    if (TINST_VALUE_ON_LOAD_ACCESS_FAULT == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_LOAD_ACCESS_FAULT == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a LoadAccessFault exception");
    }
} else if (code == ExceptionCode::StoreAmoAddressMisaligned) {
    if (TINST_VALUE_ON_STORE_AMO_ADDRESS_MISALIGNED == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_STORE_AMO_ADDRESS_MISALIGNED == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a StoreAmoAddressMisaligned exception");
    }
} else if (code == ExceptionCode::StoreAmoAccessFault) {
    if (TINST_VALUE_ON_STORE_AMO_ACCESS_FAULT == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_STORE_AMO_ACCESS_FAULT == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a StoreAmoAccessFault exception");
    }
} else if (code == ExceptionCode::Ucall) {
    if (TINST_VALUE_ON_UCALL == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a UCall exception");
    }
} else if (code == ExceptionCode::Scall) {
    if (TINST_VALUE_ON_SCALL == "always zero") {
        return 0;
    }
```



```

    } else {
        unpredictable("An unpredictable value is written into tinst in response to a SCall exception");
    }
} else if (code == ExceptionCode::Mcall) {
    if (TINST_VALUE_ON_MCALL == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a MCall exception");
    }
} else if (code == ExceptionCode::VScall) {
    if (TINST_VALUE_ON_VSCALL == "always zero") {
        return 0;
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a VSCall exception");
    }
} else if (code == ExceptionCode::InstructionPageFault) {
    return 0;
} else if (code == ExceptionCode::LoadPageFault) {
    if (TINST_VALUE_ON_LOAD_PAGE_FAULT == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_LOAD_PAGE_FAULT == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a LoadPageFault exception");
    }
} else if (code == ExceptionCode::StoreAmoPageFault) {
    if (TINST_VALUE_ON_STORE_AMO_PAGE_FAULT == "always zero") {
        return 0;
    } else if (TINST_VALUE_ON_STORE_AMO_PAGE_FAULT == "always transformed standard instruction") {
        return transformed_standard_instruction_for_tinst(encoding);
    } else {
        unpredictable("An unpredictable value is written into tinst in response to a StoreAmoPageFault exception");
    }
} else {
    assert(false, "Unhandled exception type");
}

```

D.169. gstage_page_walk

Translate guest physical address to physical address through a page walk.

May raise a Guest Page Fault if an error involving the page table structure occurs along the walk.

Implicit reads of the page table are accessed check, and may raise Access Faults. Implicit writes (updates of A/D) are also accessed checked, and may raise Access Faults

The translated address *is not* accessed checked.

Returns the translated physical address.

Return Type	TranslationResult
Arguments	XReg gpaddr, XReg vaddr, MemoryOperation op, PrivilegeMode effective_mode, Boolean for_final_vs_pte, Bits<INSTR_ENC_SIZE> encoding

```

Bits<PA_SIZE> ppn;
TranslationResult result;
U32 VPN_SIZE = (LEVELS == 2) ? 10 : 9;
ExceptionCode access_fault_code = op == MemoryOperation::Read ? ExceptionCode::LoadAccessFault : (op == MemoryOperation::Fetch ?
ExceptionCode::InstructionAccessFault : ExceptionCode::StoreAmoAccessFault);
ExceptionCode page_fault_code = op == MemoryOperation::Read ? ExceptionCode::LoadGuestPageFault : (op == MemoryOperation::Fetch ?
ExceptionCode::InstructionGuestPageFault : ExceptionCode::StoreAmoGuestPageFault);
Boolean mxr = for_final_vs_pte && (CSR[mstatus].MXR == 1);
Boolean pbmt = implemented?(ExtensionName::Svpbmt) && CSR[menvcfg].PBMTE == 1;
Boolean adue = implemented?(ExtensionName::Svadu) && CSR[menvcfg].ADUE == 1;
Bits<32> tinst = tinst_value_for_guest_page_fault(op, encoding, for_final_vs_pte);
U32 max_gpa_width = LEVELS * VPN_SIZE + 2 + 12;
if (gpaddr >> max_gpa_width != 0) {
    raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
}
ppn = CSR[hgatp].PPN;

```

```

for (U32 i = (LEVELS - 1); i >= 0; i--) {
    U32 this_vpn_size = (i == (LEVELS - 1)) ? VPN_SIZE + 2 : VPN_SIZE;
    U32 vpn = (gpaddr >> (12 + VPN_SIZE * i)) & 1 << this_vpn_size) - 1);    Bits<PA_SIZE> pte_paddr = (ppn << 12) + (vpn * (PTESIZE /
8;
    if (!pma_applies?(PmaAttribute::HardwarePageTableRead, pte_paddr, PTESIZE)) {
        raise(access_fault_code, PrivilegeMode::U, vaddr);
    }
    access_check(pte_paddr, PTESIZE, vaddr, MemoryOperation::Read, access_fault_code, effective_mode);
    Bits<PTESIZE> pte = read_physical_memory<PTESIZE>(pte_paddr);
    PteFlags pte_flags = pte[9:0];
    if ((VA_SIZE != 32) && (pte[58:54] != 0)) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if (!implemented?(ExtensionName::Svrsw60t59b)) {
        if ((PTESIZE >= 64) && pte[60:59] != 0) {
            raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
        }
    }
    if (!implemented?(ExtensionName::Svnapot)) {
        if ((PTESIZE >= 64) && pte[63] != 0) {
            raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
        }
    }
    if ((PTESIZE >= 64) && !pbmte && (pte[62:61] != 0)) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if ((PTESIZE >= 64) && pbmte && (pte[62:61] == 3)) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if (pte_flags.V == 0) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if (pte_flags.R == 0 && pte_flags.W == 1) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if (pte_flags.R == 1 || pte_flags.X == 1) {
        if (pte_flags.U == 0) {
            raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
        }
        if (op == MemoryOperation::Write) || (op == MemoryOperation::ReadModifyWrite && (pte_flags.W == 0)) {
            raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
        } else if ((op == MemoryOperation::Fetch) && (pte_flags.X == 0)) {
            raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
        } else if ((op == MemoryOperation::Read) || (op == MemoryOperation::ReadModifyWrite)) {
            if (!mxr) && (pte_flags.R == 0 || mxr) && (pte_flags.X == 0 && pte_flags.R == 0) {
                raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
            }
        }
    }
    if ((i > 0) && (pte[(i - 1) * VPN_SIZE:0] != 0)) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if ((pte_flags.A == 0) || pte_flags.D == 0) && ((op == MemoryOperation::Write) || (op == MemoryOperation::ReadModifyWrite)) {
        if (adue) {
            if (!pma_applies?(PmaAttribute::RsrvEventual, pte_paddr, PTESIZE)) {
                raise(access_fault_code, PrivilegeMode::U, vaddr);
            }
            if (!pma_applies?(PmaAttribute::HardwarePageTableWrite, pte_paddr, PTESIZE)) {
                raise(access_fault_code, PrivilegeMode::U, vaddr);
            }
            access_check(pte_paddr, PTESIZE, vaddr, MemoryOperation::Write, access_fault_code, effective_mode);
            Boolean success;
            Bits<PTESIZE> updated_pte;
            if (pte_flags.D == 0 && (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite)) {
                updated_pte = pte | 0b11000000;
            } else {
                updated_pte = pte | 0b01000000;
            }
            if (PTESIZE == 32) {
                success = atomic_check_then_write_32(pte_paddr, pte, updated_pte);
            } else if (PTESIZE == 64) {
                success = atomic_check_then_write_64(pte_paddr, pte, updated_pte);
            } else {
                assert(false, "Unexpected PTESIZE");
            }
            if (!success) {

```



```
        i = i + 1;
    } else {
        result.paddr = pte_paddr;
        if (PTESIZE >= 64) {
            result.pbmt = $enum(Pbmt, pte[62:61]);
        }
        result.pte_flags = pte_flags;
        return result;
    }
} else {
    raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
}
}
} else {
    if (i == 0) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if (pte_flags.D == 1 || pte_flags.A == 1 || pte_flags.U == 1) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if ((VA_SIZE != 32) && (pte[62:61] != 0)) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    if ((VA_SIZE != 32) && pte[63] != 0) {
        raise_guest_page_fault(op, gpaddr, vaddr, tinst, effective_mode);
    }
    ppn = pte[PA_SIZE - 3:10] << 12;
}
}
```

D.170. stage1_page_walk

Translate virtual address to physical address through a page walk.

May raise a Page Fault if an error involving the page table structure occurs along the walk.

Implicit reads of the page table are accessed check, and may raise Access Faults. Implicit writes (updates of A/D) are also accessed checked, and may raise Access Faults

The translated address *is not* accessed checked.

Returns the translated guest physical address.

Return Type	TranslationResult
Arguments	Bits<MXLEN> vaddr, MemoryOperation op, PrivilegeMode effective_mode, Bits<INSTR_ENC_SIZE> encoding

```
Bits<PA_SIZE> ppn;
TranslationResult result;
U32 VPN_SIZE = (LEVELS == 2) ? 10 : 9;
ExceptionCode access_fault_code = op == MemoryOperation::Read ? ExceptionCode::LoadAccessFault : (op == MemoryOperation::Fetch ? ExceptionCode::InstructionAccessFault : ExceptionCode::StoreAmoAccessFault);
ExceptionCode page_fault_code = op == MemoryOperation::Read ? ExceptionCode::LoadPageFault : (op == MemoryOperation::Fetch ? ExceptionCode::InstructionPageFault : ExceptionCode::StoreAmoPageFault);
Boolean sse = false;
Boolean adue;
if (CSR[misa].H == 1 && (effective_mode == PrivilegeMode::VS || effective_mode == PrivilegeMode::VU)) {
    adue = implemented?(ExtensionName::Svadu) && CSR[henvcfg].ADUE == 1;
} else {
    adue = implemented?(ExtensionName::Svadu) && CSR[menvcfg].ADUE == 1;
}
Boolean pbmte;
if (VA_SIZE == 32) {
    pbmte = false;
} else {
    if (CSR[misa].H == 1 && (effective_mode == PrivilegeMode::VS || effective_mode == PrivilegeMode::VU)) {
        pbmte = implemented?(ExtensionName::Svpbmt) && CSR[henvcfg].PBMTE == 1;
    } else {
        pbmte = implemented?(ExtensionName::Svpbmt) && CSR[menvcfg].PBMTE == 1;
    }
}
```

```

}
Boolean mxr;
if (CSR[misa].H == 1 && (effective_mode == PrivilegeMode::VS || effective_mode == PrivilegeMode::VU)) {
    mxr = (CSR[mstatus].MXR == 1) || (CSR[vsstatus].MXR == 1);
    ppn = CSR[vsatp].PPN;
} else {
    mxr = CSR[mstatus].MXR == 1;
    ppn = CSR[satp].PPN;
}
Boolean sum;
if (CSR[misa].H == 1 && (effective_mode == PrivilegeMode::VS)) {
    sum = CSR[vsstatus].SUM == 1;
} else {
    sum = CSR[mstatus].SUM == 1;
}
if ((VA_SIZE < xlen()) && (vaddr[xlen() - 1:VA_SIZE] != {xlen() - VA_SIZE{vaddr[VA_SIZE - 1]}})) {
    raise(page_fault_code, mode(), vaddr);
}
for (U32 I = (LEVELS - 1); I >= 0; I--) {
    U32 vpn = (vaddr >> (12 + VPN_SIZE * I)) & 1 << VPN_SIZE - 1;    Bits<PA_SIZE> pte_gpaddr = (ppn << 12) + (vpn * (PTESIZE / 8);
    TranslationResult pte_phys = translate_gstage(pte_gpaddr, vaddr, MemoryOperation::Read, effective_mode, encoding);
    if (!pma_applies?(PmaAttribute::HardwarePageTableRead, pte_phys.paddr, PTESIZE)) {
        raise(access_fault_code, mode(), vaddr);
    }
    access_check(pte_phys.paddr, PTESIZE, vaddr, MemoryOperation::Read, access_fault_code, effective_mode);
    Bits<PTESIZE> pte = read_physical_memory<PTESIZE>(pte_phys.paddr);
    PteFlags pte_flags = pte[9:0];
    Boolean ss_page = (pte_flags.R == 0) && (pte_flags.W == 1) && (pte_flags.X == 0);
    if ((VA_SIZE != 32) && (pte[58:54] != 0)) {
        raise(page_fault_code, mode(), vaddr);
    }
    if (pte_flags.V == 0) {
        raise(page_fault_code, mode(), vaddr);
    }
    if (!sse) {
        if ((pte_flags.R == 0) && (pte_flags.W == 1)) {
            raise(page_fault_code, mode(), vaddr);
        }
    }
    if (pbmte) {
        if (pte[62:61] == 3) {
            raise(page_fault_code, mode(), vaddr);
        }
    } else {
        if ((PTESIZE >= 64) && (pte[62:61] != 0)) {
            raise(page_fault_code, mode(), vaddr);
        }
    }
    if (!implemented?(ExtensionName::Svrsw60t59b)) {
        if ((PTESIZE >= 64) && pte[60:59] != 0) {
            raise(page_fault_code, mode(), vaddr);
        }
    }
    if (!implemented?(ExtensionName::Svnapot)) {
        if ((PTESIZE >= 64) && (pte[63] != 0)) {
            raise(page_fault_code, mode(), vaddr);
        }
    }
    if (pte_flags.R == 1 || pte_flags.X == 1) {
        Bits<PA_SIZE> paddr_base = pte[PA_SIZE - 3:I * VPN_SIZE + 10] << (I * VPN_SIZE + 12);
        Bits<PA_SIZE> offset = vaddr[I * VPN_SIZE + 11:0];
        if (op == MemoryOperation::Read || op == MemoryOperation::ReadModifyWrite) {
            if (!mxr) && (pte_flags.R == 0 || mxr) && (pte_flags.X == 0 && pte_flags.R == 0) {
                raise(page_fault_code, mode(), vaddr);
            }
            if (effective_mode == PrivilegeMode::U && pte_flags.U == 0) {
                raise(page_fault_code, mode(), vaddr);
            } else if (CSR[misa].H == 1 && effective_mode == PrivilegeMode::VU && pte_flags.U == 0) {
                raise(page_fault_code, mode(), vaddr);
            } else if (effective_mode == PrivilegeMode::S && pte_flags.U == 1 && !sum) {
                raise(page_fault_code, mode(), vaddr);
            } else if (effective_mode == PrivilegeMode::VS && pte_flags.U == 1 && !sum) {
                raise(page_fault_code, mode(), vaddr);
            }
        }
    }
}
}

```

```

if (op == MemoryOperation::Write) || (op == MemoryOperation::ReadModifyWrite && (pte_flags.W == 0)) {
    raise(page_fault_code, mode(), vaddr);
} else if ((op == MemoryOperation::Fetch) && (pte_flags.X == 0)) {
    raise(page_fault_code, mode(), vaddr);
} else if ((op == MemoryOperation::Fetch) && ss_page) {
    raise(page_fault_code, mode(), vaddr);
}
raise(page_fault_code, mode(), vaddr) if;
if ((pte_flags.A == 0) || pte_flags.D == 0) && ((op == MemoryOperation::Write) || (op == MemoryOperation::ReadModifyWrite)) {
    if (adue) {
        TranslationResult pte_phys = translate_gstage(pte_gpaddr, vaddr, MemoryOperation::Write, effective_mode, encoding);
        if (!pma_applies?(PmaAttribute::RsrvEventual, pte_phys.paddr, PTESIZE)) {
            raise(access_fault_code, effective_mode, vaddr);
        }
        if (!pma_applies?(PmaAttribute::HardwarePageTableWrite, pte_phys.paddr, PTESIZE)) {
            raise(access_fault_code, effective_mode, vaddr);
        }
        access_check(pte_phys.paddr, PTESIZE, vaddr, MemoryOperation::Write, access_fault_code, effective_mode);
        Boolean success;
        Bits<PTESIZE> updated_pte;
        if (pte_flags.D == 0 && (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite)) {
            updated_pte = pte | 0b11000000;
        } else {
            updated_pte = pte | 0b01000000;
        }
        if (PTESIZE == 32) {
            success = atomic_check_then_write_32(pte_phys.paddr, pte, updated_pte);
        } else if (PTESIZE == 64) {
            success = atomic_check_then_write_64(pte_phys.paddr, pte, updated_pte);
        } else {
            assert(false, "Unexpected PTESIZE");
        }
        if (!success) {
            I = I + 1;
        } else {
            TranslationResult pte_phys = translate_gstage(paddr_base + offset, vaddr, op, effective_mode, encoding);
            result.paddr = pte_phys.paddr;
            result.pbmt = pte_phys.pbmt == Pbmt::PMA ? $enum(Pbmt, pte[62:61]) : pte_phys.pbmt;
            result.pte_flags = pte_flags;
            return result;
        }
    } else {
        raise(page_fault_code, mode(), vaddr);
    }
}
TranslationResult pte_phys = translate_gstage(paddr_base + offset, vaddr, op, effective_mode, encoding);
result.paddr = pte_phys.paddr;
if (PTESIZE >= 64) {
    result.pbmt = pte_phys.pbmt == Pbmt::PMA ? $enum(Pbmt, pte[62:61]) : pte_phys.pbmt;
}
result.pte_flags = pte_flags;
return result;
} else {
    if (I == 0) {
        raise(page_fault_code, mode(), vaddr);
    }
    if (pte_flags.D == 1 || pte_flags.A == 1 || pte_flags.U == 1) {
        raise(page_fault_code, mode(), vaddr);
    }
    if ((VA_SIZE != 32) && (pte[62:61] != 0)) {
        raise(page_fault_code, mode(), vaddr);
    }
    if ((VA_SIZE != 32) && pte[63] != 0) {
        raise(page_fault_code, mode(), vaddr);
    }
    ppn = pte[PA_SIZE - 3:10];
}
}

```

D.171. translate

Translate a virtual address for operation type `op` that appears to execute at `effective_mode`.

The translation will depend on the effective privilege mode.

May raise a Page Fault or Access Fault.

The final physical address is **not** access checked (for PMP, PMA, etc., violations). (though intermediate page table reads will be)

Return Type	TranslationResult
Arguments	XReg vaddr, MemoryOperation op, PrivilegeMode effective_mode, Bits<INSTR_ENC_SIZE> encoding

```
Boolean cached_translation_valid;
CachedTranslationResult cached_translation_result;
cached_translation_result = cached_translation(vaddr, op);
if (cached_translation_result.valid) {
    return cached_translation_result.result;
}
TranslationResult result;
if (effective_mode == PrivilegeMode::M) {
    result.paddr = vaddr;
    return result;
}
SatpMode translation_mode = current_translation_mode(effective_mode);
if (translation_mode == SatpMode::Reserved) {
    if (op == MemoryOperation::Read) {
        raise(ExceptionCode::LoadPageFault, mode(), vaddr);
    } else if (op == MemoryOperation::Write || op == MemoryOperation::ReadModifyWrite) {
        raise(ExceptionCode::StoreAmoPageFault, mode(), vaddr);
    } else {
        assert(op == MemoryOperation::Fetch, "Unexpected memory operation");
        raise(ExceptionCode::InstructionPageFault, mode(), vaddr);
    }
}
if (translation_mode == SatpMode::Bare) {
    result.paddr = vaddr;
} else if (xlen() == 32 && translation_mode == SatpMode::Sv32) {
    result = stage1_page_walk<32, 34, 32, 2>(vaddr, op, effective_mode, encoding);
} else if (xlen() == 64 && translation_mode == SatpMode::Sv39) {
    result = stage1_page_walk<39, 56, 64, 3>(vaddr, op, effective_mode, encoding);
} else if (xlen() == 64 && translation_mode == SatpMode::Sv48) {
    result = stage1_page_walk<48, 56, 64, 4>(vaddr, op, effective_mode, encoding);
} else if (xlen() == 64 && translation_mode == SatpMode::Sv57) {
    result = stage1_page_walk<57, 56, 64, 5>(vaddr, op, effective_mode, encoding);
} else {
    assert(false, "Unexpected SatpMode");
}
maybe_cache_translation(vaddr, op, result);
return result;
```

D.172. canonical_vaddr?

Returns whether or not *vaddr* is a valid (*i.e.*, canonical) virtual address.

If pointer masking (S**pm) is enabled, then vaddr will be masked before checking the canonical address.

Return Type	Boolean
Arguments	XReg vaddr

```
if (CSR[misa].S == 1'b0) {
    return true;
}
SatpMode satp_mode;
if (virtual_mode?()) {
    satp_mode = $enum(SatpMode, CSR[vsatp].MODE);
} else {
    satp_mode = $enum(SatpMode, CSR[satp].MODE);
}
```

```

}
XReg eaddr = mask_eaddr(vaddr);
if (SATP_MODE_BARE && (satp_mode == SatpMode::Bare)) {
    return true;
} else if ((MXLEN == 32) && satp_mode == SatpMode::Sv32) {
    return true;
} else if ((MXLEN == 64) && satp_mode == SatpMode::Sv39) {
    return eaddr[63:39] == {25{eaddr[38]}};
} else if ((MXLEN == 64) && satp_mode == SatpMode::Sv48) {
    return eaddr[63:48] == {16{eaddr[47]}};
} else if ((MXLEN == 64) && satp_mode == SatpMode::Sv57) {
    return eaddr[63:57] == {6{eaddr[56]}};
}

```

D.173. canonical_gpaddr?

Returns whether or not gpaddr is a valid (*i.e.*, canonical) guest physical address.

Return Type	Boolean
Arguments	XReg gpaddr

```

SatpMode satp_mode = $enum(SatpMode, CSR[satp].MODE);
if (satp_mode == SatpMode::Bare) {
    return true;
} else if (satp_mode == SatpMode::Sv32) {
    return true;
} else if ((MXLEN > 32) && (satp_mode == SatpMode::Sv39)) {
    return gpaddr[63:39] == {25{gpaddr[38]}};
} else if ((MXLEN > 32) && (satp_mode == SatpMode::Sv48)) {
    return gpaddr[63:48] == {16{gpaddr[47]}};
} else if ((MXLEN > 32) && (satp_mode == SatpMode::Sv57)) {
    return gpaddr[63:57] == {6{gpaddr[56]}};
}

```

D.174. misaligned_is_atomic?

Returns true if an access starting at physical_address that is N bits long is atomic.

This function takes into account any Atomicity Granule PMAs, so **it should not be used for load-reserved/store-conditional**, since those PMAs do not apply to those accesses.

Return Type	Boolean
Arguments	Bits<PHYS_ADDR_WIDTH> physical_address

```

return false if (MISALIGNED_MAX_ATOMICITY_GRANULE_SIZE == 0);
if (pma_applies?(PmaAttribute::MAG16, physical_address, N) && in_naturally_aligned_region?<128>(physical_address, N)) {
    return true;
} else if (pma_applies?(PmaAttribute::MAG8, physical_address, N) && in_naturally_aligned_region?<64>(physical_address, N)) {
    return true;
} else if (pma_applies?(PmaAttribute::MAG4, physical_address, N) && in_naturally_aligned_region?<32>(physical_address, N)) {
    return true;
} else if (pma_applies?(PmaAttribute::MAG2, physical_address, N) && in_naturally_aligned_region?<16>(physical_address, N)) {
    return true;
} else {
    return false;
}

```

D.175. read_memory_aligned

Read from virtual memory using a known aligned address.

Return Type	Bits<LEN>
Arguments	XReg virtual_address, Bits<INSTR_ENC_SIZE> encoding

```

TranslationResult result;
if (CSR[misa].S == 1) {
    result = translate(virtual_address, MemoryOperation::Read, effective_ldst_mode(), encoding);
} else {
    result.paddr = virtual_address;
}
access_check(result.paddr, LEN, virtual_address, MemoryOperation::Read, ExceptionCode::LoadAccessFault, effective_ldst_mode());
return read_physical_memory<LEN>(result.paddr);

```

D.176. read_memory

Read from virtual memory.

Return Type	Bits<LEN>
Arguments	XReg virtual_address, Bits<INSTR_ENC_SIZE> encoding

```

Boolean aligned = is_naturally_aligned<LEN>(virtual_address);
XReg physical_address;
if (aligned) {
    return read_memory_aligned<LEN>(virtual_address, encoding);
}
if (MISALIGNED_MAX_ATOMICITY_GRANULE_SIZE > 0) {
    assert(MISALIGNED_LDST_EXCEPTION_PRIORITY == "low", "Invalid config: can't mix low-priority misaligned exceptions with large atomicity granule");
    physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Read, effective_ldst_mode(), encoding).paddr : virtual_address;
    if (misaligned_is_atomic?<LEN>(physical_address)) {
        access_check(physical_address, LEN, virtual_address, MemoryOperation::Read, ExceptionCode::LoadAccessFault, effective_ldst_mode());
        return read_physical_memory<LEN>(physical_address);
    }
}
if (!MISALIGNED_LDST) {
    if (MISALIGNED_LDST_EXCEPTION_PRIORITY == "low") {
        physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Read, effective_ldst_mode(), encoding).paddr : virtual_address;
        access_check(physical_address, LEN, virtual_address, MemoryOperation::Read, ExceptionCode::LoadAccessFault, effective_ldst_mode());
    }
    raise(ExceptionCode::LoadAddressMisaligned, mode(), virtual_address);
} else {
    if (MISALIGNED_SPLIT_STRATEGY == "sequential_bytes") {
        Bits<LEN> result = 0;
        for (U32 I = 0; I < (LEN / 8); I++) {
            result = result | (read_memory_aligned<8>(virtual_address + I, encoding) '<< (8 * I));
        }
        return result;
    } else if (MISALIGNED_SPLIT_STRATEGY == "custom") {
        unpredictable("An implementation is free to break a misaligned access any way, leading to unpredictable behavior when any part of the misaligned access causes an exception");
    }
}

```

D.177. read_memory_xlen

Read XLEN bits from memory

Return Type	Bits<MXLEN>

Arguments	XReg virtual_address, Bits<INSTR_ENC_SIZE> encoding

```

if (xlen() == 32) {
    return read_memory<32>(virtual_address, encoding);
} else {
    return read_memory<64>(virtual_address, encoding);
}

```

D.178. write_memory_xlen

Read XLEN bits from memory

Return Type	void
Arguments	XReg virtual_address, Bits<MXLEN> value, Bits<INSTR_ENC_SIZE> encoding

```

if (xlen() == 32) {
    return write_memory<32>(virtual_address, value, encoding);
} else {
    return write_memory<64>(virtual_address, value, encoding);
}

```

D.179. read_memory_xlen_aligned

Read from virtual memory XLEN (which may be runtime-determined) bits using a known aligned address.

Return Type	Bits<MXLEN>
Arguments	XReg virtual_address, Bits<INSTR_ENC_SIZE> encoding

```

TranslationResult result;
if (CSR[misa].S == 1) {
    result = translate(virtual_address, MemoryOperation::Read, effective_ldst_mode(), encoding);
} else {
    result.paddr = virtual_address;
}
access_check(result.paddr, xlen(), virtual_address, MemoryOperation::Read, ExceptionCode::LoadAccessFault, effective_ldst_mode());
if (xlen() == 32) {
    return read_physical_memory<32>(result.paddr);
} else {
    return read_physical_memory<64>(result.paddr);
}

```

D.180. invalidate_reservation_set

Invalidates any currently held reservation set.



This function may be called by the platform, independent of any actions occurring in the local hart, for any or no reason.

The platform **must** call this function if an external hart or device accesses part of this reservation set while reservation_set_valid could be true.

Return Type	void
Arguments	None

```

reservation_set_valid = false;

```

D.181. register_reservation_set

Register a reservation for a physical address range that subsumes [physical_address, physical_address + N).

Return Type	void
Arguments	Bits<MXLEN> physical_address, Bits<MXLEN> length

```
reservation_set_valid = true;
reservation_set_address = physical_address;
if (LRSC_RESERVATION_STRATEGY == "reserve naturally-aligned 64-byte region") {
    reservation_set_address = physical_address & ~MXLEN'h3f;
    reservation_set_size = 64;
} else if (LRSC_RESERVATION_STRATEGY == "reserve naturally-aligned 128-byte region") {
    reservation_set_address = physical_address & ~MXLEN'h7f;
    reservation_set_size = 128;
} else if (LRSC_RESERVATION_STRATEGY == "reserve exactly enough to cover the access") {
    reservation_set_address = physical_address;
    reservation_set_size = length;
} else if (LRSC_RESERVATION_STRATEGY == "custom") {
    unpredictable("Implementations may set reservation sets of any size, as long as they cover the reserved accessed");
} else {
    assert(false, "Unexpected LRSC_RESERVATION_STRATEGY");
}
```

D.182. load_reserved

Register a reservation for virtual_address at least N bits long and read the value from memory.

If aq is set, then also perform a memory model acquire.

If rl is set, then also perform a memory model release (software is discouraged from doing so).

This function assumes alignment checks have already occurred.

Return Type	Bits<N>
Arguments	Bits<MXLEN> virtual_address, Bits<1> aq, Bits<1> rl, Bits<INSTR_ENC_SIZE> encoding

```
Bits<PHYS_ADDR_WIDTH> physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Read,
effective_ldst_mode(), encoding).paddr : virtual_address;
if (pma_applies?(PmaAttribute::RsrvNone, physical_address, N)) {
    raise(ExceptionCode::LoadAccessFault, mode(), virtual_address);
}
if (aq == 1) {
    memory_model_acquire();
}
if (rl == 1) {
    memory_model_release();
}
register_reservation_set(physical_address, N);
if (CSR[misa].S == 1 && LRSC_FAIL_ON_VA_SYNONYM) {
    reservation_virtual_address = virtual_address;
}
return read_memory_aligned<N>(physical_address, encoding);
```

D.183. store_conditional

Atomically check the reservation set to ensure:

- it is valid
- it covers the region addressed by this store
- the address setting the reservation set matches virtual address

If the preceding are met, perform the store and return 0. Otherwise, return 1.

Return Type	Boolean
Arguments	Bits<MXLEN> virtual_address, Bits<MXLEN> value, Bits<1> aq, Bits<1> rl, Bits<INSTR_ENC_SIZE> encoding

```
Bits<PHYS_ADDR_WIDTH> physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Write,
effective_ldst_mode(), encoding).paddr : virtual_address;
if (pma_applies?(PmaAttribute::RsrvNone, physical_address, N)) {
    raise(ExceptionCode::StoreAmoAccessFault, mode(), virtual_address);
}
access_check(physical_address, N, virtual_address, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
if (aq == 1) {
    memory_model_acquire();
}
if (rl == 1) {
    memory_model_release();
}
if (reservation_set_valid == false) {
    return false;
}
if (!contains?(reservation_set_address, reservation_set_size, physical_address, N)) {
    invalidate_reservation_set();
    return false;
}
if (LRSC_FAIL_ON_NON_EXACT_LRSC) {
    if (reservation_physical_address != physical_address || reservation_size != N) {
        invalidate_reservation_set();
        return false;
    }
}
if (LRSC_FAIL_ON_VA_SYNONYM) {
    if (reservation_virtual_address != virtual_address || reservation_size != N) {
        invalidate_reservation_set();
        return false;
    }
}
write_physical_memory<N>(physical_address, value);
return true;
```

D.184. amo

Atomically read-modify-write the location at virtual_address.

The value written to virtual_address will depend on op.

If aq is 1, then the amo also acts as a memory model acquire. If rl is 1, then the amo also acts as a memory model release.

Return Type	Bits<N>
Arguments	XReg virtual_address, Bits<N> value, AmoOperation op, Bits<1> aq, Bits<1> rl, Bits<INSTR_ENC_SIZE> encoding

```
Boolean aligned = is_naturally_aligned<N>(virtual_address);
if (!aligned && MISALIGNED_LDST_EXCEPTION_PRIORITY == "high") {
    raise(ExceptionCode::StoreAmoAddressMisaligned, mode(), virtual_address);
}
Bits<PHYS_ADDR_WIDTH> physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::ReadModifyWrite,
effective_ldst_mode(), encoding).paddr : virtual_address;
if (pma_applies?(PmaAttribute::AmoNone, physical_address, N)) {
    raise(ExceptionCode::StoreAmoAccessFault, mode(), virtual_address);
} else if (op == AmoOperation::Add || op == AmoOperation::Max || op == AmoOperation::Maxu || op == AmoOperation::Min || op ==
AmoOperation::Minu && !pma_applies?(PmaAttribute::AmoArithmetic, physical_address, N)) {
    raise(ExceptionCode::StoreAmoAccessFault, mode(), virtual_address);
} else if (op == AmoOperation::And || op == AmoOperation::Or || op == AmoOperation::Xor && !pma_applies?(PmaAttribute::AmoLogical,
```

```
physical_address, N)) {
    raise(ExceptionCode::StoreAmoAccessFault, mode(), virtual_address);
} else {
    assert(pma_applies?(PmaAttribute::AmoSwap, physical_address, N) && op == AmoOperation::Swap, "Bad AMO operation");
}
if (!aligned && !misaligned_is_atomic?<N>(physical_address)) {
    raise(ExceptionCode::StoreAmoAddressMisaligned, mode(), virtual_address);
}
if (N == 32) {
    return atomic_read_modify_write_32(physical_address, value, op);
} else {
    return atomic_read_modify_write_64(physical_address, value, op);
}
```

D.185. write_memory_aligned

Write to virtual memory using a known aligned address.

Return Type	void
Arguments	XReg virtual_address, Bits<LEN> value, Bits<INSTR_ENC_SIZE> encoding

```
XReg physical_address;
physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Write, effective_ldst_mode(), encoding).paddr :
virtual_address;
access_check(physical_address, LEN, virtual_address, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
write_physical_memory<LEN>(physical_address, value);
```

D.186. write_memory

Write to virtual memory

Return Type	void
Arguments	XReg virtual_address, Bits<LEN> value, Bits<INSTR_ENC_SIZE> encoding

```
Boolean aligned = is_naturally_aligned<LEN>(virtual_address);
XReg physical_address;
if (aligned) {
    write_memory_aligned<LEN>(virtual_address, value, encoding);
    return ;
}
if (MISALIGNED_MAX_ATOMICITY_GRANULE_SIZE > 0) {
    assert(MISALIGNED_LDST_EXCEPTION_PRIORITY == "low", "Invalid config: can't mix low-priority misaligned exceptions with large
atomicity granule");
    physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Write, effective_ldst_mode(), encoding).paddr
: virtual_address;
    if (misaligned_is_atomic?<LEN>(physical_address)) {
        access_check(physical_address, LEN, virtual_address, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
        write_physical_memory<LEN>(physical_address, value);
        return ;
    }
}
if (!MISALIGNED_LDST) {
    if (MISALIGNED_LDST_EXCEPTION_PRIORITY == "low") {
        physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Write, effective_ldst_mode(),
encoding).paddr : virtual_address;
        access_check(physical_address, LEN, virtual_address, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
    }
    raise(ExceptionCode::StoreAmoAddressMisaligned, mode(), virtual_address);
} else {
    if (MISALIGNED_SPLIT_STRATEGY == "sequential_bytes") {
        for (U32 I = 0; I < (LEN / 8); I++) {
```

```
        write_memory_aligned<8>(virtual_address + I, (value >> (8 * I))[7:0], encoding);
    }
} else if (MISALIGNED_SPLIT_STRATEGY == "custom") {
    unpredictable("An implementation is free to break a misaligned access any way, leading to unpredictable behavior when any part
of the misaligned access causes an exception");
}
}
```

D.187. write_memory_xlen_aligned

Write to virtual memory XLEN bits (which may be runtime determined) using a known aligned address.

Return Type	void
Arguments	XReg virtual_address, Bits<MXLEN> value, Bits<INSTR_ENC_SIZE> encoding

```
XReg physical_address;
physical_address = (CSR[misa].S == 1) ? translate(virtual_address, MemoryOperation::Write, effective_ldst_mode(), encoding).paddr :
virtual_address;
access_check(physical_address, xlen(), virtual_address, MemoryOperation::Write, ExceptionCode::StoreAmoAccessFault,
effective_ldst_mode());
if (xlen() == 32) {
    write_physical_memory<32>(physical_address, value);
} else {
    write_physical_memory<64>(physical_address, value);
}
```

D.188. mstatus_sd_has_known_reset

Returns true if the mstatus.SD bit has a defined reset value, as determined by various parameters.

Return Type	Boolean
Arguments	None

```
Boolean fs_has_single_value = !implemented?(ExtensionName::F || ($array_size(MSTATUS_FS_LEGAL_VALUES) == 1));
Boolean vs_has_single_value = !implemented?(ExtensionName::V || ($array_size(MSTATUS_VS_LEGAL_VALUES) == 1));
return fs_has_single_value && vs_has_single_value;
```

D.189. mstatus_sd_reset_value

Returns the reset value of mstatus.SD when known

Return Type	Bits①
Arguments	None

```
assert(mstatus_sd_has_known_reset(), "mstatus_sd_reset_value is only defined when mstatus_sd_has_known_reset() == true");
Bits<2> fs_value, vs_value;
if ((!implemented?(ExtensionName::F)) || ($array_size(MSTATUS_FS_LEGAL_VALUES) == 1)) {
    fs_value = (!implemented?(ExtensionName::F)) ? 0 : MSTATUS_FS_LEGAL_VALUES[0];
}
if ((!implemented?(ExtensionName::V)) || ($array_size(MSTATUS_VS_LEGAL_VALUES) == 1)) {
    fs_value = (!implemented?(ExtensionName::V)) ? 0 : MSTATUS_VS_LEGAL_VALUES[0];
}
return fs_value == 3) || (vs_value == 3 ? 1 : 0;
```

D.190. check_zcmt_enabled

If the Smstateen extension is implemented, then bit 2 in mstateen0, sstateen0, and hstateen0 is implemented. If bit 2 of a controlling stateen0 CSR is zero, then access to the jvt CSR and execution of a cm.jalt or cm.jt instruction by a lower privilege level results in an illegal-instruction trap (or, if appropriate, a virtual-instruction trap).

Return Type	void
Arguments	Bits<INSTR_ENC_SIZE> encoding

```
if ((mode() != PrivilegeMode::M && implemented?(ExtensionName::Smstateen) && CSR[mstateen0].JVT == 1'b0) || (mode() == PrivilegeMode::U && implemented?(ExtensionName::Ssstateen) && CSR[sstateen0].JVT == 1'b0)) {
    raise(ExceptionCode::IllegalInstruction, mode(), encoding);
} else if ((mode() == PrivilegeMode::VS && implemented?(ExtensionName::Ssstateen) && CSR[hstateen0].JVT == 1'b0) || (mode() == PrivilegeMode::VU && implemented?(ExtensionName::Ssstateen) && (CSR[sstateen0].JVT == 1'b0 || CSR[hstateen0].JVT == 1'b0))) {
    raise(ExceptionCode::VirtualInstruction, mode(), encoding);
}
```